Chapter 4

All-optical logic gates based on SPTMI coupler

Contents

4.1 Introduction

As discussed in chapter 2, all-optical control of optical processor devices have become essential to achieve faster operation of the devices in present day's high speed communication system. High performance all-optical logic gates have become key components in optical computing and networking systems to perform optical signal processing functions such as binary addition, parity checking, header reorganization, all-optical label swapping and data encryption [10]. Over the last few years, various technologies have been reported to realize all-optical logic operations. But most of those reported works suffer from some fundamental limitations such as large size [67–69], complex architecture [66, 76, 78, 129] , instability [27, 79, 80, 84], difficulty in cascading [26, 83] and very few or single logic [72, 81, 82, 85] functions.

In this chapter, all-optical fundamental logic gates have been designed with the help of the surface plasmonic two-mode interference (SPTMI) coupler discussed in chapter 3. By using a single 2×2 SPTMI coupler, basic logic operations NOT, AND and OR have been realized. By cascading three stages of the SPTMI coupler, optically-controlled NAND, NOR and XOR operations have been implemented. Implementation of different logic functions are controlled by the optical pulse applied at the nonlinear cladding and the power incident at the two single mode input access waveguides.

4.2 Implementation of fundamental logic operation

In optical logic operations, the logic '1' or logic 'high' represents the presence of optical power, whereas the logic '0' or logic 'low' means absence of optical power. All-optical fundamental logic operations can be realized using the basic surface plasmonic two-mode interference (SPTMI) coupler shown in Fig-4.1 (discussed in chapter 3). The proposed structure consists of two-mode coupling region of core width $2w = 0.48\mu m$, core thickness $t = 5.0\mu m$ and length $L = 92.35\mu m$ and two single mode input access waveguides and two single mode output access waveguides having core width $w = 0.24\mu m$ and core thickness $t = 5.0\mu m$. The core material is silicon with refractive index n_1 and the claddings are made up of GaAsInP (refractive index $n_2(E)$) on the left and right side and silver (refractive index n_m) on upper and lower side. The input powers P_1 and P_2 are launched

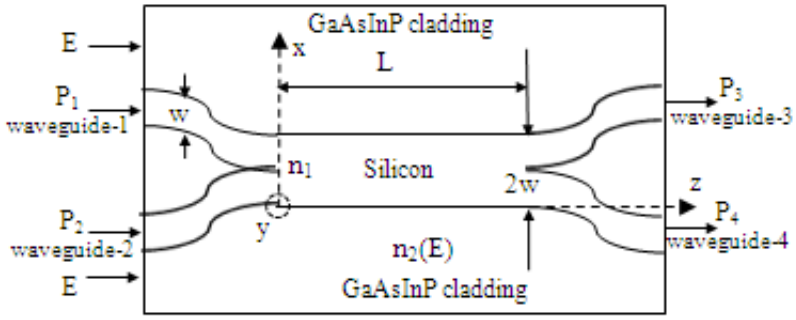


Figure 4.1: SPTMI coupler for fundamental logic operations

into TMI region through input access waveguide-1 and waveguide-2, whereas optical pulse of energy E and width T_P is applied at the GaAsInP cladding. The output power at access waveguide-3 and waveguide-4 are obtained as P_3 and P_4 respectively.

The optical pulse controlled switching operation of the SPTMI coupler has already been discussed in chapter 3. When an input power is incident at input access waveguide-1, SPP fundamental and first order modes are excited in the two-mode coupling region. As these two modes propagate along the coupling region with different phase velocities, the phase difference between the two modes increases. When an optical pulse is applied at the nonlinear GaAsInP cladding in the device, the resulting refractive index modulation of GaAsInP cladding introduces an additional phase difference between the two propagating modes. The phase change between the two-modes can be expressed as

$$\Delta\Phi_T(E) = \left[\beta_0^r(n_2(0)) - \beta_1^r(n_2(0))\right] L + \frac{2\pi L}{\lambda}\left[\Delta n_{1,r}^{eff}(E) - \Delta n_{0,r}^{eff}(E)\right] \quad (4.1)$$

where, the first term gives the phase difference between the two modes before application of optical pulse and the second term is the additional phase change introduced due to application of optical pulse at cladding. $\beta_0^r(n_2(0))$ and $\beta_1^r(n_2(0))$ are the real parts of propagation constants of zeroth order mode and first order mode before application of optical pulse and λ is the wavelength of operation. $\Delta n_{0,r}^{eff}(E)$ and $\Delta n_{1,r}^{eff}(E)$ are respectively the effective real refractive index change of fundamental mode and first order mode due to applied optical pulse. When the additional phase difference introduced due to applied optical pulse becomes π, switching of coupling states is observed in the device.

The expression for the output power at bar state output access waveguide-3 (P_3) and cross state output access waveguide-4 (P_4) at the end

of the coupling region at a distance L can be written as

$$P_3 = |H_3(x, L, E)|^2 \tag{4.2}$$
$$P_4 = |H_4(x + w, L, E)|^2 \tag{4.3}$$

where, $H_3(x, L, E)$ and $H_4(x + w, L, E)$ are the field profiles at output access waveguide-3 and waveguide-4 respectively, at a distance L at the end of the coupling region. From equations (3.21) and (3.22) in section 3.4.3 of previous chapter, it is seen that the normalized bar state coupling power P_3 and cross state coupling power P_4 are functions of the phase difference ($\Delta\Phi_T(E)$) between the SPP fundamental mode and first order mode excited in the two-mode coupling region.

It is already discussed in chapter 3 that, for a two-mode coupling region of length $L = 92.35\mu m$, the phase difference between the two SPP modes on absence of optical pulse energy ($E = 0$) is π ($\Delta\Phi_T(0) = \pi$) and the SPTMI coupler shows cross state coupling. The corresponding output power for $E = 0$ are given by

$$P_3 = |H_3(x, L, E)|^2 = 0 \tag{4.4}$$
$$P_4 = |H_4(x + w, L, E)|^2 = 1 \tag{4.5}$$

where, 1 and 0 respectively denote the presence and absence of output power. When an optical pulse of energy $E = 16.4pJ$ and width $T_P = 1ps$ is applied at the GaAsInP cladding, refractive index modulation of GaAsInP cladding occurs [124] and an additional phase change of π is introduced between the two SPP modes ($\Delta\Phi_T(E) = 2\pi$) which changes the cross state coupling of the device to bar state coupling. The corresponding output power are obtained as

$$P_3 = |H_3(x, L, E)|^2 = 1 \tag{4.6}$$
$$P_4 = |H_4(x + w, L, E)|^2 = 0 \tag{4.7}$$

By using the power launched in waveguide-1 (P_1) as control signal and optical pulse of energy E applied in cladding region and optical power launched into input waveguide-2 (P_2) as input signals, NOT, AND and OR logic gates can be implemented with the SPTMI coupler. The output states of logic gates are obtained at either output waveguide-3 (P_3) or output waveguide-4 (P_4). Table-4.1 shows values of designed parameters of the proposed device shown in Fig-4.1

(discussed in the chapter-3) for logic gate operation.

Table 4.1: Device parameters required for fundamental logic gate operation

Device parameters	**Values**
Core (silicon) refractive index (n_1)	3.5
Metal (silver) cladding refractive index (n_m)	$0.394 + 8.2j$
Side (GaAsInP) cladding refractive index ($n_2(0)$)	3.17
Side (GaAsInP) cladding nonlinear coefficient (n_{nl})	$-2 \times 10^{-3} \mu m^2 W^{-1}$
Wavelength of operation (λ)	$1.33 \mu m$
Core width ($2w$)	$0.48 \mu m$
Core thickness (t)	$5.0 \mu m$
Bending radius of access waveguides (R)	$39 \mu m$
Separation between access waveguides	$8 \mu m$
Transition length of access waveguides (L_T)	$24.97 \mu m$
Area of GaAsInP cladding region (A_{clad})	$2.0 \mu m^2$
Area of metal cladding region	$4.4 \mu m^2$
Energy of pulse applied (E)	$16.4 pJ$
Full width at half maximum of pulse (T_P)	$1 ps$
Length of coupling region (L)	$92.35 \mu m$
Device length	$142.29 \mu m$

It is possible to produce any digital system using the fundamental logic gates NOT, AND and OR. The implementation of these all-optical fundamental logic operations based on SPTMI coupler are explained in the succeeding sections:

4.2.1 All-optical NOT gate

The NOT operation is one of the most basic operations in a digital system. The truth table of a basic NOT gate is shown in Table-4.2. Basically, this boolean function gives a logic '1' (logic 'high') if the input is at logic '0' (logic 'low') and a logic '0' (logic 'low') if the input is at logic '1' (logic 'high'). In other words, the NOT gate inverts a digital signal and is also known as the 'inverter'. In boolean equation form, the NOT gate is denoted as $Y = \overline{A}$.

Table 4.2: Truth table for a basic NOT gate

Input	Output
A	**Y**
0	1
1	0

The NOT gate operation is obtained by launching control signal into waveguide-1 and applying optical pulse of energy E at GaAsInP cladding region as the input signal. The output power is taken at waveguide-4 (P_4). The input-output logic combinations for SPTMI based all-optical NOT logic gate are shown in Fig-4.2. The principle of operation of SPTMI based all-optical NOT logic gate

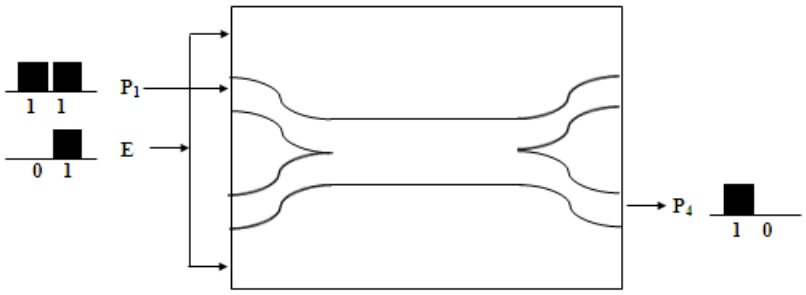


Figure 4.2: Implementation of NOT logic operation using SPTMI coupler

are explained by using $P_1 = 1$ as control signal. There are two cases for NOT truth table as given below-

- **Case 1:** $E = 0$ (logic '0')
  When no optical pulse is applied at the GaAsInP cladding (treated as '0' state), the phase difference between the propagating modes is given by $\Delta\Phi_T(0) = \pi$. The SPTMI coupler shows cross state coupling and the power incident on waveguide-1 is transferred to waveguide-4. The power at the output access waveguides are given by

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 0 \\ P_4 &= |H_4(x + w, L, E)|^2 = 1 \end{aligned}$$

- **Case 2:** $E = 16.4pJ$ (logic '1')
  When optical pulse of energy $E = 16.4pJ$ (treated as '1' state) is applied in cladding region, an additional phase difference of π is introduced between

the SPP fundamental and first order modes propagating in the SPTMI waveguide ($\Delta\Phi_T(E) = 2\pi$) and the cross state coupling is changed to bar state coupling. The power at waveguide-1 is transferred to waveguide-3 and no power ('0' state) is coupled to waveguide-4. The power at the output access waveguides are given by

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 1 \\ P_4 &= |H_4(x + w, L, E)|^2 = 0 \end{aligned}$$

Thus, the output power of waveguide-4 shows NOT gate characteristics in the proposed SPP device. The input and output logic states for the all-optical NOT logic operation implemented with the basic SPTMI coupler is shown in Table-4.3.

Table 4.3: Truth table for all-optical NOT gate implemented with SPTMI coupler

Control	**Input**	**Output**
P_1	E	P_4
1	0	1
1	1	0

4.2.2 All-optical AND gate

The AND gate is a digital circuit with two or more inputs and a single output. The output of AND gate is obtained at logic 'high' only when all the inputs are at logic 'high' state. Table-4.4 summarizes all the input-output possibilities of a 2-input AND logic gate. Basically, this boolean function gives a logic '1' only when both the two inputs are at logic '1' (combination (1,1)). If any one of the input signals is at logic '0', the output signal is also obtained at logic '0' state (combinations (0,0), (0,1) and (1,0)). In boolean equation form, this logic operation is denoted as $Y = AB$.

All-optical AND logic operation can be realized with the SPTMI coupler discussed in preceding chapter by using optical pulse of energy E applied at GaAsInP cladding region as first input signal and optical power launched into input waveguide-2 (P_2) as second input signal. The control signal or the power at input access waveguide-1 is not required for AND logic operation. The output

Table 4.4: Truth table for a basic AND gate

Inputs		Output
A	**B**	**Y**
0	0	0
0	1	0
1	0	0
1	1	1

states of logic gates are obtained at the output waveguide-4 (P_4). The various input-output combinations for the SPTMI based all-optical AND logic gate are depicted in Fig-4.3. The working principle of SPTMI based all-optical AND logic

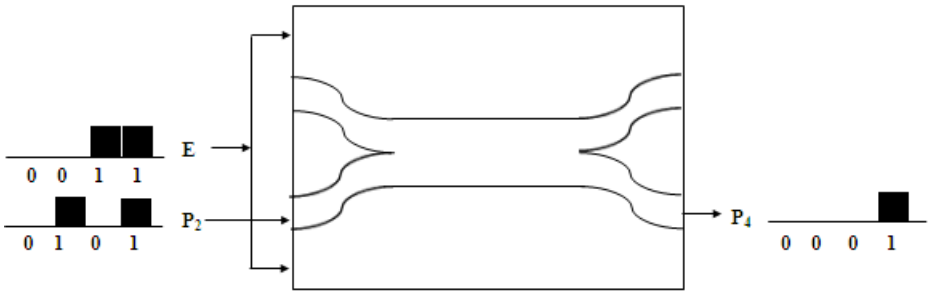


Figure 4.3: Implementation of AND logic operation using SPTMI coupler

gate are explained by using $P_1 = 0$ as control signal. There are four cases for truth table of AND gate, as given below-

- **Case 1:** E='0', P_2='0'
  When no optical pulse is applied at the cladding region ($E = 0$) and no power is incident on waveguide-2 ($P_2 = 0$), there is no power in the core of the waveguide and hence, there is no power at output waveguide-3 and waveguide-4. Thus, we get

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 0 \\ P_4 &= |H_4(x + w, L, E)|^2 = 0 \end{aligned}$$

- **Case 2:** E='0', P_2='1'
  When no input optical pulse is applied in cladding region ($E = 0$), and input power is incident in waveguide-2 ($P_2 = 1$), the phase difference between the SPP modes is given by $\Delta\Phi_T(0) = \pi$. The power at waveguide-2

is transferred to output waveguide-3 and no output power is obtained at waveguide-4 due to cross state coupling of device. The power at the output waveguides can be given by

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 1 \\ P_4 &= |H_4(x + w, L, E)|^2 = 0 \end{aligned}$$

- **Case 3:** E='1', P_2='0'
  When optical pulse of energy $E = 16.4pJ$ is applied to cladding region and no power is incident on waveguide-2 ($P_2 = 0$), there is no power at waveguide-3 and waveguide-4 due to having no power at the core of the proposed device. Thus, we get

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 0 \\ P_4 &= |H_4(x + w, L, E)|^2 = 0 \end{aligned}$$

- **Case 4:** E='1', P_2='1'
  When input power is applied to waveguide-2 ($P_2 = 1$) and optical pulse of energy $E = 16.4pJ$ is applied at cladding region, the phase difference between the SPP modes is given by $\Delta\Phi_T(E) = 2\pi$ and the coupling state changes from cross state to bar state. Thus, the output signal is obtained at waveguide-4 due to transfer of power from waveguide-2. The power at the output waveguides can be given by

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 0 \\ P_4 &= |H_4(x + w, L, E)|^2 = 1 \end{aligned}$$

Thus, it is seen that the output at waveguide-4 gives AND logic operation. Table-4.5 shows all the input-output combinations for the all-optical AND logic operation realized with the basic SPTMI coupler.

4.2.3 All-optical OR gate

The OR gate is a digital circuit with two or more inputs and a single output such that, the output is obtained at logic 'high' if any or all of the inputs are at logic 'high' state. Table-4.6 summarizes all the input-output possibilities of a 2-input OR logic gate. Basically, this boolean function gives a logic '1' if any

Table 4.5: Truth table of all-optical AND gate implemented with SPTMI coupler

Control	**Inputs**		**Output**
P_1	E	P_2	P_4
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

one or both the inputs are at logic '1' state (combinations (0,1),(1,0) and (1,1)) and the output is at logic '0' only when both the inputs are at logic '0' state (combination (0,0)). In boolean equation form, the OR logic operation is denoted as $Y = A + B$.

Table 4.6: Truth table for a basic OR gate

Inputs		**Output**
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	1

The OR logic operations can be realized by using optical pulse of energy $E = 16.4pJ$ applied in cladding region as one input signal and optical power launched into input waveguide-2 (P_2) as the other input signal and by using the power launched into waveguide-1 (P_1) as control signal. The output for OR logic operation are obtained at output waveguide-3 (P_3). Fig-4.4 illustrates the various input-output combinations for the SPTMI based all-optical OR logic gate. The basic principle for implementation of OR logic operation in SPTMI device is explained by using $P_1 = 1$ as control signal. There are four states of truth table of OR gate, as given below-

- **Case 1:** E='0', P_2='0'
  When no optical pulse is applied at the cladding region ($E = 0$ and $\Delta\Phi_T(0) = \pi$) and no power is applied into waveguide-2 ($P_2 = 0$), power

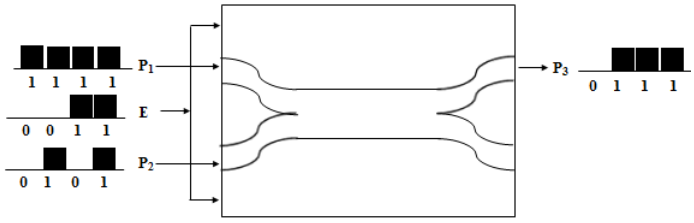


Figure 4.4: Implementation of OR logic operation using SPTMI coupler

at waveguide-1 is transferred to waveguide-4 due to cross state coupling of the device and no power will be obtained at waveguide-3. The power at the output waveguides are obtained as

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 0 \\ P_4 &= |H_4(x + w, L, E)|^2 = 1 \end{aligned}$$

- **Case 2:** E='0', P_2='1'
  When input power is incident on waveguide-2 ($P_2 = 1$) and no optical pulse is applied at cladding ($E = 0$ and $\Delta\Phi_T(0) = \pi$), power at waveguide-1 is transferred to waveguide-4 and power at waveguide-2 is transferred to waveguide-3 due to cross state coupling of the device. The power at the output waveguides are obtained as

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 1 \\ P_4 &= |H_4(x + w, L, E)|^2 = 1 \end{aligned}$$

- **Case 3:** E='1', P_2='0'
  When optical pulse of energy $E = 16.4pJ$ is applied in cladding region, the cross state coupling of the device changes to bar state coupling ($\Delta\Phi_T(E) = 2\pi$). Even if no signal is incident into waveguide-2 ($P_2 = 0$), the power in waveguide-1 is transferred to waveguide-3 due to bar state coupling and power at the output waveguides are obtained as

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 1 \\ P_4 &= |H_4(x + w, L, E)|^2 = 0 \end{aligned}$$

- **Case 4:** E='1', P_2='1'
  When optical pulse of energy $E = 16.4pJ$ is applied in cladding region, the cross state coupling of the device changes to bar state coupling

($\Delta\Phi_T(E) = 2\pi$). When signal power is incident at waveguide-2, due to bar state coupling of the device, power in waveguide-1 is transferred to waveguide-3 and power in waveguide-2 is transferred to waveguide-4. Thus,

$$\begin{aligned} P_3 &= |H_3(x, L, E)|^2 = 1 \\ P_4 &= |H_4(x + w, L, E)|^2 = 1 \end{aligned}$$

Thus, the output of waveguide-3 in the proposed SPTMI coupler shows characteristics of OR logic gate. The various input-output combinations for the all-optical OR logic gate implemented with the SPTMI coupler are summarized in Table-4.7.

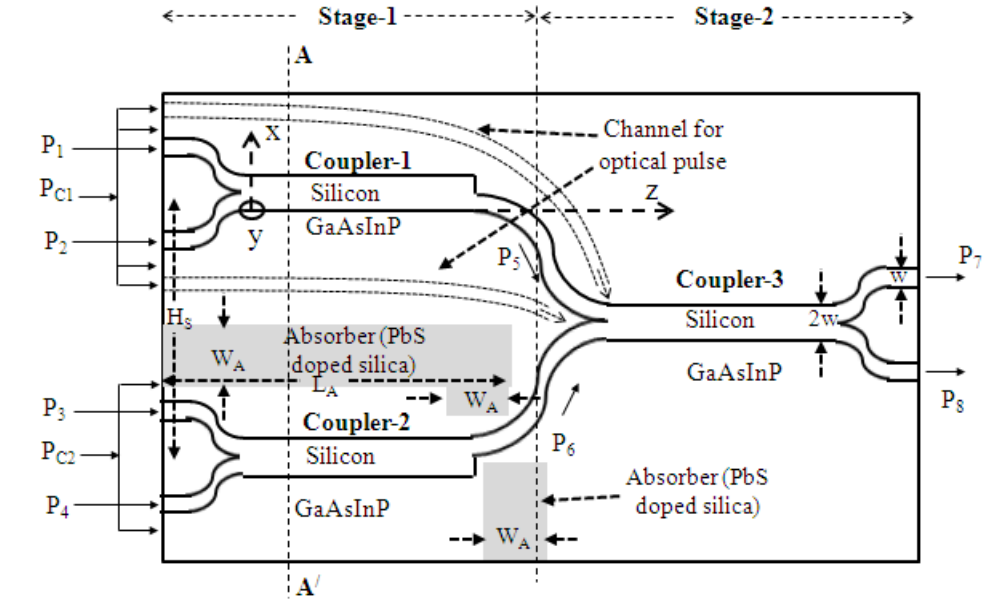
Table 4.7: Truth table of all-optical OR gate implemented with SPTMI coupler

Control	**Inputs**		**Output**
P_1	E	P_2	P_3
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

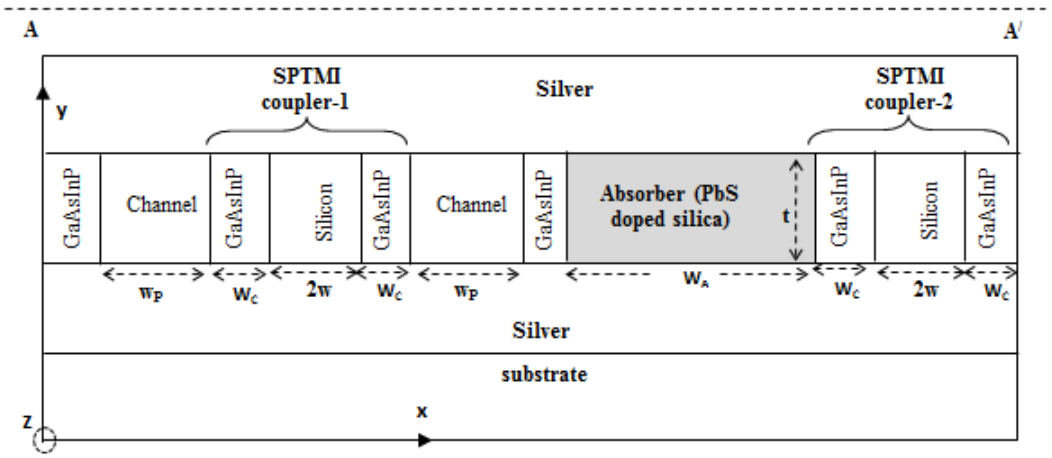
4.3 Demonstration of all-optical universal logic gates

NOR and NAND logic gates are known as the universal logic gates. All the logic operations such as NOT, AND, OR etc can be implemented by using repetition of only NOR gate or only NAND gate. Logic NAND and NOR operations can be realized simultaneously by cascading three basic SPTMI devices discussed in the preceding chapter. Fig-4.5 shows two dimensional (2D) schematic view of the cascaded SPTMI waveguide for NOR and NAND logic operations.

For implementation of all-optical NOR and NAND logic gates using the proposed cascaded structure, the input powers P_1 and P_4 launched into the input access waveguides are used as control signals, whereas optical pulse of energy E and width T_P applied at the claddings of coupler-1(P_{C1}) and coupler-2 (P_{C2}) of stage-1 are taken as the input signals. The input access waveguide-2 (P_2)



(a) Top view



(b) Cross sectional view along the line AA/

Figure 4.5: Schematic view of cascaded SPTMI device for implementation of logic operations.

and access waveguide-3 (P_3) are not used. The field at the access waveguide-5, access waveguide-6, access waveguide-7 and access waveguide-8 can be written as $H_5(L_1, E)$, $H_6(L_2, E)$, $H_7(L_3, E)$ and $H_8(L_3, E)$ respectively where, L_1, L_2, and L_3 are the length of two-mode coupling region of coupler-1 and coupler-2 for stage-1 and coupler-3 for stage-2 respectively. $P_5 = |H_5(L_1, E)|^2$ and $P_6 = |H_6(L_2, E)|^2$ are output powers of coupler-1 and coupler-2 respectively, which act as the inputs for the third SPTMI coupler of stage-2. To prevent the optical pulse in GaAsInP cladding of coupler-2 from entering the cladding of other couplers, GaAsInP cladding of coupler-2 has been isolated from the other couplers by

using PbS nanoparticle doped silica glass as an absorber [130]. The cladding signal for coupler-3 of stage-2 is same as the cladding signal for coupler-1, i.e., P_{C1}. The output for NOR and NAND logic gates are obtained at output access waveguide-7 ($P_7 = |H_7(L_3, E)|^2$) and access waveguide-8 ($P_8 = |H_8(L_3, E)|^2$) respectively.

The length of two-mode region for the SPTMI waveguide couplers in stage-1 and stage-2 are taken as $L_1 = L_2 = L_3 = L = 92.35\mu m$ for cross state coupling. Thus, the total length of device for implementation of NOR and NAND gates can be estimated as $L_{cascaded} = 2 \times 92.35 + 4 \times 24.97 = 284.58\mu m$ where, $L_T = 24.97\mu m$ is the transition length for access waveguides. The length and width of PbS doped silica [130] used between first and second SPTMI couplers to absorb optical pulse of wavelength $1.5\mu m$ [124] are given as $L_A = 123\mu m$ and $W_A = 5\mu m$, as shown in Fig-4.5. Channels of width $w_P = 1.8\mu m$ and thickness $t = 5.0\mu m$ are used to apply optical pulse to the cladding of coupler-3 of stage-2, so that the energy of applied optical pulse is same as that applied at the cladding of coupler-1 ie, P_{C1}. Table-4.8 shows values of designed parameters of the cascaded SPTMI structure shown in Fig-4.5 for universal logic gate operations.

Table 4.8: Device parameters for cascaded SPTMI structure for logic operations

Device parameters	**Values**
Core (silicon) refractive index (n_1)	3.5
Metal (silver) cladding refractive index (n_m)	$0.394 + 8.2j$
Side (GaAsInP) cladding refractive index ($n_2(0)$)	3.17
Side (GaAsInP) cladding nonlinear coefficient (n_{nl})	$-2 \times 10^{-3}\mu m^2 W^{-1}$
Wavelength of operation (λ)	$1.33\mu m$
Core width ($2w$)	$0.48\mu m$
Core thickness (t)	$5.0\mu m$
Energy of pulse applied (E)	$16.4pJ$
Full width at half maximum of pulse (T_P)	$1ps$
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Table 4.8 – continued from previous page

Device parameters	Values
Coupling length for coupler-1 (L_1)	$92.35\mu m$
Coupling length for coupler-2 (L_2)	$92.35\mu m$
Coupling length for coupler-3 (L_3)	$92.35\mu m$
Device length	$284.58\mu m$
Bending radius of access waveguides (R)	$39\mu m$
Transition length of access waveguides (L_T)	$24.97\mu m$
Bending loss	$0.1dB$
Separation between coupler-1 and coupler-2 (H_S)	$16\mu m$
Area of GaAsInP cladding for each coupler (A_{clad})	$2.0\mu m^2$
Total area of metal cladding	$90\mu m^2$
Width of channels used to apply optical pulse to cladding area of coupler-3 (w_P)	$1.8\mu m$
Length and width of PbS doped silica (absorber)	$L_A = 123\mu m$ $W_A = 5\mu m$

4.3.1 All-optical NOR gate

Basically, the NOR logic operation gives a logic '0' if any one or both the inputs are at logic '1' state (combinations (0,1),(1,0) and (1,1)) and the output is at logic '1' only when both the inputs are at logic '0' state (combination (0,0)). In boolean equation form, the NOR logic operation is denoted as $Y = \overline{A + B}$. The possible input-output combinations of a NOR logic gate are given in Table-4.9.

All-optical NOR logic gate is realized by using input powers P_1 and P_4 launched into the input access waveguides as control signals, and optical pulse of

Table 4.9: Truth table for a basic NOR gate

Inputs		**Output**
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	0

energy E and width T_P applied at the claddings of coupler-1 (P_{C1}) and coupler-2 (P_{C2}) of stage-1 as the input signals. For this configuration, P_5 and P_6 gives the NOT gate output for coupler-1 and coupler-2 respectively. P_5 and P_6 act as the inputs for the third SPTMI coupler and the optical pulse at cladding of coupler-3 is P_{C1}. The output for NOR logic gate are obtained at output port P_7. The various input and output logic states for implementation of all-optical NOR logic gate with the cascaded SPTMI structure shown in Fig-4.5 are given in Table-4.10. The various input-output combinations for the SPTMI based all-optical NOR logic gate are illustrated in Fig-4.6. There are four cases in which $P_1 = 1$ and $P_4 = 1$ are used as control signals and P_{C1} and P_{C2} are used as input-1 and input-2 respectively.

Table 4.10: Implementation of NOR gate with cascaded SPTMI coupler

Stage-1 (coupler-1)			Stage-1 (coupler-2)			Stage-2 (coupler-3)			
P_1 (Control)	P_2	P_{C1} (input 1)	P_3	P_4 (Control)	P_{C2} (Input 2)	P_5	P_6	P_{C1} (Input 1)	P_7 (Output)
1	-	0	-	1	0	1	1	0	1
1	-	1	-	1	0	0	1	1	0
1	-	0	-	1	1	1	0	0	0
1	-	1	-	1	1	0	0	1	0

- **Case 1:** P_{C1}='0', P_{C1}='0'
  When no optical pulse is applied at the cladding regions of both coupler-1 and coupler-2 (combination (0,0)), both the couplers are in cross state coupling ($\Delta\Phi_T(0) = \pi$) and P_5 and P_6 are high due to transfer of power

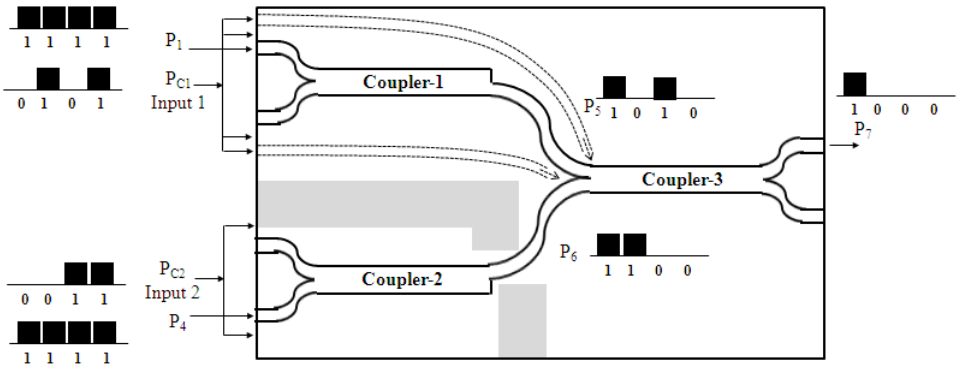

Figure 4.6: Implementation of NOR logic operation using SPTMI coupler

from access waveguide-1 and waveguide-4 respectively and are given as

$$\begin{aligned} P_5 &= |H_5(L_1, E)|^2 = 1 \\ P_6 &= |H_6(L_2, E)|^2 = 1 \end{aligned}$$

As P_{C1} is low, coupler-3 is in cross state ($\Delta\Phi_T(0) = \pi$) and the power at P_6 is transferred to P_7 (output logic '1') i.e.,

$$P_7 = |H_7(L_3, E)|^2 = 1$$

- **Case 2:** P_{C1}='1', P_{C1}='0'
  When an optical pulse of energy $E = 16.4pJ$ is applied at the cladding of coupler-1 ($P_{C1} = 1$) but no optical pulse is applied at the cladding region of coupler-2 ($P_{C2} = 0$), coupler-1 shows bar state coupling ($\Delta\Phi_T(E) = 2\pi$) and coupler-2 shows cross state coupling ($\Delta\Phi_T(0) = \pi$). Thus, no power is coupled to P_5, whereas P_6 is at logic '1' due to transfer of power from access waveguide-4. This can be written as

$$\begin{aligned} P_5 &= |H_5(L_1, E)|^2 = 0 \\ P_6 &= |H_6(L_2, E)|^2 = 1 \end{aligned}$$

Since P_{C1} is 'high', the cross state coupling of coupler-3 changes to bar state coupling ($\Delta\Phi_T(E) = 2\pi$) and no power is obtained at P_7 due to absence of power at P_5 (output logic '0') i.e.,

$$P_7 = |H_7(L_3, E)|^2 = 0$$

- **Case 3:** P_{C1}='0', P_{C1}='1'
  When no optical pulse is applied at the cladding region of coupler-1 ($P_{C1} = 0$), and an optical pulse of energy $E = 16.4pJ$ is applied at the cladding of coupler-2 ($P_{C2} = 1$), coupler-1 shows cross state coupling ($\Delta\Phi_T(0) = \pi$) and coupler-2 shows bar state coupling ($\Delta\Phi_T(E) = 2\pi$). Thus, P_5 is at logic '1' due to transfer of power from access waveguide-1 and P_6 is at logic '0' as no power is coupled to P_6 which can be written as

$$\begin{aligned} P_5 &= |H_5(L_1, E)|^2 = 1 \\ P_6 &= |H_6(L_2, E)|^2 = 0 \end{aligned}$$

  Since P_{C1} is 'low', stage-3 shows cross state coupling ($\Delta\Phi_T(0) = \pi$) and no power is obtained at P_7 due to absence of power at P_6 (output logic '0') i.e.,

$$P_7 = |H_7(L_3, E)|^2 = 0$$

- **Case 4:** P_{C1}='1', P_{C1}='1'
  When optical pulse of energy $E = 16.4pJ$ is applied at the claddings of both coupler-1 ($P_{C1} = 1$) and coupler-2 ($P_{C2} = 1$), the cross state coupling of both changes to bar state coupling ($\Delta\Phi_T(E) = 2\pi$) and there is no power coupled to P_5 and P_6 i.e.,

$$\begin{aligned} P_5 &= |H_5(L_1, E)|^2 = 0 \\ P_6 &= |H_6(L_2, E)|^2 = 0 \end{aligned}$$

  Because there is no input power to coupler-3, we have

$$P_7 = |H_7(L_3, E)|^2 = 0$$

  The output is obtained at logic '0'.

Thus, considering the output at P_7, all-optical NOR logic operation is realized.

4.3.2 All-optical NAND gate

The NAND logic operation gives a logic '0' only when both the two inputs are 'high' (combination (1,1)). If any one of the input signals is at logic '0', the

output signal is obtained at logic '1' state (combinations (0,0), (0,1) and (1,0)). This logic operation is denoted as $Y = \overline{AB}$ in boolean equation form. Table-4.11 shows the truth table for the operation of a 2 input NAND logic gate.

Table 4.11: Truth table for a basic NAND gate

Inputs		**Output**
A	**B**	**Y**
0	0	1
0	1	1
1	0	1
1	1	0

All-optical NAND gate is realized by using input powers P_1 and P_4 launched into input access waveguides as control signals, and optical pulse of energy E and width T_P applied at the claddings of coupler-1 (P_{C1}) and coupler-2 (P_{C2}) as the input signals. P_5 and P_6 are the output powers for coupler-1 and coupler-2 respectively (which show characteristics of NOT logic operation) and act as the inputs for the third SPTMI coupler. The optical pulse at cladding of coupler-3 is the same as that applied at the cladding of first coupler (P_{C1}). The output for NAND logic gate are obtained at output port P_8. The various input and output logic states for implementation of all-optical NAND logic gate with the cascaded SPTMI structure shown in Fig-4.5 are given in Table-4.12. The

Table 4.12: Implementation of NAND gate with cascaded SPTMI coupler

Stage-1 (coupler-1)			Stage-1 (coupler-2)			Stage-2 (coupler-3)			
P_1 (Control)	P_2	P_{C1} (input 1)	P_3	P_4 (Control)	P_{C2} (Input 2)	P_5	P_6	P_{C1} (Input 1)	P_8 (Output)
1	-	0	-	1	0	1	1	0	1
1	-	1	-	1	0	0	1	1	1
1	-	0	-	1	1	1	0	0	1
1	-	1	-	1	1	0	0	1	0

various input-output combinations for the SPTMI based all-optical NAND logic gate are depicted in Fig-4.7. There are four states in which P_{C1} and P_{C2} are

input-1 and input-2 respectively, whereas $P_1 = 1$ and $P_4 = 1$ are used as control signals.

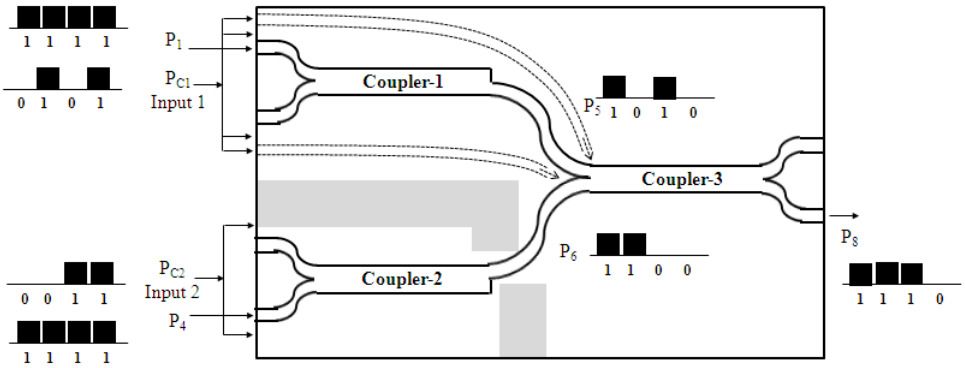

Figure 4.7: Implementation of NAND logic operation using SPTMI coupler

- **Case 1:** P_{C1}='0', P_{C1}='0'
  When no optical pulse is applied at the cladding regions of both coupler-1 and coupler-2 (combination (0,0)), phase difference for both couplers is given by $\Delta\Phi_T(0) = \pi$ and both the couplers are in cross state coupling. P_5 and P_6 are high due to transfer of power from access waveguide-1 and waveguide-4 respectively and can be expressed as

$$\begin{aligned} P_5 &= |H_5(L_1, E)|^2 = 1 \\ P_6 &= |H_6(L_2, E)|^2 = 1 \end{aligned}$$

  As P_{C1} is low, coupler-3 is in cross state ($\Delta\Phi_T(0) = \pi$) and the power at P_5 is transferred to P_8 (output logic '1') i.e.,

$$P_8 = |H_8(L_3, E)|^2 = 1$$

- **Case 2:** P_{C1}='1', P_{C1}='0'
  When an optical pulse of energy $E = 16.4pJ$ is applied at the cladding of coupler-1 ($P_{C1} = 1$) but no optical pulse is applied at the cladding region of coupler-2 ($P_{C2} = 0$), coupler-1 shows bar state coupling ($\Delta\Phi_T(E) = 2\pi$) and coupler-2 shows cross state coupling ($\Delta\Phi_T(0) = \pi$) . Thus, no power is coupled to P_5, whereas P_6 is at logic '1' due to transfer of power from access waveguide-4. This can be expressed as

$$\begin{aligned} P_5 &= |H_5(L_1, E)|^2 = 0 \\ P_6 &= |H_6(L_2, E)|^2 = 1 \end{aligned}$$

Since P_{C1} is 'high', the cross state coupling of coupler-3 changes to bar state coupling ($\Delta\Phi_T(E) = 2\pi$) and the power at P_6 is transferred to P_8 (output logic '1') i.e.,

$$P_8 = |H_8(L_3, E)|^2 = 1$$

- **Case 3:** P_{C1}='0', P_{C1}='1'
  When no optical pulse is applied at the cladding region of coupler-1 ($P_{C1} = 0$), and an optical pulse of energy $E = 16.4pJ$ is applied at the cladding of coupler-2 ($P_{C2} = 1$), coupler-1 shows cross state coupling ($\Delta\Phi_T(0) = \pi$) and coupler-2 shows bar state coupling ($\Delta\Phi_T(E) = 2\pi$) . Thus, P_5 is at at logic '1' due to transfer of power from access waveguide-1 and P_6 is at logic '0' as no power is coupled to P_6 i.e.,

$$\begin{aligned} P_5 &= |H_5(L_1, E)|^2 = 1 \\ P_6 &= |H_6(L_2, E)|^2 = 0 \end{aligned}$$

  Since P_{C1} is 'low', coupler-3 shows cross state coupling ($\Delta\Phi_T(0) = \pi$) and the power at P_5 is transferred to P_8 (output logic '1') which can be given by

$$P_8 = |H_8(L_3, E)|^2 = 1$$

- **Case 4:** P_{C1}='1', P_{C1}='1'
  When optical pulse of energy $E = 16.4pJ$ is applied at the claddings of both coupler-1 ($P_{C1} = 1$) and coupler-2 ($P_{C2} = 1$), the cross state coupling of both changes to bar state coupling ($\Delta\Phi_T(E) = 2\pi$) and there is no power coupled to P_5 and P_6. Thus, we have

$$\begin{aligned} P_5 &= |H_5(L_1, E)|^2 = 0 \\ P_6 &= |H_6(L_2, E)|^2 = 0 \end{aligned}$$

  Because there is no input power to coupler-3, the output is obtained at logic '0' i.e.,

$$P_8 = |H_8(L_3, E)|^2 = 0$$

Thus, considering the output at P_8, all-optical NAND logic operation is realized.

4.4 Demonstration of all-optical XOR logic gate

The XOR gate is one of the main building block for a wide range of signal processing functions [131]. Basically, this boolean function gives a logic '0' if the two inputs are same (combinations (0,0) and (1,1). On the other hand, if the two inputs being compared are different, the output signal is at logic '1' (combinations (0,1) and (1,0)). In boolean equation form, the XOR logic operation is denoted as $Y = A\overline{B} + \overline{A}B$. All the possible input-output combinations of an XOR logic gate are summarized in Table-4.13.

Table 4.13: Truth table for a basic XOR gate

Inputs		**Output**
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

All-optical XOR logic operation can be implemented using the same structure shown in Fig-4.5, used for implementation of all-optical NOR and NAND logic gates. For implementation of XOR gates, the input powers P_2 and P_4 launched into the input access waveguides 2 and 4 are used as control signals, whereas optical pulse of energy E and width T_P applied at the claddings of coupler-1 (P_{C1}) and coupler-2 (P_{C2}) of stage-1 are taken as the input signals. The logic state at input access waveguides-1 (P_1) is kept same as that of the cladding signal of coupler-2 (P_{C2}), whereas input access waveguide-3 (P_3) is not used. $P_5 = |H_5(L_1, E)|^2$ and $P_6 = |H_6(L_2, E)|^2$ are output powers of coupler-1 and coupler-2 which act as the inputs for the third SPTMI coupler. GaAsInP cladding of coupler-2 has been isolated from the cladding of the other coupler by a light absorbing material (PbS doped silica) such that, cladding signal for coupler-3 is same as the cladding signal for coupler-1 (P_{C1}). The output of the XOR logic operation can be obtained as $P_8 = |H_8(L_3, E)|^2$. The design parameters for the implementation of all-optical XOR logic gate with the cascaded SPTMI structure can be obtained from Table-4.8. Table-4.14 gives the various logic states for implementation of all-optical XOR logic gate with the proposed structure.

Table 4.14: Implementation of XOR gate with cascaded SPTMI coupler

Stage-1 (coupler-1)			Stage-1 (coupler-2)			Stage-2 (coupler-3)			
P_1 (Input 2)	P_2 (Control)	P_{C1} (input 1)	P_3	P_4 (Control)	P_{C2} (Input 2)	P_5	P_6	P_{C1} (Input 1)	P_8 (Output)
0	1	0	-	1	0	0	1	0	0
0	1	1	-	1	0	1	1	1	1
1	1	0	-	1	1	1	0	0	1
1	1	1	-	1	1	1	0	1	0

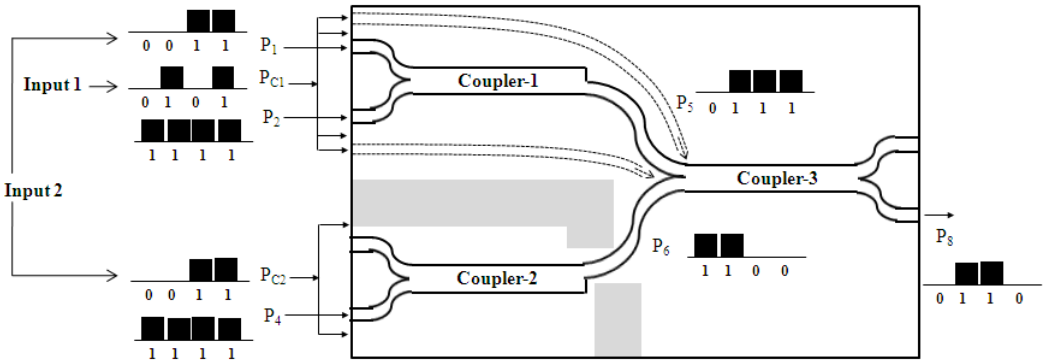

Figure 4.8: Implementation of XOR logic operation using SPTMI coupler

Fig-4.8 illustrates the various input-output combinations for the SPTMI based all-optical XOR logic gate. There are four cases in which $P_2 = 1$ and $P_4 = 1$ are used as control signals, whereas P_{C1} and $P_{C2} = P_1$ are input-1 and input-2 respectively.

- **Case 1:** P_{C1}='0', P_{C1}='0'
  When no optical pulse is applied at the cladding regions of both coupler-1 and coupler-2 (combination (0,0)), both the couplers show cross state coupling ($\Delta\Phi_T(0) = \pi$). Thus, P_5 is 'low' because no power is transferred from P_1 to P_5 and P_6 is 'high' as the power at P_4 is transferred to P_6. This is given as

$$P_5 = |H_5(L_1, E)|^2 = 0$$
$$P_6 = |H_6(L_2, E)|^2 = 1$$

  As P_{C1} is 'low', coupler-3 is in cross state ($\Delta\Phi_T(0) = \pi$) and no power is

transferred to P_8 as the power at P_5 is zero (output logic '0') i.e.,

$$P_8 = |H_8(L_3, E)|^2 = 0$$

- **Case 2:** P_{C1}='1', P_{C1}='0'
  When an optical pulse of energy $E = 16.4pJ$ is applied at the cladding of coupler-1 ($P_{C1} = 1$) but no optical pulse is applied at the cladding region of coupler-2 ($P_{C2} = 0$), the cross state coupling of coupler-1 changes to bar state ($\Delta\Phi_T(E) = 2\pi$), whereas coupler-2 is in cross state ($\Delta\Phi_T(0) = \pi$). Thus, the power at P_2 is transferred to P_5 and the power at P_4 is transferred to P_6. This can be expressed as

$$P_5 = |H_5(L_1, E)|^2 = 1$$
$$P_6 = |H_6(L_2, E)|^2 = 1$$

  Since P_{C1} is 'high', the cross state coupling of coupler-3 changes to bar state coupling ($\Delta\Phi_T(E) = 2\pi$) and the power at P_6 is transferred to P_8 (output logic '1') which is given by

$$P_8 = |H_8(L_3, E)|^2 = 1$$

- **Case 3:** P_{C1}='0', P_{C1}='1'
  When no optical pulse is applied at the cladding region of coupler-1 ($P_{C1} = 0$), and an optical pulse of energy $E = 16.4pJ$ is applied at the cladding of coupler-2 ($P_{C2} = 1$), coupler-1 shows cross state coupling ($\Delta\Phi_T(0) = \pi$), whereas the cross state coupling of coupler-2 changes to bar state coupling ($\Delta\Phi_T(E) = 2\pi$). Thus, the power at P_1 is transferred to P_5 and no power is obtained P_6. This can be expressed as

$$P_5 = |H_5(L_1, E)|^2 = 1$$
$$P_6 = |H_6(L_2, E)|^2 = 0$$

  Since P_{C1} is 'low', due to cross state coupling of coupler-3 ($\Delta\Phi_T(0) = \pi$), the power at P_5 is transferred to P_8 (output logic '1') which is given by

$$P_8 = |H_8(L_3, E)|^2 = 1$$

- **Case 4:** P_{C1}='1', P_{C1}='1'
  When optical pulse of energy $E = 16.4pJ$ is applied at the claddings of both coupler-1 ($P_{C1} = 1$) and coupler-2 ($P_{C2} = 1$), the cross state coupling of the input couplers changes to bar state coupling ($\Delta\Phi_T(E) = 2\pi$). The power at P_2 is transferred to P_5 and no power is obtained at P_6 due to absence of power at P_3 i.e.,

$$\begin{aligned} P_5 &= |H_5(L_1, E)|^2 = 1 \\ P_6 &= |H_6(L_2, E)|^2 = 0 \end{aligned}$$

  As P_{C1} is 'high', coupler-3 shows bar state coupling ($\Delta\Phi_T(E) = 2\pi$) and no power is transferred to P_8 as the power at P_6 is zero (output logic '0'). Thus, we have

$$P_8 = |H_8(L_3, E)|^2 = 0$$

So, the output power at P_8 shows characteristics of XOR logic gate.

4.5 Comparison of the proposed SPTMI based logic gates with previous works

We have implemented optical pulse controlled fundamental NOT, OR and AND logic operations using the basic surface plasmonic two-mode interference (SPTMI) coupler discussed in chapter 3. The device parameters for the proposed SPTMI coupler based all-optical logic gates can be obtained from Table-4.1. The length of the coupling region for implementation of fundamental logic gates is $92.35\mu m$ which is about ~ 53.9 times less than that for all-optical OR and NOT gates based on SiGe/Si MMI coupler [69] and ~ 8.4 times less than that for AND and NOT gates based on OTMI coupler [67] reported by previous researchers. Total length of the SPTMI coupler for fundamental logic gate operations is obtained as $\sim 142.29\mu m$ which is about ~ 45.7 times less than that for SiGe/Si MMI coupler [69] based logic gates and ~ 5.9 times less than that for OTMI coupler [67] based gates reported previously. The operating time of gate is almost as same as recovery time of nonlinearity in refractive index of GaAsInP which is of the order of picoseconds. The power consumption is $16.4pJ$ which is close to optical pulse energy required for change of coupling states and is about ~ 1.65 times less than that for AND and NOT gates based on OTMI coupler [67].

All the three fundamental logic gates can be implemented using the same basic SPTMI device unlike some previous works which could implement only few [67–69] or single logic functions [72, 81, 82, 85]. Implementation of different logic functions are controlled by the presence or absence of optical pulse applied at the nonlinear cladding and power at the input access waveguides, whereas in previously reported works, different logic functions are determined by the intensity of the output [26] or input [83] signals which may lead to difficulty in cascading of gates necessary for large scale integration of integrated optic devices. In this work, optically-controlled NOR, NAND and XOR operations have been shown by cascading three basic SPTMI coupler. Moreover, the output state depends on the phase difference induced between the propagating modes during propagation along coupling region, but not on the phase difference of input signals. As such, the designed gates are free from any instability that can be caused by difficulty in precise control of input phase difference, as seen in previously reported works [27,79,80,84]. The advantages of the SPTMI waveguide coupler based all-optical logic gates over previous works are summarized in Table-4.15.

Table 4.15: Comparison of implemented logic gates with previous works

Parameter	**Proposed device**	**Comparison to previous work**
Coupling length	$92.35\mu m$	$778.5\mu m$ (gates using OTMI coupler), smaller by $\sim$ 8.4 times [67]
		$4980\mu m$ (Gates using SiGe/Si based MMI coupler), smaller by $\sim$ 53.6 times [69]
Device length	$142.29\mu m$	$834.1\mu m$ (gates using OTMI coupler), smaller by $\sim$ 5.9 times [67]
		$5964\mu m$ (Gates using SiGe/Si based MMI coupler), smaller by $\sim$ 45.7 times [69]

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Table 4.15 – continued from previous page

Parameter	Proposed device	Comparison to previous work
Power consumption	$16.4pJ$	$27pJ$ (gates using OTMI coupler), smaller by ~ 1.65 times [67]
Control over logic operation	By presence or absence of power at input ports	By varying intensity of output signal (Interference in Y-branch) [26]
		By varying energy of input optical pulse (nonlinear ring resonator) [83]
Gates realized by using basic device	NOT, AND and OR (three gates)	NOT and AND logic gates (OTMI coupler), 2 gates [67]
		NOT and OR logic gates (SiGe/Si based MMI coupler), 2 gates [69]
		NOT and AND logic gates (MMI coupler with partially nonlinear region), 2 gates [68]
		OR logic gate (plasmonic waveguide with metallic nanorods), single logic function [85]
		NOT logic gate (microring MIM plasmonic waveguide), single logic function [82]
		OR logic gate (ferroelectric hybrid plasmonic waveguide), single logic function [81]

Continued on next page

Table 4.15 – continued from previous page

Parameter	Proposed device	Comparison to previous work
		AND logic gate (nonlinear photonic crystal), single logic function [72]

4.6 Conclusion

In this chapter, applications of the basic surface plasmonic TMI waveguide coupler in all-optical logic operations have been shown. All-optical fundamental logic gates are implemented by using the 2×2 SPTMI coupler. By using the power launched in one of the input access waveguides as control signal and optical pulse energy applied in cladding region and optical power launched into the other access waveguide as input signals, all-optical basic NOT, AND and OR logic gates have been realized. The output states of logic gates are obtained at either one of the output access waveguides. The length of the coupling region for implementation of fundamental logic gates is $92.35\mu m$ which is about ~ 53.9 times [69] and ~ 8.4 times [67] less than that in previously reported works for realization of all-optical logic operations. Total length of the SPTMI coupler for fundamental logic gate operations is obtained as $\sim 142.29\mu m$ which is about ~ 45.7 times [69] less and ~ 5.9 times [67] less than previous works for all-optical logic gates. The operating time of gate is of the order of picoseconds and the power consumption is $16.4pJ$ which is about ~ 1.65 times less than previously reported gates [67]. Implementation of different logic functions are controlled by the presence or absence of optical pulse applied at the nonlinear cladding and power at the input access waveguides.

We have proposed new structure for universal gates cascading two stages of coupler and demonstrated NAND and NOR gate operation with same structure by considering proper control signals. We have also demonstrated XOR operation by using same new structure having proper control signals. Since the output power in these proposed all-optical logic gates does not depend on the phase difference of input signals, the designed gates are free from any instability that can be caused by any unwanted variation of input phase difference.