Chapter 1

Introduction

1.1 Motivation

Precision and accuracy of current control led to the development of the concept of the transistors. The early approach for current control based on field effect principle was first patented by Julius Edgar Lilienfeld [1] in 1930 and by Oskar Heil [2] in 1935. During that period the device implementation was not possible due to certain limitations. With the invention of metal oxide semiconductor field effect transistor (MOSFET) [3] in 1960 the VLSI era started. In the last few decades, astounding advancement in the field of VLSI has been seen with introduction of many new devices and device structures. VLSI devices are reaching towards scaling limit due to on-going downscaling. The limitations observed in bulk MOSFET at very small dimension led to the invention of several new devices such as the SOI devices, strained Si devices, device with high-k dielectric etc [4-9]. With the invention of new device structures it is possible to scale down the devices further into the nanometer regime. However, the presence of the junction in these devices imposes few other limitations in scaling down beyond a certain point in nanoscale regime. This is due to presence of a space charge region which is always associated with a junction. The necessity to overcome the limitations of junction, gave new dimension to the MOSFET technology, which results in the formulation of Junctionless FET or simply Junctionless Transistor or JLT. In 2009 J.P. Collinge and his associates successfully fabricated the first Junctionless Transistor (JLT) [10].

Compared to devices having junctions, JLT exhibits several advantages such as simpler fabrication process, superior I_{on}/I_{off} ratio, reduced Drain Induced Barrier Lowering (DIBL) and subthreshold slope resulting in extremely low leakage currents [10-27]. Moreover, it also exhibits better scalability as compared to conventional devices. It also has the advantage of less sensitivity to process parameters compared to conventional transistors. Despite of all these advantages, JLT suffers from few drawbacks such as- higher off-state current, carrier mobility degradation resulting from high doping concentration (Coulombic scattering). To tackle these drawbacks of JLT as well as to obtain a reasonably accurate and efficient model

and to provide more device structure choices regarding scaling limit for better designing of JLT, the objectives of this work have been set as follows.

1. Scale Length Determination of Some Non-Conventional Structures of JLT

2. Modelling Some parameters of JLT

    a) Depletion Width Modelling

    b) Threshold Voltage Modelling

    c) Potential Modelling

    d) Drain Current Modelling

3. Enhancement of Performance Parameters of JLT

    a) Off-state Leakage Current Reduction

    b) Carrier Mobility Enhancement

   c) Study of Extent of Corner Effect in JLT and a measure for reduction of corner effect.

Various methods have been adopted in the past to overcome these drawbacks such as-use of CNT based JLT etc. [28,29]. However, Si-based devices are more suitable for mass production by the semiconductor industries. Hence this work is focused on Si based JLT only.

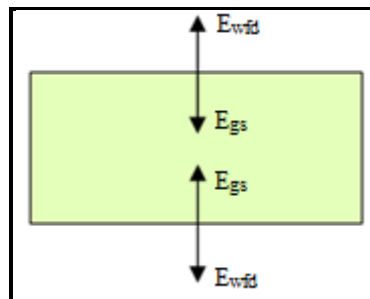**1.2 Introduction to Junctionless Transistor**

By definition, JLT is a MOSFET without any p-n junction having identical doping profile throughout the source, drain and channel [10-27] as shown in Fig. 1.1. For proper turn off of JLT the following conditions are necessary.

1. A high work function gate material which can create a large depletion region in the substrate under the gate.

2. The substrate thickness should be as small as possible so that the depletion region mentioned in point 1 covers the entire substrate under the gate.

JLT also requires a heavily doped channel to ensure an adequate amount of current flow when the device is turned on [17]. From the operation point of view JLT posses four regions namely, subthreshold, bulk current, flat band and accumulation mode as shown in Fig. 1.2, Fig. 1.3, Fig. 1.4 and Fig. 1.5 respectively.
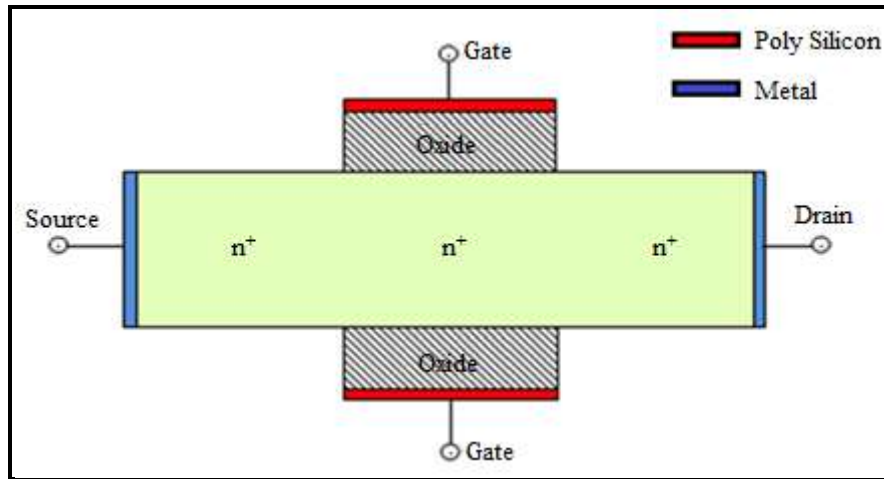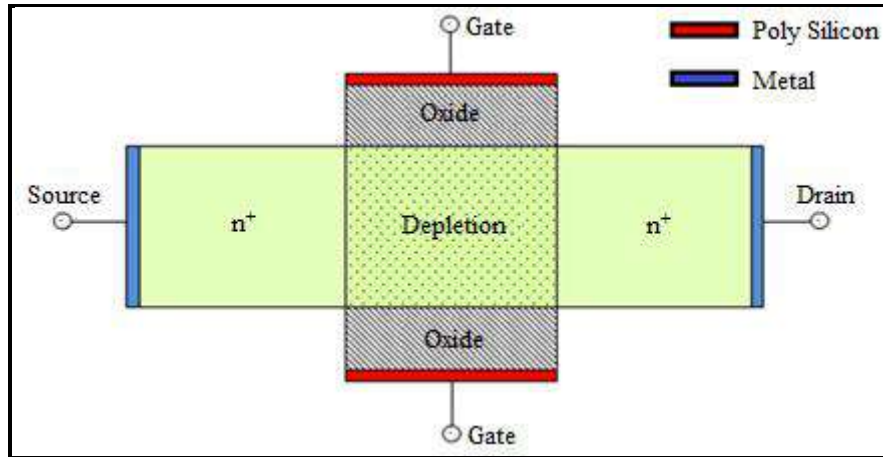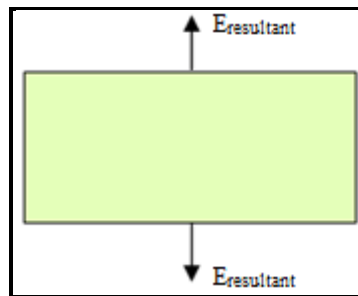

(a)

(b)

Fig. 1.1: (a) Schematic view of a Double-gate Junctionless Transistor (b) Direction of Electric fields due to work function difference (E_{wfd}) and applied gate voltage (E_{gs})

(a) Subthreshold mode


(a)

(b)

Fig. 1.2 : JLT in Subthreshold mode (a) Schematic view (b) Direction of resultant electric field ($E_{resultant}$)

Initially the channel region is fully depleted due to the work function difference between the gate and the body. The channel remains fully depleted until the applied gate voltage (V_{gs}) reaches a value called threshold voltage (V_{th}). The fully depleted channel blocks large voltage and consequently turn the device off. This region of operation, in which gate voltage is below the threshold value ($V_{gs} < V_{th}$), is called the subthreshold region [17].

(b) Bulk Current Mode
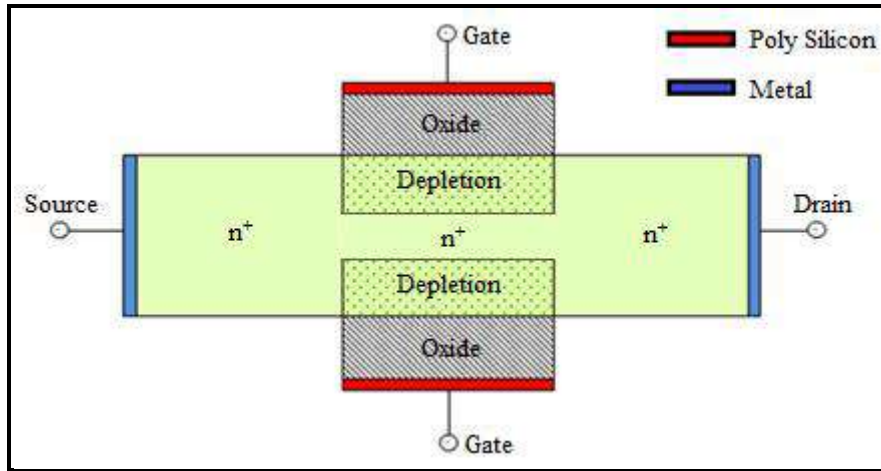

(a)
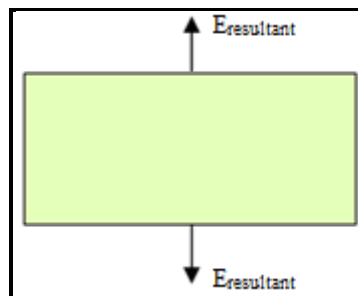
(b)

Fig. 1.3: JLT in Bulk Current Mode (a) Schematic view (b) Direction of resultant electric field ($E_{resultant}$)

The electric field due to applied gate voltage opposes the internal electric field induced by the work function difference between gate and substrate. As the gate voltage is increased beyond the threshold voltage ($V_{gs} > V_{th}$), the applied gate electric field is larger than the internal electric field. It results in a neutral semiconductor layer in the channel and JLT enters in partial depletion mode. The drain current starts flowing through the neutral region turning the device on. This region of operation is termed as bulk current region [17].

(c) Flat Band Mode
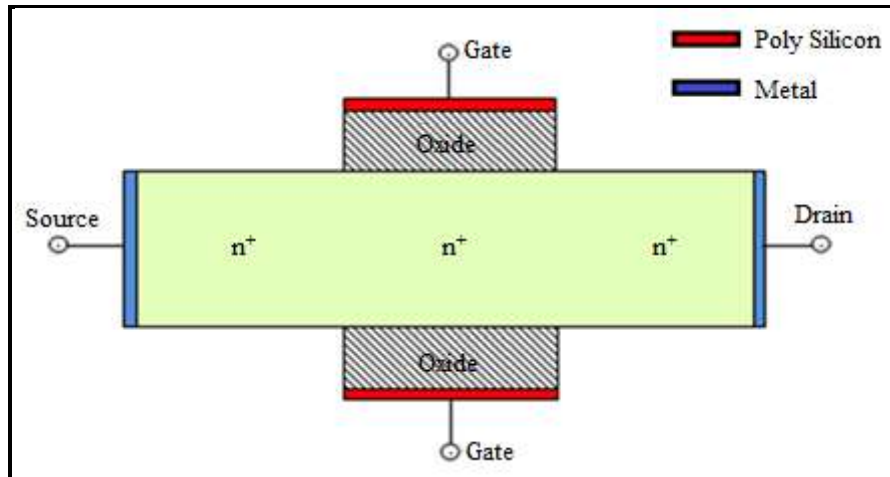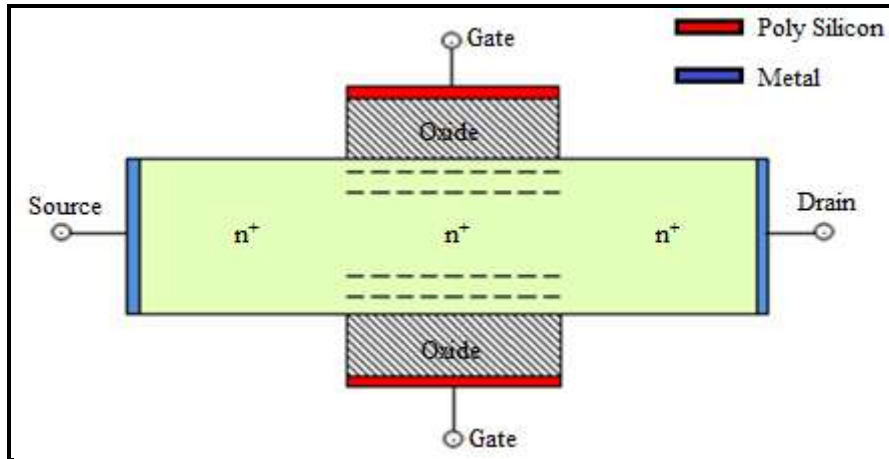

(a)
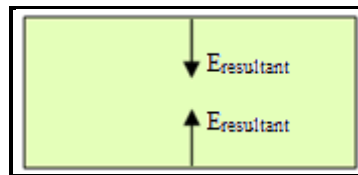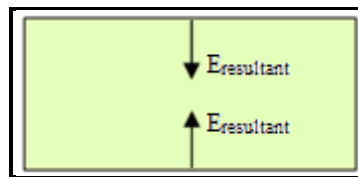

(b)

Fig. 1.4: JLT in Flat Band Mode (a) Schematic view (b) Direction of resultant electric field ($E_{resultant}$)

When the gate voltage reaches the flat band value ($V_{gs}=V_{fb}$), the depletion layer is completely removed creating a complete neutral channel. Maximum bulk current flows through the channel at this point. It is termed as the flat band region [17].

(d) Accumulation Mode

(a)

(b)

Fig. 1.5: JLT in Accumulation Mode (a) Schematic view (b) Direction of resultant electric field ($E_{resultant}$)

If the gate voltage is increased farther ($V_{gs}>V_{fb}$) negative charges are accumulated near the surfaces of the channel. However, bulk charges causes the major portion of the current to flow through the channel, as the surface current due to accumulated charges flow at a gate voltage much larger than the threshold voltage. The region is called accumulation region [17]. The transfer characteristics of a JLT showing different operating region is shown in Fig. 1.6.
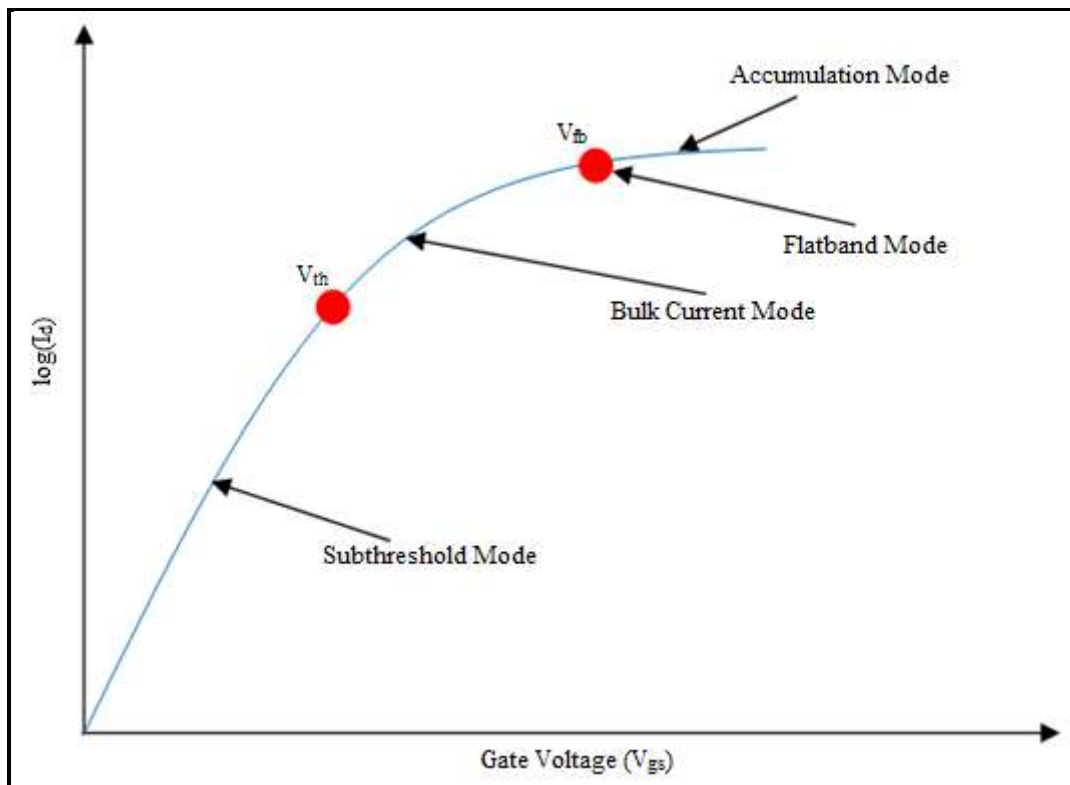
Fig. 1.6: Transfer characteristics of a JLT showing different modes of operation[17]

1.3 Organization of The Thesis

The thesis is organized as follows:

Chapter 2   Literature Review

Detailed literature review on MOSFET technologies with special emphasis on JLT has been presented in a historical and chronological manner in this chapter.

Chapter3   Scale Length Determination of Some Non Conventional Structures of JLT

Scale length is a theoretical parameter that is obtained by solving Poisson's equation. It indicates the scaling limit of a device. In this chapter, the methods for obtaining the scale length expression of four structures of JLT- Pentagonal, Hexagonal, Octagonal and Rectangular has been presented. A comparison has been drawn among the scale lengths of the structures. This chapter provides a way of estimation of the scaling limit of the four structures mentioned which enables the selection of appropriate structure for a particular application.

Chapter 4   Depletion Width, Threshold Voltage and Potential Modelling of JLT

In this chapter, the depletion width model for a single and double gate JLT has been presented. The model of the threshold voltage obtained from depletion width model along with a complete potential model of double gate JLT is also presented in this chapter. The validation of the models by comparing with TCAD results and results available in literature is also presented. This chapter provides a threshold voltage model and a potential model which is valid in both short channel and long channel range. The accuracy obtained from the potential model is due to the inclusion of the source-drain regions completely in this model.

Chapter 5   Drain Current Modelling of JLT

An analytical model of drain current for double gate JLT is presented in this chapter. The accuracy and applicability of the model has been validated by comparing the model with TCAD simulation results and experimental results available in literature. This chapter

provides a fully analytical, practically applicable and accurate general drain current model. It will help in designing JLT accurately with reduced computation time.

Chapter 6   Enhancement of Performance Parameters of JLT

In this chapter, the proposal for enhancement of two performance parameters- off-state leakage current and carrier mobility of JLT has been presented along with a method for obtaining the minimum possible gate length for JLT. The models for the proposed structures have also been presented. The models of the proposed structures are validated by comparing with TCAD simulation results. The proposed structures are implemented in a CMOS inverter circuit. The voltage transfer characteristics and transient response of the CMOS inverter designed with the structures are compared using TCAD simulation. A study on corner effect in different structures of surrounding gate JLT has been carried out. A gate uderlap technique for reduction of corner effect is also presented and analysed. This chapter provides the concept of three new structures of JLT which exhibits lower off-state current and enhanced carrier mobility.

Chapter 7   Conclusions

The summary of the complete work, results and contribution of the thesis is presented in this chapter.

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