Chapter 2

Literature Review

2.1 Introduction

The field of VLSI is dominated by the devices based on the field effect principle of current control. The field-effect transistor (FET) has its root before BJT. FET was first patented by Julius Edgar Lilienfeld in 1930 and by Oskar Heil in 1935. However, due to the limitations of semiconductor materials and fabrication facilities, fabrication was not possible until the late forties . With the invention of MOSFET in 1960 by Atalla and Kahng the era of VLSI design started. In the last few decades astounding advancement could be seen in the field of VLSI design. The advancement in VLSI design and technology led to the introduction of many new devices and device structures such as Multigate FET, FinFET, High electron mobility transistor (HEMT), Single electron transistor (SET). Due to the continuous downscaling MOSFETs are on the verge of scaling limit. Due to the limitations of bulk MOSFET at very small dimension, several new devices such as, the SOI devices, strained Si devices, device with high k dielectric etc. appeared. With these structures it is possible to scale down the devices into the nanometre regime. Unfortunately the presence of the junction in these devices imposes certain other limitations in scaling down beyond a certain point in nanoscale regime. The Junctionless transistor (JLT) is one of the devices which posses a great potential in the field of VLSI devices in the sub 22nm regime. In 2009 J.P. Collinge and his associates successfully fabricated the first Junctionless transistor (JLT).

2.2 Evolution of MOSFET Technologies

Field effect principle was first reported by Lilienfeld [1] in 1926 and by Heil [2] in 1935. Kahng and Atala developed the first successful field effect transistor at Bell Labs in 1959 and the same was reported [3] in 1960. It was a Metal oxide semiconductor (MOS) based FET with high input impedance. With this the VLSI era started. The combination of active and passive element on an integrated circuit resulted in a performance degradation of the individual elements and consequently same was reflected on the circuit performance also. The active elements were required to be fabricated on semiconductor substrate while the passive elements were required to be fabricated on insulator substrate for best performance

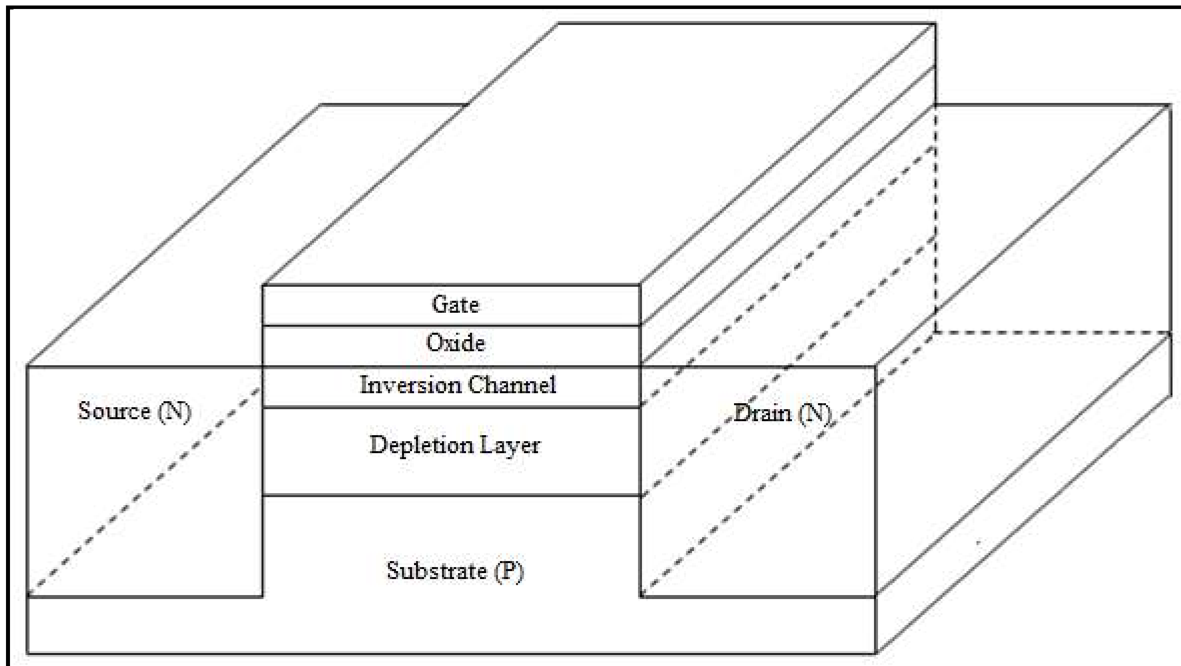
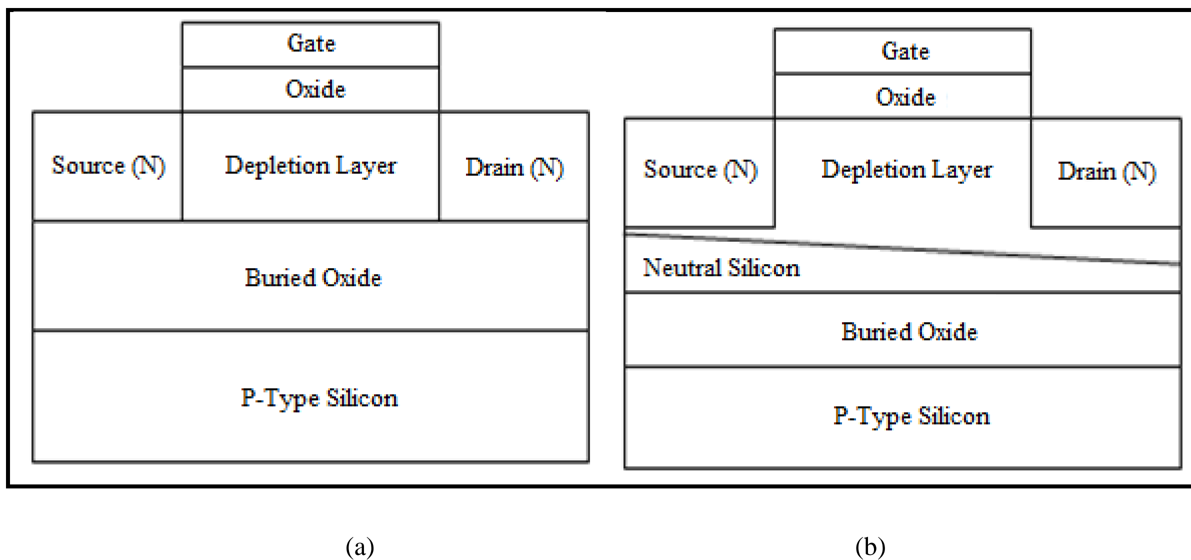


Fig. 2.1: A Bulk MOSFET [4]



(a) (b)

Fig. 2.2: Cross-sectional view of (a) Fully Depleted SOI MOSFET and (b) Partially Depleted SOI MOSFET [4]

individually. In order to get better performance while combining both active and passive devices on integrated circuit, silicon on insulator (SOI) technology was introduced [5]. In SOI technology, a MOSFET is grown on a thin layer of dielectric. This thin layer of dielectric is known as buried oxide. The SOI technology is divided into following two types [4-12].

- Partially Depleted
- Fully Depleted

In a partially depleted SOI MOSFET the depletion region exists only in part of the body. On the other hand in case of fully depleted SOI MOSFET the depletion region extends upto the buried oxide. The operation of partially depleted SOI MOSFET is similar to that of a bulk MOSFET. While in case of partially depleted SOI MOSFET the surface potential near the gate oxide is coupled to the potential near the buried oxide. The drain current expression for fully depleted SOI MOSFET and Bulk MOSFET are identical and can be written as [4],

$$I_d = \mu_n C_{ox} \frac{W}{L} \left\{ (V_{gs} - V_{th}) V_d - \frac{1}{2} n V_d^2 \right\}$$

and

$$I_{dsat} = \mu_n C_{ox} \frac{W}{L} \frac{(V_{gs} - V_{th})^2}{2n}$$

where the body factor n=1.5 for bulk MOSFET and n=1.05 for SOI MOSFET [4].
Some of the parasitic effects associated with SOI MOSFETs are-

(a) Floating Body effect

In an SOI MOSFET one of the major parasitic effect is the floating body effect. It is due to complete isolation of the device from the substrate. The holes generated by impact ionization creates a positive charge in the body which cannot be removed rapidly due to the absence of contact with silicon body. At a high drain voltage electron hole pairs are generated by the channel electrons through impact ionization The electrons generated in this process move towards drain while the holes move towards the P-type floating body as shown in Fig. 2.3. This positive charge comprised of holes rises many negative consequences termed as floating body effects such as- negative conductance, circuit instability, single transistor latch,

premature breakdown etc. With the help of a body contact some of these effects can be minimized [12].

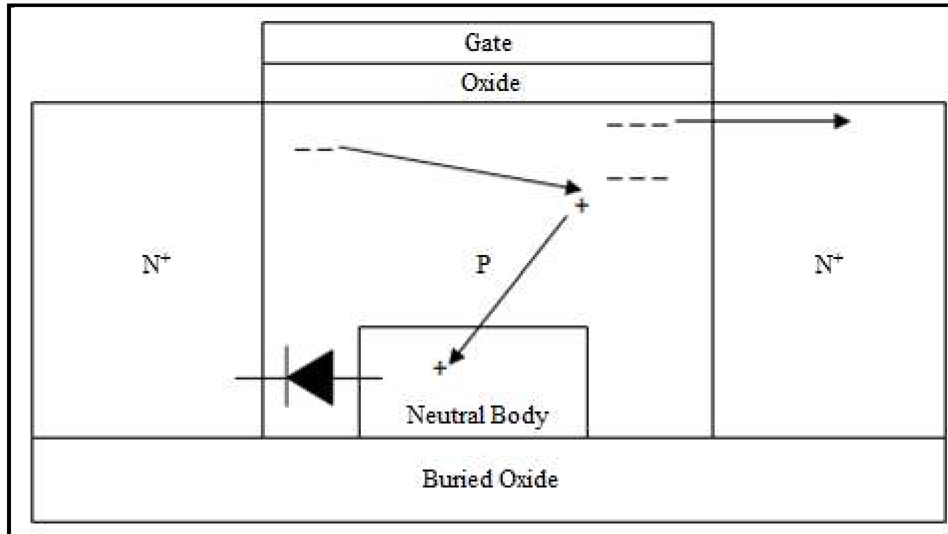


Fig. 2.3: Cross-sectional view of an SOI MOSFET showing floating body effect

(b) Kink effect

In the output characteristics of an SOI MOSFET operating in the strong inversion region a kink appears as shown in Fig. 2.4. The holes generated by the impact ionization moves towards the floating body which forward biases the source-body diode. A positive potential is attained by the floating body. The threshold voltage and source-body potential barrier is lowered due to the increase in body potential. This result in flow of more numbers of minority carriers from source to channel. It causes an excess drain current and creation of more numbers EHPs. The sudden rise in drain current is termed as kink. Kink effect is significant in partially depleted SOI MOSFETs. However the kink effect is reduced to a minimum in case fully depleted SOI MOSFET as the source-body diode is already forward biased due to full depletion. The p-channel devices are free of kink effect because coefficient of electron-hole pair generation by energetic holes is much lower than that by energetic electrons. The kink effect is not observed in bulk devices as the majority carriers generated by impact ionization can escape into the substrate or to a well contact [12].

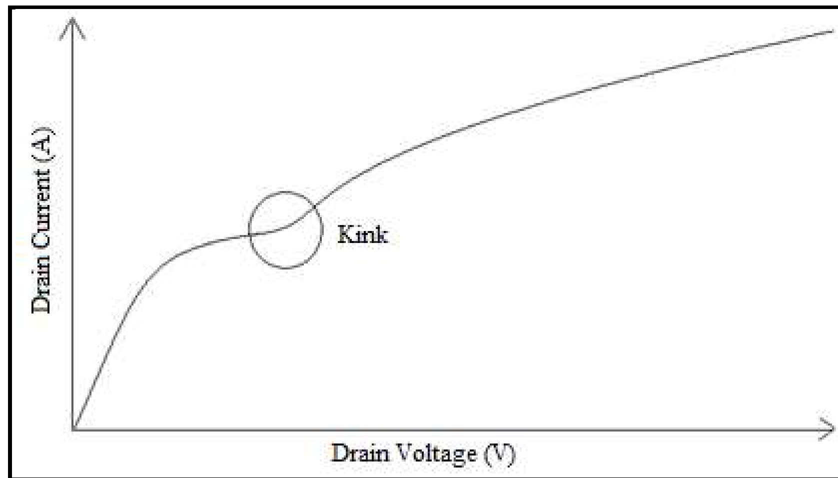


Fig. 2.4: Output characteristics of an SOI MOSFET showing Kink effect

The continuous downscaling of devices resulted in degradation of gate controllability due to following short channel effects-

(a) Punch-through

The width of the drain and source junctions can be written as [13],

$$x_{dD} = \sqrt{\left(\frac{2\in_{si}}{qN_a}\right)(V_{DS} + \phi_{si} + V_{SB})}$$

and

$$x_{dS} = \sqrt{\left(\frac{2\in_{si}}{qN_a}\right)(\phi_{si} + V_{SB})}$$

Where, V_{DS} and V_{SB} are the drain to source and source to body voltage.

When the channel length is shortened to a value at which the depletion regions around the source and drain regions merges (X_{dD}+X_{dS}=L), the gate gives up the control of the channel completely [13]. This condition is known as Punch-through. Punch-through can be reduced by thinner gate oxide, larger substrate doping and sallower junctions [13].

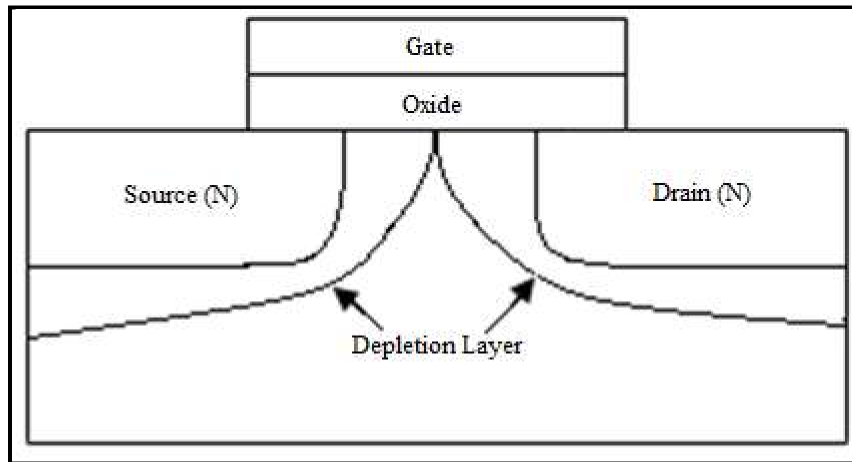


Fig. 2.5: Punch-through

(b) Drain Induced Barrier Lowering

When the device channel length is shortened into the nanometre regime the sole control of gate over the channel potential barrier is lost. The control of the potential barrier is shared between gate and drain in short channel devices. Therefore with increase in the drain voltage in short channel device causes reduction in the potential barrier which results in a decrease in threshold voltage. This effect is termed a drain induced barrier lowering (DIBL) [5,13]. The change in threshold voltage due to DIBL can be written as [13],

$$\Delta V_{th} = \frac{24t_{ox}}{W_{dm}} \sqrt{\psi_{bi}(\psi_{bi} + V_{ds})} e^{-\pi L/2(W_{dm}+3t_{ox})}$$

Where, t_{ox} is the gate oxide thickness, W_{dm} is the minimum depletion width at the threshold condition, L is the channel length, ψ_{bi} is the built in potential, V_{ds} is the drain voltage.

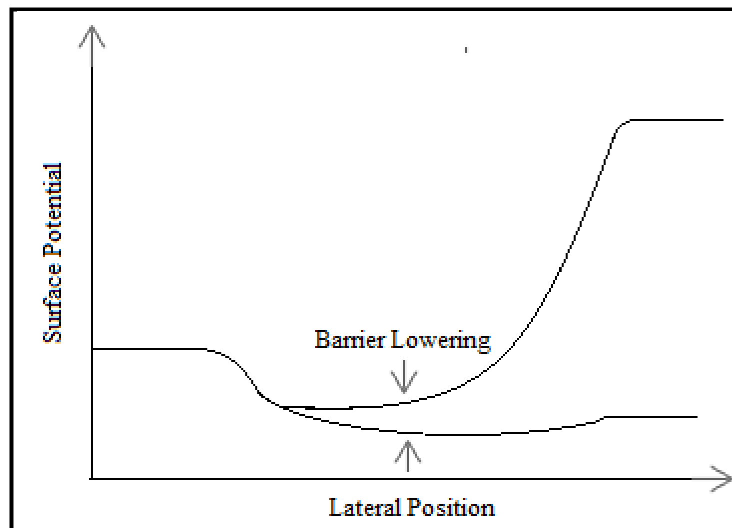


Fig. 2.6: DIBL

(c) Channel Length Modulation

In a short channel device an increase in the drain current is seen beyond the saturation voltage (V_{dsat}) due to decrease in the effective channel length as a function V_{ds} - V_{dsat}. This effect is called channel length modulation [4,13]. The drain current beyond saturation voltage can be written as [4,13],

$$I'_{dsat} = I_{dsat}(1-\frac{\Delta L}{L})^{-1}$$

Where, ΔL is the change in channel length given as [4],

$$\Delta L = L\left(1-\frac{1}{1+\frac{V_{ds}-V_{dsat}}{V_A+V_{dsat}}}\right)$$

Where V_A is positive voltage value termed as early voltage

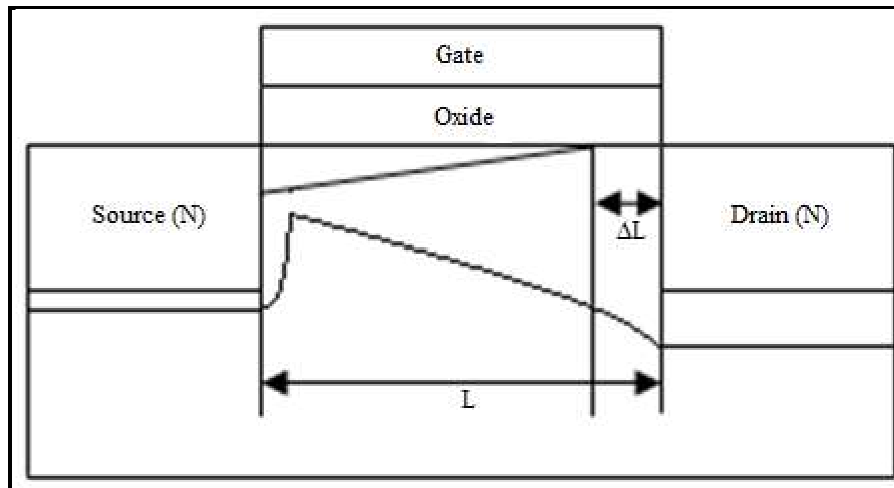


Fig. 2.7: Channel length modulation

(d) Gate Induced Drain Leakage

When the gate voltage is less than the drain voltage, a depletion region is created in the gate-drain overlap region. The high doping concentration in the drain causes the depletion region to become thin which results in a high electric field in the drain. Thus band to band tunnelling occurs in the overlap region which causes generation of electron-hole pair. The electrons and holes create a drain current and a substrate current respectively. This phenomenon is called gate induced drain leakage (GIDL) [4].

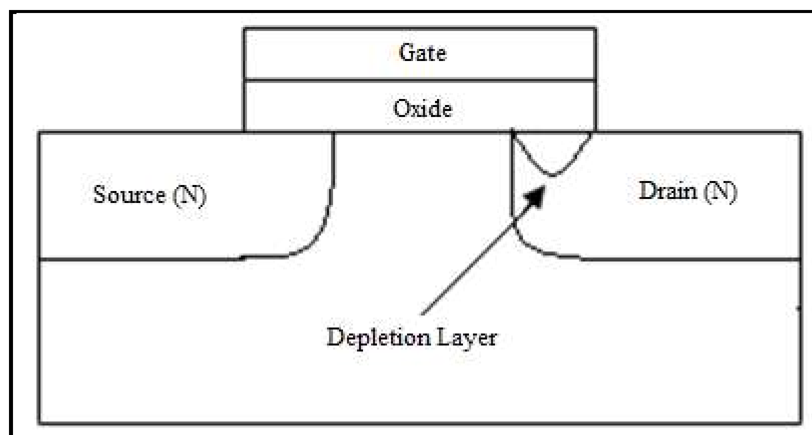


Fig. 2.8: Formation of a depletion layer in the drain

(e) Gate Oxide leakage

To reduce the chances of punch-through the gate oxide thickness is reduced. However, the reduction in gate oxide thickness beyond 2nm may cause gate tunnelling which constitutes the gate oxide leakage current [14]. By using a high-K dielectric the probability of gate oxide leakage can be minimized [14].

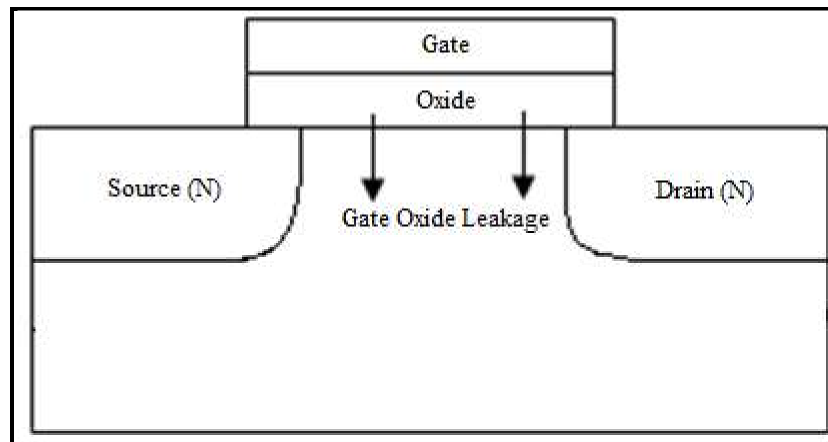


Fig. 2.9: Gate oxide leakage

(f) Fowler-Nordheim (F-N) tunnelling

Under the influence of an electric field band bending occurs resulting in apparent thinning of the barrier. Electrons and even holes can tunnel through the barrier and reach the conduction and the valance band of the oxide, respectively. This is called Fowler-Nordheim (F-N) tunnelling, first proposed by Fowler and Nordheim, where the electrons are injected by tunnelling into the conduction band of the oxide through a triangular energy barrier [15].

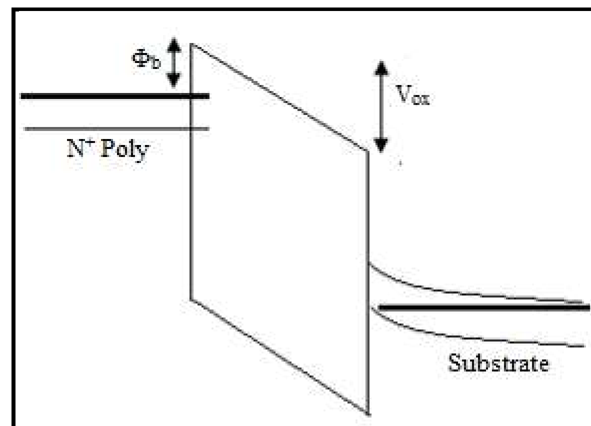


Fig. 2.10: Band diagram for F-N tunnelling

(g) Statistical Fluctuation of Dopant Atoms

Most widely used doping methods in semiconductors are by ion implantation or by insitu doping during thin film deposition. The amount of doping in these methods are estimated by pure statistics. In addition, the CMOS processing involves several high temperature anneal steps. The diffusion of dopant in the anneal steps is also based on statistics. When it comes to an ultra-scaled device, the volume of the semiconductor in the channel have shrunk down to few atoms and the dopant atoms are only a fraction of these. This makes the magnitude of doping in the channel a highly variable quantity. Also the position of the dopants are random. Both the number and position impact the device variability. As the channel lengths were scaled down, the doping in the channel was scaled up to improve the short channel behaviour of the device. This in turn increased the variability of the device. In addition, heavy doping in the channel also degrades the mobility because of scattering. An alternative set of devices, with undoped channels, were brought forward to address the issue of dopant fluctuations. Extremely thin silicon on insulator (ETSOI) and Fin FETs are examples of such devices [14].

(h) Velocity saturation

The scaling down of a device into the nano regime led to another short channel effect termed as velocity saturation which is resulted due to the reduction in effective mobility by a

high electric field. The velocity saturation forces the drain current to saturate at a value much lower than that of a long channel device. The velocity and electric field relation can be given as [13],

$$v = \frac{\mu_{eff} E}{[1 + (\frac{E}{E_c})^n]^{\frac{1}{n}}}$$

Where, n=2 for electron and n=1 for holes, E is the vertical electric field, E_c is critical field. When the vertical electric field is very high (E→∞) , $v = v_{sat}$. The saturation velocity can be written as [13]

$$v_{sat} = E_c \mu_{eff}$$

(i) Charge sharing effect

In case of long channel MOSFETs, gate has control over the channel and supports most of the charge. As channel length is shortened, the threshold voltage begins to decrease as the charge in the depletion region is now supported by the drain and the source also. Thus the gate needs to support less charge in this region and as a result, V_{th} falls down. This phenomenon is known as charge sharing effect [13].

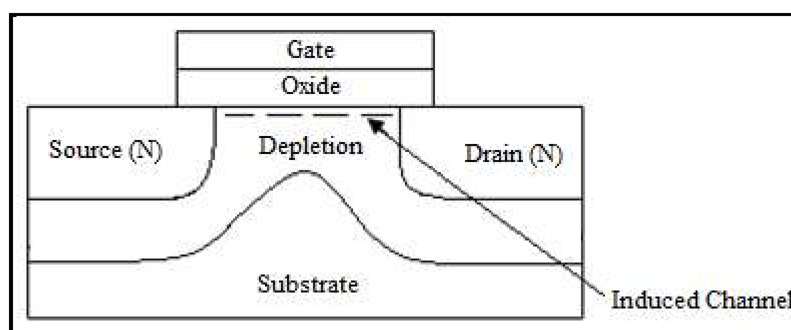


Fig. 2.11: Charge sharing effect

(j) Hot carrier effect

The very high electric field developed between the pinch off point and drain causes the electrons to acquire a high kinetic energy. These energetic electrons known as hot electrons can cause electron-hole pair generation and can overcome the gate oxide potential barrier to form a gate current. The holes generated forms substrate current. This effect is known as hot carrier effect [4]. Some of the hot carriers can have sufficient energy to overcome the oxide-Si barrier. They are injected from channel to the gate oxide and cause gate current to flow. Trapping of some of this charge can change threshold voltage permanently. Avalanching can take place producing electron-hole pairs. The holes produced by avalanching drift into the substrate and are collected by the substrate contact causing substrate current. voltage drop due to substrate current can cause substrate-source junction to be forward biased causing electrons to be injected from source into substrate. Some of the injected electrons are collected by the reversed biased drain and cause a parasitic bipolar action [4].

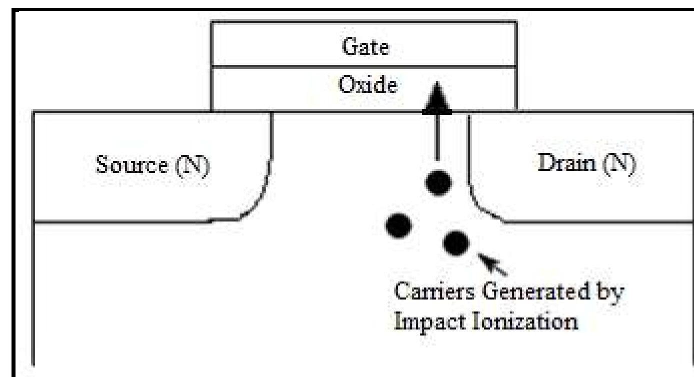


Fig. 2.12: Hot carrier effect

To overcome the limitations imposed on gate controllability by short channel effects resulting from downscaling of devices multigate MOSFETs were introduced [16,17,29,32,38]. The most basic multigate MOSFET structure is a planar double gate MOSFET [16]. Other additions in the multigate MOSFET are FinFET, triple gate MOSFET and Gate all around MOSFET [17,29,32,38].

The double gate MOSFET is nothing but an extension of SOI MOSFET as shown in Fig. 2.13. The DG MOSFET consists of two channels near the two gates. The body factor reduces to n=1 with comparatively lower short channel effects. Floating body effects can be minimized to an optimum value with the help of a double gate MOSFET. The double-gate structure was widely studied for application in sub-50-nm MOSFETs. It is because for conventional bulk MOSFETs, the high concentration punch-through stopper is indispensable but results in severe drivability and leakage degradation [17]. For the double-gate SOI-MOSFETs, the gates are able to control effectively the energy barrier between the source and drain. Therefore, the short channel effects can be suppressed without increasing the channel impurity concentration [18-22]. However, the studies found that the ultrathin body devices have different problems, such as parasitic resistance or threshold voltage controllability [23-25]. Moreover, the complexity of the fabrication process was a severe problem of double-gate structure as the Si-planar technology is not suitable to form the gate-channel-gate stacked structure that the double-gate device demands. To mitigate these problems a new structure termed as Fin-FET was proposed [26].

It is a self aligned double gate MOSFET structure as shown in Fig. 2.14. The channel of the device was formed on the side "vertical" surface of the Si-fin. The current flows in parallel to the wafer surface. It uses the elevated S/D process applied on DELTA [27]. The most important part of the FinFET is a thin Si fin. This fin serves as the body of the MOSFET. A heavily-doped poly-Si film wraps around the fin and makes electrical contact to the vertical faces of the fin. The poly-Si film greatly reduces the S/D series resistance and provide a convenient means for local interconnect and making connections to the metal [17]. A gap is etched through the poly-Si film to separate the source and drain. The width of this gap, further reduced by the dielectric spacers determines the gate length. The channel width is generally twice the fin height [17]. The conducting channel is wrapped around the surface of the fin. As the S/D and gate are much thicker (taller) than the fin, the device structure is quasiplanar.

In the case of single-gate FDSOI devices, the silicon body thickness needs to be about a third to a half of the electrical gate length in order to maintain full substrate depletion under gate control [27]. For non-planar double-gate FinFET devices, the thickness requirement for the silicon (W_{Si}) between the two gates is relaxed to approximately the electrical gate length, or two-thirds the physical gate length since each gate controls half the body thickness [28]. However, since W_{Si} is smaller than the physical gate length, the most critical lithography step in printing the double-gate transistor becomes the patterning of the Fin, rather than the physical gate length patterning [28]. More importantly, the tall vertical structure of the FinFET device presents significant challenges to device fabrication, since the transistor is fabricated vertical to the wafer plane on processing tools developed largely for planar horizontal devices. To overcome these challenges trigate MOSFETs as introduced [29-31].

The Gate all around (GAA) MOSFET with square section has been reported for the first time by Nitayama et al. [32]. The Gate all around MOSFETs are extension of tri gate MOSFET in which the gate wraps around the body of the device. In other words it can be said to have four gates. In such devices two electric flux lines at the corner are not parallel and mutually crossed at a point away from the oxide semiconductor interface. At that point the resultant electric field is considerably higher causing premature local turn on of the device [33-37]. In case of cylindrical device although the flux lines are not parallel there is a uniformity throughout the entire periphery. Hence such localized effect is not observed. To avoid the limitations of corner effect Cylindrical or circular cross sectioned GAA was introduced. A Cylindrical MOSFET was reported by Miyano et al. [38]. The cylindrical MOSFET exhibits superior subthreshold characteristics, enhanced electron mobility compared to its square counterpart. However, square cross sectioned MOSFETs has higher packing density compared to circular one. So some techniques to use the square MOSFET with reduced corner effect are also introduced. A technique to reduce the corner effect of square MOSFET was reported by Sharma and Chaudhury [39]. In this technique the gate width is reduced than the actual requirement. This is commonly known as gate underlap technique. After application of this method in these structures the gate does not remain a single piece of metal or a single piece of polycrystalline Silicon. Instead it becomes a set of

gate with a number of segments. Cross sectional views of Triple Gate MOSFET and Surrounding Gate MOSFET are shown in Fig. 2.15 and Fig. 2.16 respectively.

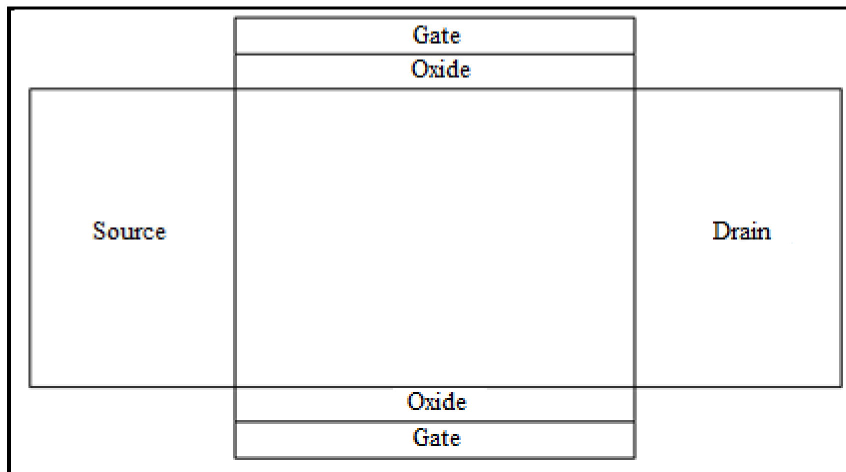


Fig. 2.13: Cross-sectional view of Double Gate SOI MOSFET [5]

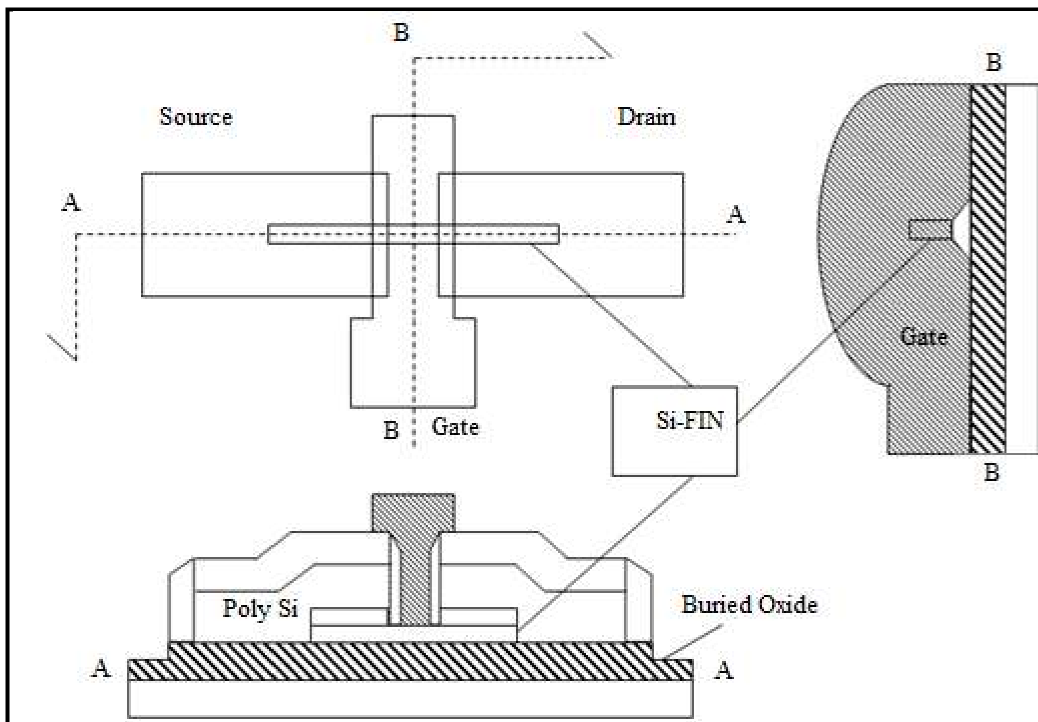


Fig. 2.14: FinFET typical layout and schematic cross sectional structures [17]

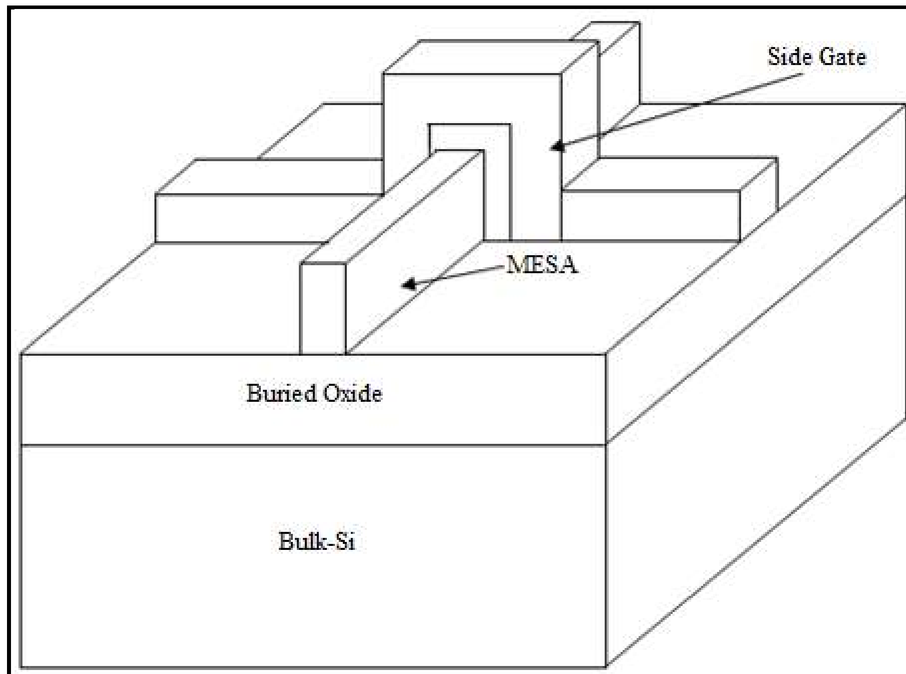


Fig. 2.15: Schematic of a triple-gate SOI transistor [28]

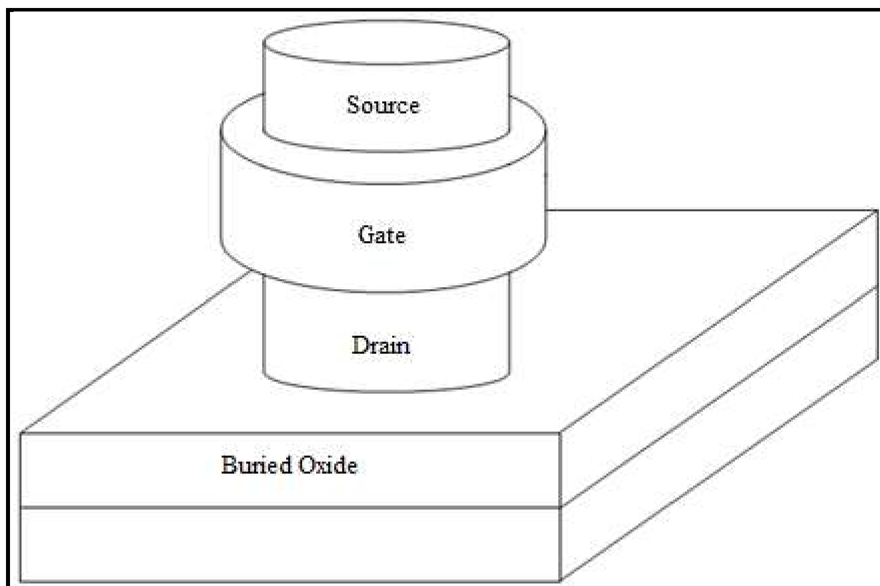


Fig. 2.16: CYNTHIA/surrounding-gate MOSFET structure [38]

Some technologies such as strained device are also introduced to reduce the short channel effects and enhance the carrier mobility [40]. The electron occupancy of the twofold and the fourfold valleys at room temperature is almost the same without any strain [41]. It is due to the fact that the lower subband energy of the twofold valleys is compensated by the higher density-of-states of the fourfold valleys having the higher valley degeneracy and the higher density-of-state mass. When tensile strain parallel to MOS interfaces or compressive strain perpendicular to MOS interfaces is applied to MOSFETs, the conduction band edge in the fourfold valleys becomes higher than that in the twofold valleys and this splitting energy is added to the subband energy difference caused by the surface quantization. As a result, the subband energy between the two valleys significantly increases. This increase in the subband energy splitting yields an increase in the inversion-layer mobility through the following two mechanisms. One is the increase in the average mobility due to the increase in the occupancy of electrons in the twofold valleys having higher mobility. The other is the suppression of inter-valley scattering between the twofold and the fourfold valleys. This is because, when the splitting energy between the twofold and the fourfold valleys is higher than the phonon energies associated with inter-valley scattering, the transition of electrons in the twofold valleys through a phonon absorption process cannot occur, resulting in the reduction in the scattering probability. Since the inter-valley scattering has a large contribution to the total scattering rate of Si MOSFETs at room temperature and the influence becomes larger with an increase in temperature, this increase in the mobility due to tensile strain is more effective in enhancing LSI performance during real operation at temperatures higher than room temperature [41].

Different advanced structures and technologies of MOSFET have been discussed. With these advanced structures it was possible to scale down in the nanometre regime to a significant extent. However, due to the presence of junction all of these techniques are reaching their physical limitations as the short channel effects such as punch-through, DIBL, channel length modulation etc. are directly associated with junction. Moreover the formation of ultra shallow junctions to minimize the short channel effects puts severe constraints on the thermal budget [42,43]. The reproducibility problems caused by random impurity fluctuations

from Source and Drain dopants scattered in the channel region is another limiting factor of devices with junctions [42,43]. To overcome the drawbacks associated with the devices with junctions the concept of Junctionless transistor (JLT) was introduced by Lee et al. [42] and first fabrication was reported by Collinge et al. [43] in 2009. The first JLT fabricated by Collinge et al. was a tri-gate JLT with 1μm channel length which shows the advantage of JLT over conventional MOSFETs such as extremely low DIBL, near ideal subthreshold slope [43]. Fig. 2.17 shows the evolution of MOSFET to JLT. In the next section a review on JLT is presented.

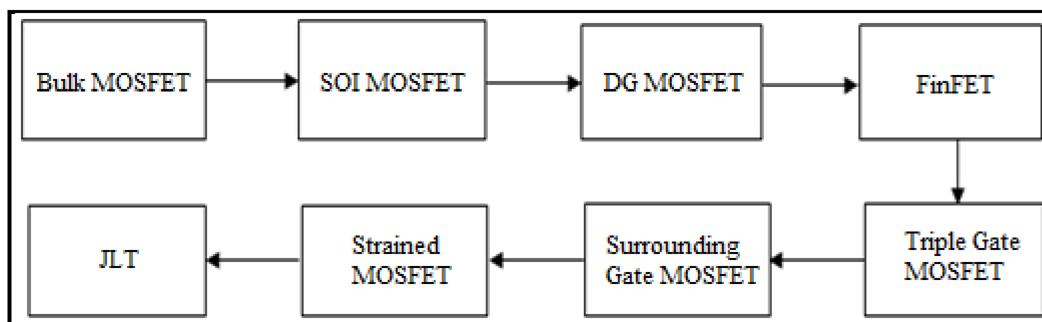


Fig. 2.17: Evolution of MOSFET from Conventional MOSFET to Junctionless Transistor

2.3 A Review on JLT

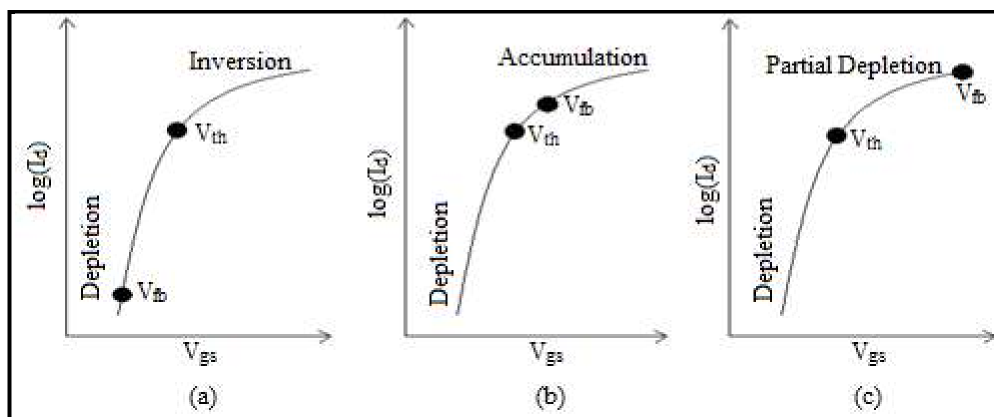


Fig. 2.18: Drain current as a function of gate voltage in (a) Inversion Mode MOSFET ("n^+pn^+" doped) (b) Accumulation mode MOSFET ("n^+nn^+"doped) (c) A heavily doped Junctionless Transistor ("$n^+n^+n^+$" doped) [42]

The electrical characteristics of JLT are similar to inversion mode MOSFET as shown in Fig. 2.18, but the device physics is quite different [42-49]. The difference between transfer characteristics of inversion mode MOSFET and JLT is that the flat band voltage of JLT is higher than its threshold voltage similar to accumulation mode MOSFET while flat band voltage of inversion mode MOSFET is lower than its threshold voltage [44]. However, the flat band voltage and threshold voltage difference for JLT is much larger than that of accumulation mode MOSFET [44]. The analytical model for a cylindrical JLT which clarifies the nearly ideal subthreshold slope and excellent on-state characteristics of JLT was reported by Gnani et al. [45]. The JLT shows full CMOS functionality [46]. The Physics of JLT was reported by Collinge [47]. The guidelines for design as well as the basic properties of JLT was reported by Collinge et al. [48] which shows the dependence of threshold voltage of JLT on the four parameters- the doping concentration, gate oxide thickness, device width and channel thickness.

Channel potential models of JLT for different structures such as a double gate, triple gate, cylindrical etc. have been reported by many researchers [50-55]. The potential model by partially considering extension of depletion layer into the source-drain region of a double gate JLT has been reported by Gnudi et al. [50]. This model shows accuracy for longer source and drain region. A fully analytical channel potential model for a triple gate JLT was reported by Travisoli et al. [51]. Li et al. [52] reports the channel potential model for a short channel cylindrical JLT while the analytical potential model for a DG JLT has been reported by Holtiz et al. [53] using Schwarz-Christoffel transformation. Another approach for analytical potential modelling of DG JLT has been reported by Chiang [54]. A channel potential model for a cylindrical JLT using 2-D approximation of 3-D Poisson's equation in cylindrical coordinate system has been reported by Chiang [55]. In all the works reported earlier, the source-drain regions have not been completely considered in the model formulation. The extension of the depletion region in the source-drain regions play an important role in device characteristics in the case of small dimension device as the depletion region may extend to the ohmic contact.

Few models of drain current have also been reported [56-60]. Sallese et al. [56] have reported a charge based model for the drain current of double gate JLT. Duarte et al. [57] have reported a full-range current model for double gate JLT. Gnudi et al. [50] have reported a semi-analytical expression for the current within the drift-diffusion approximation. Li et al. [52] have reported a subthreshold current model for Cylindrical Surrounding Gate MOSFETs. The drain current models for long channel DG JLT has been reported by Lime et al. [58] and Duarte et al [59]. Most of these models are not fully analytical and requires several iterations for solving it numerically. Hence computation time increases.

An expression for depletion width for long channel JLT along with bulk current and threshold voltage has been reported by Duarte et al. [59]. In this work the threshold voltage expression was obtained from the bulk current expression. The depletion width and threshold voltage expressions are simpler but not suitable for short channel devices. Gupta et al. [60] have reported another threshold voltage model. The threshold voltage in this model was computed by computing the minimum potential. This model shows high accuracy for some specific values of channel length only. Few works on performance enhancement of JLT have also been reported [61-65]. Lou et al. [61] reported a dual material gate JLT that exhibits improved on-state current, reduced DIBL and enhanced transconductance. Gundapaneni et al. [62] have reported the enhancement of electrostatic integrity of short-channel JLT with high-k spacers. Baruah and Paily [63] have reported a double gate JLT using dual-material gate along with high-k spacer dielectric (DMG-SP) on both sides of the gate oxides of the device for enhanced analog performance. Raskin et al. [64] have reported a method for enhancing the carrier mobility of JLT using uniaxial strain by applying compressive stress to p-type JLT and traction stress to n-type JLT. The direction of application of stress is parallel to the current flow in the devices. A comparison of corner effect in inversion mode MOSFET and JLT has been reported by Lee et al. [66]. The corner effect in JLT is less significant compared to inversion mode MOSFET. Use of CNT in JLT has been reported by Barik et al. [67,68]. However, for mass production by the semiconductor industries Si-based devices are more suitable compared to CNT.

2.4 Conclusions

A discussion on evolution of MOSFET technologies starting from bulk MOSFET to JLT is presented. Different structures of MOSFET has been presented in historical and chronological order. A brief review on some of the works reported on JLT is also presented. As the junctoned MOSFET technologies are reaching their physical limitations, the JLT may replace the junctioned MOSFET in near future and carry on the Moore's law for another couple of decades.

Bibliography

[1] Lilienfield, J. E. *Method and Apparatus for Controlling Currents* **U.S. Patent 1,745,175**, Jan 28, 1930

[2] Heil, O. *Improvements in or Relating to Electrical Amplifiers and Other Control Arrangements and Devices* **British Patent 439,457**, Dec 6, 1935

[3] Kahng, D. and Atalla, M. M. Silicon-silicon Dioxide Field Induced Surface Devices. In *IRE-A IEEE Solid-State Device Research Conference*, Carnegie Institute of Technology, Pittsburgh, PA, 1960

[4] Colinge, J. P. and Colinge, C. A. *Physics of Semiconductor Devices*, Kluwer Academic Publishers, 2002

[5] Mueller, C. W. and Robinson P.H. Grown-film Silicon Transistor on Sapphire. *Proceedings of the IEEE,* 52(12)**,** pages 1487-1490, 1964

[6] Crisoloveanu, S. SOI Technologies, Materials and Devices. In *1996 IEEE International SOI Conference*, Pages 3- 12, Sanibel Island, Florida, 1996

[7] Lin, S. C. and Kuo, J. B. Temperature-Dependent Kink Effect Model for Partially-Depleted SOI NMOS Devices. *IEEE Transactions on Electron Devices*, 46(1), pages 254-258, 1999

[8] Cheng, B. Rao, V. R. and Woo, J. C. S. Sub 0.18 μm SOI Mosfets Using Lateral Asymmetric Channel Profile and Ge Pre-Amorphization Salicide Technology. In *Proceedings of The IEEE SOI Conference*, Stuart, Florida, USA, 1998.

[9] Cristoloveanu, S. and Li, S. S. *Electrical Characterization of Silicon-On-Insulator Materials And Devices.* Kluwer Academic Publishers, 1995.

[10] Chen, C. E. D., Matloubian, M., Sundaresan, R., Mao, B. Y., Wei, C. and Pollack, G. P. Single Transistor Latch in SOI MOSFET's. *IEEE Electron Device Letters*, 9(12), Pages 636-638, 1988

[11] Sleight J. and Mistry, K. A Compact Schottky Body Contact Technology for SOI Transistors. In *International Electron Devices Meeting, (IEDM) Digest*, Pages. 419 - 422. 1997.

[12] Vandana, B. Study of Floating Body Effect in SOI Technology *International Journal of Modern Engineering Research (IJMER)* 3(3), pages 1817-1824, 2013

[13] Taur, Y. and Ning, T. H. *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998

[14] Gundapaneni, S. *Investigation of Junction-Less Transistor (JLT) for CMOS Scaling*. Ph.D. Thesis, Department of Electrical Engineering, Indian Institute of Technology, Bombay, 2012

[15] Apte P. P. and Saraswat, K. C. SiO2 Degradation with Charge Injection Polarity *IEEE Electron Device Letters,* 14(11), pages 512, 1993

[16] Barsan, R. M. Analysis and Modelling of Dual-Gate MOSFETs. *IEEE Transactions on Electron Devices*, 28(5), pages 523 - 534, 1981

[17] Hisamoto, D., Lee, W. C., Kedzierski, J., Takeuchi, H., Asano*, K.,* Kuo, C., Anderson, E., King, T. J., Bokor, J., and Hu, C. FinFET—A Self-Aligned Double-Gate MOSFET

Scalable to 20 nm. *IEEE Transactions on Electron Devices*, 47(12), pages 2320-2325, 2000

[18] Frank, D. J., Laux, S. E. and Fischetti, M. V. Monte Carlo Simulation of A 30 nm Dual-gate MOSFET: How Short can Si Go?. In *IEDM Technology Digest*, 1992, pages 553–556

[19] Fiegna C. Iwai, H., Wada, T., Saito, T., Sangiorgi, E., Ricco., B. A New Scaling Methodology for The 0.1–0.025 μm MOSFET. In *VLSI Symposium Technology Digest*, pages. 33–34¸1993

[20] Suzuki K., Tanaka, T.,Tosaka, Y., Horie, H. and Arimoto, Y. Scaling Theory for Double-gate SOI MOSFET's. *IEEE Transactions on Electron Devices*, 40(12), pages 2326–2329, 1993

[21] Wong, H. S., Frank, D. J., Taur, Y. and Stork, J. M. C. Design and Performance Considerations for Sub-0.1 um Double-gate SOI MOSFET's. In *IEDM Technology Digest*, pages 747–750,1994

[22] Majkusiak, B., Janik, T. and Walczak, J. Semiconductor Thickness Effects in The Double-gate SOI MOSFET, *IEEE Transactions on Electron Devices*, 45(5), pages 1127–1134, 1998

[23] Su, L. T., Sherony, M. J., Hu, H., Chung, J. E. and Antoniadis, D. A. Optimization of Series Resistance in sub-0.2 μm SOI MOSFETs. In *IEDM Technology Digest*, pages 723–726, 1993

[24] Hisamoto D., Nakamura, K., Saito, M., Kobayashi, N., Kimura, S., Nagai, R. Nishida, T. and Takeda, E. Metallized Ultra-shallow-junction Device Technology for sub-0.1 μm Gate MOSFET's. *IEEE Transactions on Electron Devices*, 41(5), pages 745–750, 1994

[25] Hwang J. and Pollack, G. Novel polysilicon/TiN Stacked-gate Structure for Fully-depleted SOI/CMOS. *In IEDM Technology Digest*, pages 345–348, 1992

[26] Hisamoto D., Lee, W. C., Kedzierski, J., Anderson, E., Takeuchi, H., Asano, K., King, T. J., Bokor, J. and Hu, C. A Folded-channel MOSFET for Deep-sub-tenth Micron Era. *In IEDM Technology Digest*, pages 1032–1034, 1998

[27] Chau, R., Kavalieros, J., Doyle, B., Murthy, A., Paulsen, N., Lionberger, D. Barlage, D. Arghavani, R., Roberds, B. and Doczy, M. A 50 nm Depleted-substrate CMOS Transistor (DST). In *IEDM Technology Digest*, pages 621–624, 2001

[28] Lindert, N., Chang, L., Cho, Y. K., Anderson, E. H., Lee, W. C., King, T. J., Bokor, J., and Hu, C. M. Sub-60-nm Quasiplanar FinFET's Fabricated using A Simplified Process. *IEEE Electron Device Letters*, 22, pages 487–489, 2001

[29] Park, J. T., Colinge, J. P. and Diaz, C. H. Pi-Gate SOI MOSFET. *IEEE Electron Device Letters*, 22, pages 405–406, 2001

[30] Lemme, M., Mollenhauer, T., Henschel, W., Wahlbrink, T., Gottlob, H., Efavi J., Baus, M., Winkler, O., Spangenberg, B., and Kurz H. Subthreshold Characteristics of p-type Triple-Gate MOSFETs. In *33rd Conference on European Solid state Device Research (ESSDERC, 03),* pages 123-126, Estoril, Portugal, 2003

[31] Doyle, B. S., Datta, S., Doczy, S., Hareland, M., Jin, B., Kavalieros, J., Linton, T., Murthy, A., Rios, R. and Chau., R. High Performance Fully-Depleted Tri-Gate CMOS Transistors. *IEEE Electron Device letters*, 24(4), pages 263-265, 2003

[32] Nitayama A., Takato, H., Okabe, N., Sunouchi, K., Hieda, K., Horiguchi, F., and Masuoka, F. Multi Pillar Surrounding gate transistor (M-SGT) for Compact and High Speed Circuits. *IEEE Transactions on Electron Devices,* 38(3), pages 579-583, 1991

[33] Colinge, J. P. *FinFET and Other Multi-Gate Transistors*, Springer 2008

[34] Fossum, J. G., Yang, J. W. and Trivedi, V. P. Suppression of Corner Effects in Triple-Gate MOSFETs, *IEEE Electron Device Letters*, 24, pages 745-747, 2003

[35] Kumar, M. P., Gupta, S. K. and Paul, M. Corner Effects in SOI-Tri gate FinFET Structure by Using 3D Process and Device Simulations. In *3rd IEEE International Conference on Computer Science and Information Technology (ICCSIT)*, 9, pages 704 – 707, 2010

[36] Xiong, W., Park, J. W. and Colinge, J. P. Corner Effect in Multiple-gate SOI MOSEFT. *IEEE International SOI Conference*, pages 111-113, 2003

[37] Michielis, L. D., Moselund, K. E., Selmi, L. and Ionescu, A. M. Corner Effect and Local Volume Inversion in SiNW FETs. *IEEE Transactions on Nanotechnology*, 10(4), pages 810-816, 2011

[38] Miyano S, Hirose, M., and Masuoka, F. Numerical Analysis of A Cylindrical Thin-Pillar Transistor (CYNTHIA). *IEEE Transactions on Electron Devices*, 39(8), pages 1876-1881, 1992

[39] Sharma, S. and Chaudhury, K. A Novel Technique for Suppression of Corner Effect in Square Gate All Around Mosfet. *Electrical and Electronic Engineering* ,2, pages 336-341, 2012

[40] Krishnamohan, T., Comparison of (001), (110) and (111) uniaxial- and biaxial- strained-Ge and Strained-Si PMOS DGFETs for All Channel Orientations: Mobility Enhancement, Drive current, Delay and Off-state Leakage. *In IEEE International Electron Devices Meeting*, 2008

[41] Takagi, S., Hoyt, J. L., Welser, J. J. and Gibbons, J. F. Comparative Study of Phonon-limited Mobility of Two-dimensional Electrons in Strained and Unstrained Si Metal–oxide–semiconductor Field-effect Transistors. *Journal of Applied Physics*, 80(3), pages 1567-1577, 1996

[42] Lee, C. W., Afzalian, A., Akhavan, N. D., Yan, R., Ferain, I., and Colinge. J. P. Junctionless Multigate Field Effect Transistor. *Applied Physics Letters*, 94(5), pages 053511, 2009

[43] Colinge J. P., Lee, C. W., Afzalian, A., Dehdashti, N., Yan, R., Ferain, I., Razavi, P., O’Neill, B., Blake, A., White, M., Kelleher, A. M., McCarthy B., and Murphy R. SOI Gated Resistor: CMOS without Junctions. In *IEEE International SOI Conference*, pages 1-2, Foster City, California, USA , 2009

[44] Park, C. H., Ko, M. D., Kim, K. H., Baek, R. H., Sohn, C. W., Baek, C. K., Park, S., Deen, M. J., Jeong, Y. H., and Lee, J. S. Electrical Characteristics of 20-nm Junctionless Si Nanowire Transistors. *Solid-State Electronics,* 73, pages 7–10, 2012

[45] Gnani, E., Gnudi, A., Reggiani, S., and Baccarani, G. Theory of The Junctionless Nanowire FET. *IEEE Transactions on Electron Devices*, 58(9), pages 2903 - 2910, 2011

[46] Colinge, J. P., Lee, H. W., Afzalian, A., Akhavan, N. D., Yan, R., Ferain, I., Razavi, P., O'Neill, B., Blake, A., White, M., Kelleher, A. M., McCarthy, B., and Murphy, R. Nanowire Transistors without Junctions. *Nature Nanotechnology*, 5, pages 225–229, 2010

[47] Colinge, J. P. Junctionless Transistors. In *IEEE International Meeting for Future of Electron Devices*, pages 1-2, Kansai (IMFEDK), 2012

[48] Colinge, J. P., Kranti, A., Yan, R., Lee, C. W., Ferain, I., Yu, R., Akhavan, N. D., and Razavi P. Junctionless Nanowire Transistor (JNT): Properties and Design Guidelines. *Solid- State Electronics*, 65–66, pages 33-37, 2011

[49] Nazarov, A., Balestra, F., Raskin, J. P., Gamiz, F., and Lysenko, V.S. *Semiconductor-On-Insulator Materials for Nanoelectronics Applications*, Springer, 2011

[50] Gnudi, A., Reggiani, S., Gnani, E., and Baccarani, G. Semi analytical Model of The Subthreshold Current in Short-Channel Junctionless Symmetric Double-Gate Field-Effect Transistors. *IEEE Transactions on Electron Devices*, 60(4), pages 1342-1348, 2013

[51] Trevisoli, R. D., Doria, R. T., de Souza, M., Das, S., Ferain, I., and Pavanello, M. A. Surface Potential Based Drain Current Analytical Model for Triple Gate Junctionless Nanowire Transistors. *IEEE Transactions on Electron Devices*, 59(11), pages 3510–3518, 2012

[52] Li, C., Zhuang, Y., Di, S., and Han, R. Subthreshold Behaviour Models for Nanoscale, Short-Channel Junctionless Cylindrical Surrounding-Gate MOSFETs. *IEEE Transactions on Electron Devices*, 60(11), pages 3655-3662, 2013

[53] Holtij, T., Schwarz, T., Kloes, A., and Iñiguez, B. 2D Analytical Potential Modelling of Junctionless DG MOSFETs in Subthreshold Region Including Proposal for Calculating the Threshold Voltage. In *13th International Conference on ULIS*, pages 81-84, MINATEC Grenoble, France, 2012

[54] Chiang, T. K., A Quasi-two-dimensional Threshold Voltage Model for Short-Channel Junctionless Double-gate MOSFETs. *IEEE Transactions on Electron Devices*, 59 (9), pages 2284–2289, 2012

[55] Chiang, T. K., A New Quasi-2-D Threshold Voltage Model for Short Channel Junctionless Cylindrical Surrounding Gate (JLCSG) MOSFETs. *IEEE Transactions on Electron Devices*, 59(11), pages 3127–3129, 2012

[56] Sallese, J. M., Chevillon, N., Lallement, C., Iñiguez, B., and Prégaldiny., F. Charge-Based Modeling of Junctionless Double-Gate Field-Effect Transistors. *IEEE Transactions on Electron Devices*, 58(8), pages 2628-2637, 2011

[57] Duarte, J. P., Choi, S. J., and Choi Y. K. A Full-Range Drain Current Model for Double-Gate Junctionless Transistors. *IEEE Transactions on Electron Devices*, 58(12), pages 4219-4225, 2011

[58] Lime, F., Santana, E., and Iñiguez, B. A Simple Compact Model for Long-channel Junctionless Double Gate MOSFETs. *Solid-State Electronics*, 80(2), pages 28-32, 2013

[59] Duarte, J. P., Choi, S. J., Moon, D. I., and Choi Y. K. Simple Analytical Bulk Current Model for Long-Channel Double-Gate Junctionless Transistors. *IEEE Electron Device Letters*, 32(6), pages 704-706, 2011

[60] Gupta, P., Burman, D., Das., J., Brahma, M., Rahaman, H., and Dasgupta, P. Modelling The Channel Potential and Threshold Voltage of a Fully Depleted Junctionless Double Gate FET. In *International Conference on Communications, Devices and Intelligent Systems (CODIS)*, pages 149-152, Kolkata, 2012

[61] Lou, H., Zhang, L., Zhu, Y., Lin, X., Yang, S., He, J., and Chan, M. A Junctionless Nanowire Transistor with A Dual-material Gate. *IEEE Transactions on Electron Devices*, 59(7), pages 1829–1836, 2012

[62] Gundapaneni, S., Ganguly, S., and Kottantharayil, A. Enhanced Electrostatic Integrity of Short-Channel Junctionless Transistor With High-κ Spacers. *IEEE Electron Device Letters*, 32(10), pages 1325-1327, 2011

[63] Baruah, R. K. and Paily, R. A Dual-Material Gate Junctionless Transistor With High-k Spacer for Enhanced Analog Performance. *IEEE Transactions on Electron Devices,* 61 (1), pages 123-128, 2014

[64] Raskin, J. P., Colinge, J. P., Ferain, I., Kranti, A., Lee, C. W., Dehdashti, N., Yan, R., Razavi, P., and Yu., R. Mobility Improvement in Nanowire Junctionless Transistors by Uniaxial Strain. *Applied Physics Letters,* 97(4), pages 042114, 2010

[65] Sorée, B., Magnus, W., and Vandenberghe, W. Low-field Mobility in Ultrathin Silicon Nanowire Junctionless Transistors. *Applied Physics Letters*, 99(23), pages 233509, 2011

[66] Lee, B. H., Hur, J., Kang, M. H., Bang, T., Ahn, D. C., Lee, D., Kim, K. H. and Choi, Y. K. A Vertically Integrated Junctionless Nanowire Transistor. *Nano Letters*, 16 (3), pages 1840–1847, 2016

[67] Barik, M. A., Sarma. M. K., and Dutta, J. C. Traditional Graphene and Junctionless Carbon Nanotube Field Effect Transistor for Cholesterol Sensing. In *IEEE 2nd International Conference on Emerging Electronics (ICEE),* pages 1-4, IISc, Bangalore, 2014

[68] Barik, M. A., Deka, R., and Dutta, J. C. Carbon Nanotube- Based Dual Gated Junctionless Field-Effect Transistor for Acetylcholine Detection. *IEEE Sensor Journal*, 16(2), pages 280-286, 2016