Chapter 4

Depletion Width, Threshold Voltage and Potential Modelling of JLT

4.1 Introduction

High value of work function difference between the gate material and channel material induces an internal electric field at the oxide semiconductor interface which leads to formation of depletion layer throughout the complete substrate. As a consequence, under this condition, device is devoid of free electrons and it cannot carry any current or the device is said to be in its off state [1-18]. However, when a gate voltage is applied, the resulting electric field counteracts the internally induced electric field (Electric field established due to work function difference). As a result the net electric field present in the oxide semiconductor interface starts decreasing with increase in the applied gate to source voltage. As a result width of the depletion layer starts decreasing. At this stage the device is no longer in the fully depleted state, i.e., the farthest portion of the device from the insulator semiconductor interface loses its depletion layer [1-18]. The value of the gate to source voltage at which this phenomenon occurs is known as threshold voltage of the device. At this stage current can flow through that non depleted portion of the device. As the gate voltage increases above threshold voltage the effective electric field in the semiconductor oxide interface further reduces leading to further reduction of depletion layer. Thus depletion width plays an important role in the conduction mechanism of JLT. In this entire process of gate voltage variation and the resulting variation in the depletion layer in the substrate can be linked to the variation in the potential inside the substrate. In this chapter analytical modelling has been done for the followings-

1. Depletion Width

In this part of work a generalized mathematical model for the depletion width of junctionless transistor has been obtained using the Poisson's equation. The Poisson's equation used in this part has been solved using trial function and boundary condition method.

2. Threshold Voltage

In this part of work a physics based model for threshold voltage of a junctionless transistor has been developed. For obtaining the threshold voltage of the device depletion width model considering depletion approximation has been taken as the reference. Based on this equation, potential along the central axis of the device has been obtained to find out the threshold voltage of the device.

3. Potential Modelling

In last part of this chapter the channel potential model has been obtained by solving the Poisson's equation using trial function method. This part of work has been carried out to develop a complete potential model of junctionless transistor. In this model influence of the source and drain region has also been taken into account.

The models developed in the chapter has been simulated in MATLAB and the results obtained has been compared and validated with results obtained from TCAD simulation and also with few experimental results available in literature.

4.2 Depletion Width Modelling of JLT

4.2.1 Mathematical Formulation

For the mathematical formulation, one dimensional Poisson's equation has been used as the quantity to be modelled is an one dimensional quantity. One dimensional Poisson's equation at a moderate substrate doping concentration can be written as [19],

$$\frac{d^2\phi(y)}{dy^2} = \frac{qN_a}{\in_{si}} \quad \text{for p-channel} \tag{4.1A}$$

$$\frac{d^2\phi(y)}{dy^2} = -\frac{qN_d}{\in_{si}} \quad \text{for n-channel} \tag{4.1B}$$

Where,

$\phi(y)$ is the electrostatic potential

q is charge of a carrier (hole or electron)

N_a and N_d are acceptor and donor doping concentration

ϵ_{si} is the permittivity of silicon.

Using parabolic trial function method one solution of Poisson's equation can be considered as[20],

$$\phi(y) = C_0 + C_1 y + C_2 y^2 \tag{4.2}$$

The solution considered in (4.2) can be used for both single gate and double gate JLT. Only the boundary conditions will be different for the two structures. The cross-sectional view of a single gate JLT is shown in Fig. 4.1 and a double gate JLT is shown in Fig. 4.2.

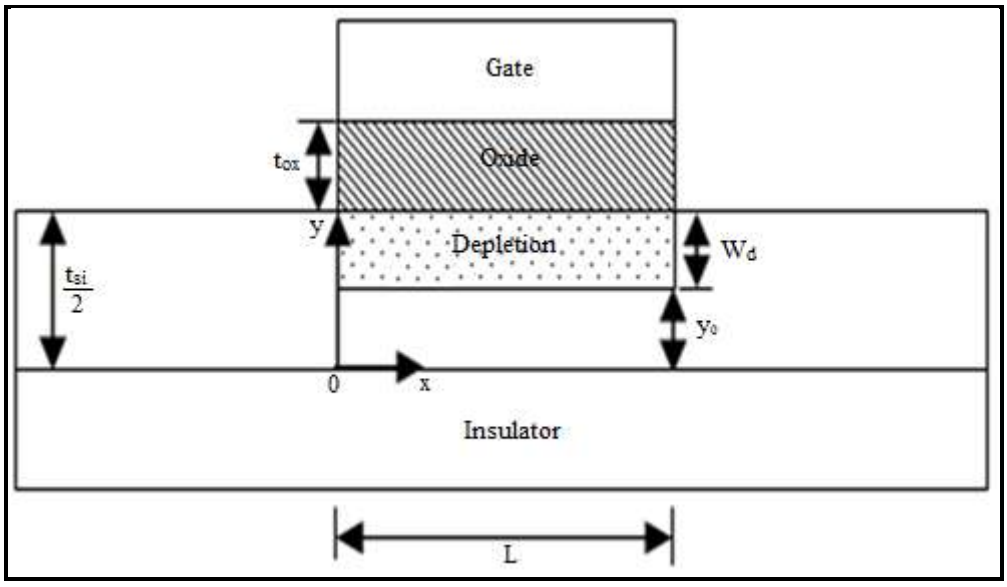

Fig. 4.1: Single Gate JLT

For a single gate JLT,

at, $y=t_{si}-W_d$, where, W_d is the depletion width and t_{si} is the channel thickness, potential $\phi(y)$ can be written as,

$$\phi(y) = C_0 + C_1(t_{si} - W_d) + C_2(t_{si} - W_d)^2 = \phi_0 \tag{4.3}$$

At y=0,

$$\frac{d\phi(y)}{dy} = 0 = C_1 \tag{4.4}$$

At $y=t_{si}$,

$$\frac{d\phi(y)}{dy} = 2t_{si}C_2 = \frac{\in_{ox}}{\in_{si} t_{ox}}(\phi_{gs} - \phi_s) \tag{4.5}$$

Or $$C_2 = \frac{\in_{ox}}{2t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s) \tag{4.6}$$

Where,

ϕ_s is the surface potential

ϵ_{ox} is the permittivity of the gate oxide

t_{ox} is the gate oxide thickness

$\phi_{gs}=V_{gs}-V_{fb}$

where,

V_{gs} is gate to source voltage

V_{fb} is the flat band voltage.

Therefore, $C_0 = \phi_0 - C_2(t_{si} - W_d)^2 = \phi_0 - \frac{\in_{ox}(t_{si} - W_d)^2}{2 \in_{si} t_{si} t_{ox}}(\phi_{gs} - \phi_s)$

$$\phi(y) = \phi_0 - \frac{\in_{ox}(t_{si} - W_d)^2}{2 \in_{si} t_{si} t_{ox}}(\phi_{gs} - \phi_s) + \frac{\in_{ox}}{2t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s)y^2 \quad (4.7)$$

At $y=t_{si}$,

$$\phi(y) = \phi_s = \phi_0 - \frac{\in_{ox}(t_{si} - W_d)^2}{2 \in_{si} t_{si} t_{ox}}(\phi_{gs} - \phi_s) + \frac{\in_{ox}}{2t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s)t_{si}^2$$

$$\text{Or, } \phi_s = \phi_0 \frac{2 \in_{si} t_{si} t_{ox}}{2 \in_{si} t_{si} t_{ox} - \in_{ox}(t_{si} - W_d)^2 + \in_{ox} t_{si}^2} + \frac{\in_{ox} t_{si}^2 - \in_{ox}(t_{si} - W_d)^2}{2t_{si} \in_{si} t_{ox} - \in_{ox}(t_{si} - W_d)^2 + \in_{ox} t_{si}^2}\phi_{gs} \quad (4.8)$$

Putting ϕ_s from (4.8) in (4.7),

$$\phi(y) = \phi_0 - \frac{\in_{ox}(t_{si} - W_d)^2}{2 \in_{si} t_{si} t_{ox} - \in_{ox}(t_{si} - W_d)^2 + \in_{ox} t_{si}^2}(\phi_{gs} - \phi_0) + \frac{\in_{ox}}{2t_{si} \in_{si} t_{ox} - \in_{ox}(t_{si} - W_d)^2 + \in_{ox} t_{si}^2}(\phi_{gs} - \phi_0)y^2 \quad (4.9)$$

Putting $\phi(y)$ from (4.9) in (4.1A),

$$2t_{si} \in_{si} t_{ox} qN_a - \in_{ox}(t_{si} - W_d)^2 qN_a + \in_{ox} t_{si}^2 qN_a - 2 \in_{ox} \in_{si} (\phi_{gs} - \phi_0) = 0 \quad (4.10)$$

$$\text{Or, } W_d = t_{si} - \sqrt{\frac{2t_{si} \in_{si} t_{ox} qN_a + \in_{ox} t_{si}^2 qN_a - 2 \in_{ox} \in_{si} (\phi_{gs} - \phi_0)}{\in_{ox} qN_a}} \quad (4.11)$$

This is the depletion width of the for p-channel device

In a similar way the depletion width for an n-channel device can be obtained as,

$$W_d = t_{si} - \sqrt{\frac{2t_{si} \in_{si} t_{ox} qN_d + \in_{ox} t_{si}^2 qN_d + 2 \in_{ox} \in_{si} (\phi_{gs} - \phi_0)}{\in_{ox} qN_d}} \tag{4.12}$$

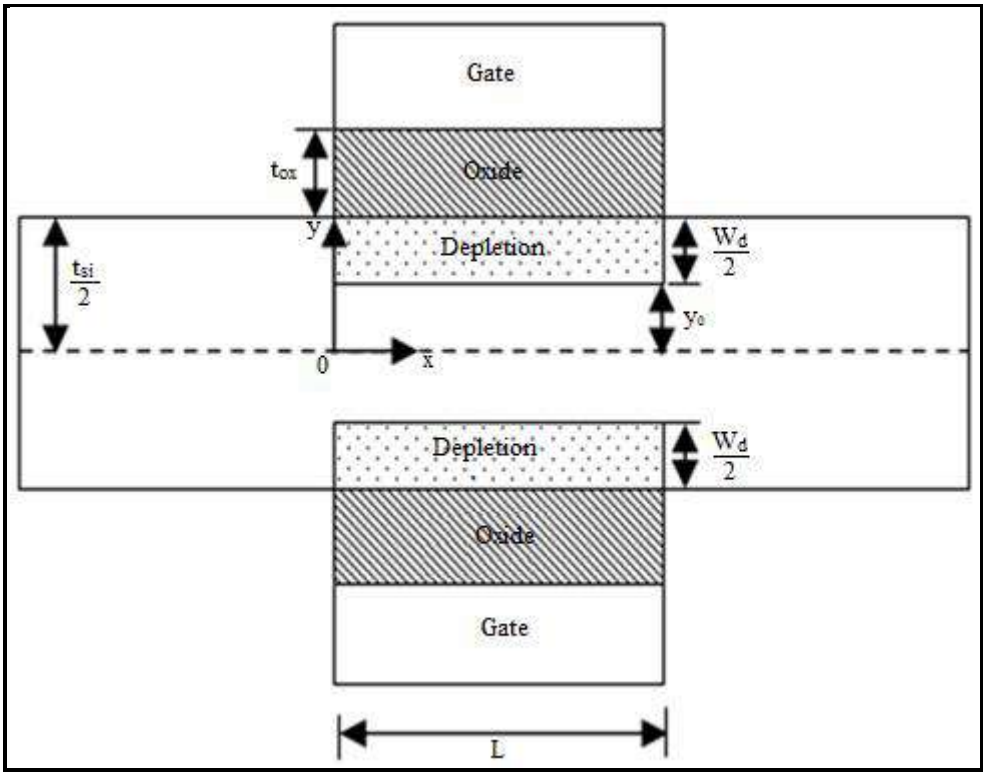

Fig. 4.2: Double Gate JLT

For Double Gate JLT,

at, $y = \frac{(t_{si} - W_d)}{2}$, the potential ϕ(y) can be written as,

$$\phi(y) = C_0 + C_2 \frac{(t_{si} - W_d)^2}{4} = \phi_0 \tag{4.13}$$

At, $y = \frac{t_{si}}{2}$

$$\frac{d\phi(y)}{dy} = t_{si}C_2 = \frac{\in_{ox}}{\in_{si} t_{ox}}(\phi_{gs} - \phi_s)$$

Or, $$C_2 = \frac{\in_{ox}}{t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s) \quad (4.14)$$

Therefore, $$C_0 = \phi_0 - C_2 \frac{(t_{si} - W_d)^2}{4} = \phi_0 - \frac{\in_{ox} (t_{si} - W_d)^2}{4 \in_{si} t_{si} t_{ox}}(\phi_{gs} - \phi_s) \quad (4.15)$$

$$\phi(y) = \phi_0 - \frac{\in_{ox} (t_{si} - W_d)^2}{4 \in_{si} t_{si} t_{ox}}(\phi_{gs} - \phi_s) + \frac{\in_{ox}}{t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s) y^2 \quad (4.16)$$

At $y = \frac{t_{si}}{2}$,

$$\phi(y) = \phi_s = \phi_0 - \frac{\in_{ox} (t_{si} - W_d)^2}{4 \in_{si} t_{si} t_{ox}}(\phi_{gs} - \phi_s) + \frac{\in_{ox}}{4t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s) t_{si}^2$$

Or, $$\phi_s = \phi_0 \frac{4 \in_{si} t_{si} t_{ox}}{4 \in_{si} t_{si} t_{ox} - \in_{ox} (t_{si} - W_d)^2 + \in_{ox} t_{si}^2} + \frac{\in_{ox} t_{si}^2 - \in_{ox} (t_{si} - W_d)^2}{4t_{si} \in_{si} t_{ox} - \in_{ox} (t_{si} - W_d)^2 + \in_{ox} t_{si}^2} \phi_{gs} \quad (4.17)$$

Putting ϕ_S from (4.17) in (4.16),

$$\phi(y) = \phi_0 - \frac{\in_{ox} (t_{si} - W_d)^2}{4 \in_{si} t_{si} t_{ox} - \in_{ox} (t_{si} - W_d)^2 + \in_{ox} t_{si}^2}(\phi_{gs} - \phi_0) + \frac{4 \in_{ox}}{4t_{si} \in_{si} t_{ox} - \in_{ox} (t_{si} - W_d)^2 + \in_{ox} t_{si}^2}(\phi_{gs} - \phi_0) y^2 \quad (4.18)$$

Putting $\phi(y)$ from (4.18) in (4.1A),

$$4t_{si} \in_{si} t_{ox} qN_a - \in_{ox} (t_{si} - W_d)^2 qN_a + \in_{ox} t_{si}^2 qN_a - 8 \in_{ox} \in_{si} (\phi_{gs} - \phi_0) = 0 \quad (4.19)$$

Solving equation (4.19), depletion width p-channel device can be obtained as,

$$W_d = t_{si} - \sqrt{\frac{4t_{si} \in_{si} t_{ox} qN_a + \in_{ox} t_{si}^2 qN_a - 8 \in_{ox} \in_{si} (\phi_{gs} - \phi_0)}{\in_{ox} qN_a}} \quad (4.20)$$

In a similar way the depletion width n-channel device can be obtained as,

$$W_d = t_{si} - \sqrt{\frac{4t_{si} \in_{si} t_{ox} qN_d + \in_{ox} t_{si}^2 qN_d + 8 \in_{ox} \in_{si} (\phi_{gs} - \phi_0)}{\in_{ox} qN_d}} \quad (4.21)$$

4.2.2 Results and Discussion

The depletion width variation with doping concentration, drain to source voltage, gate to source voltage and dielectric constant for n-channel single and double gate JLT is shown in Fig. 4.3, Fig. 4.5, Fig. 4.7 and Fig. 4.9. For p-channel single and double gate JLT is shown in Fig. 4.4, Fig. 4.6, Fig. 4.8 and Fig. 4.10. Depletion width for n-channel device decreases and p-channel device increases with increasing doping concentration and gate to source voltage. This is because the resultant of applied gate electric field and internal electric field is the difference between the two electric fields for n type device and the sum of the fields for p-type device for positive gate voltage. Hence a negative gate voltage has to be applied to turn on the p-type device. Depletion width for n-channel device increases and p-channel device decreases with increasing drain to source voltage. The drain to voltage also result in an electric field the direction of which is same as the direction of longitudinal electric field of n-type device and opposite in the case of a p-type device. However, depletion width for both n-channel and p-channel device increases with increase in dielectric constant of gate insulator due to increased capacitive coupling. For a single gate JLT the depletion width is found to be higher as compared to double gate device. In double gate device the lateral electric field in the central axis of the device is zero due to the cancellation of the two electric fields from the two gates.

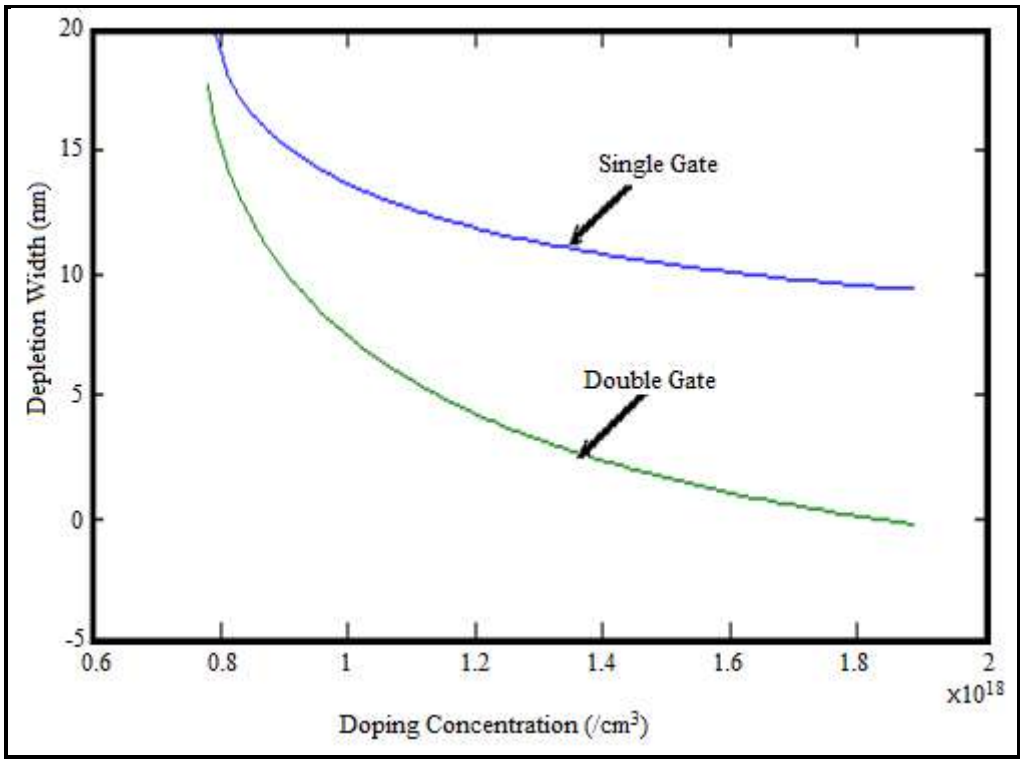

Fig. 4.3: Depletion Width variation with doping concentration for n-channel single gate and double gate JLT

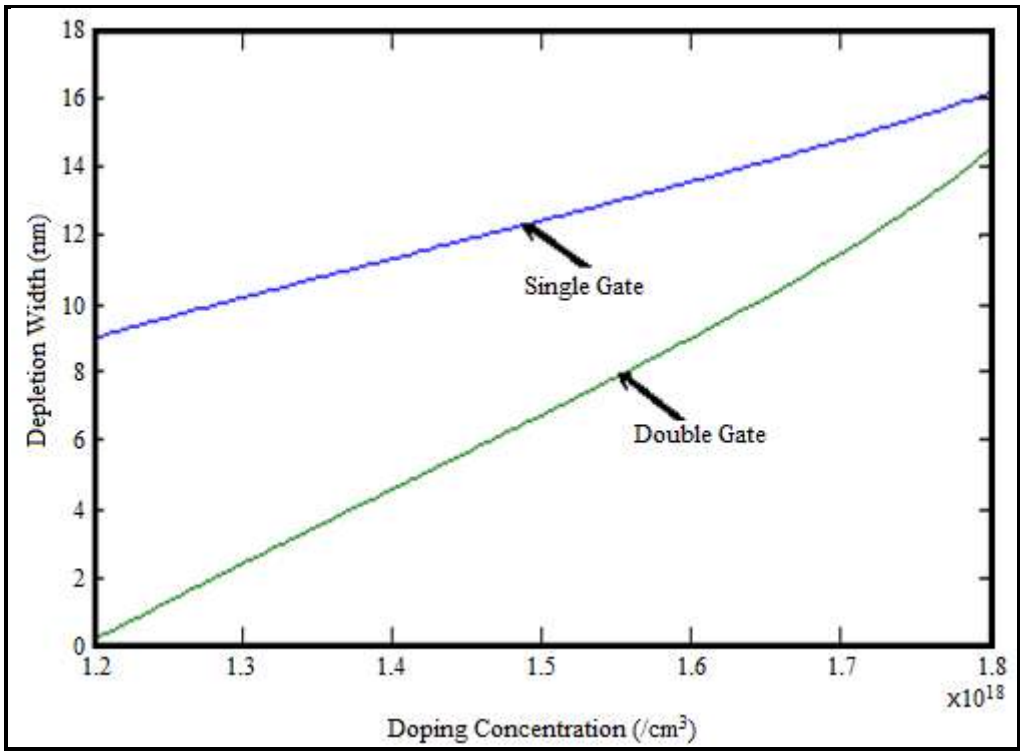

Fig. 4.4: Depletion Width variation with doping concentration for p-channel single gate and double gate JLT

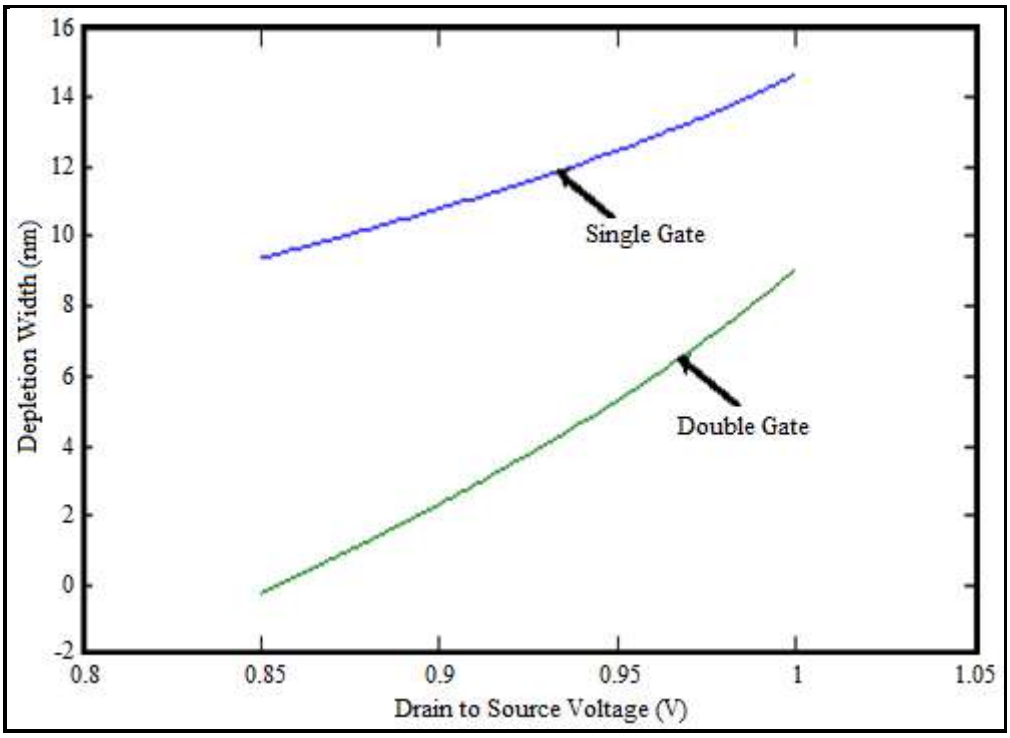

Fig. 4.5: Depletion Width variation with drain to source voltage for n-channel single gate and double gate JLT

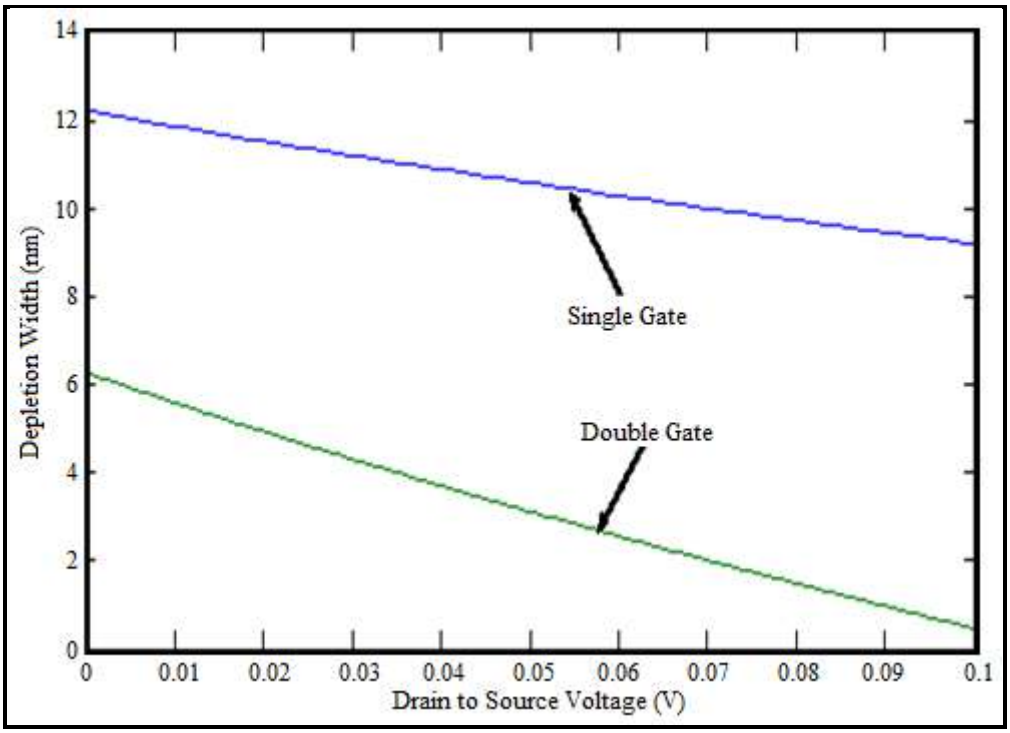

Fig. 4.6: Depletion Width variation with drain to source voltage for p-channel single gate and double gate JLT

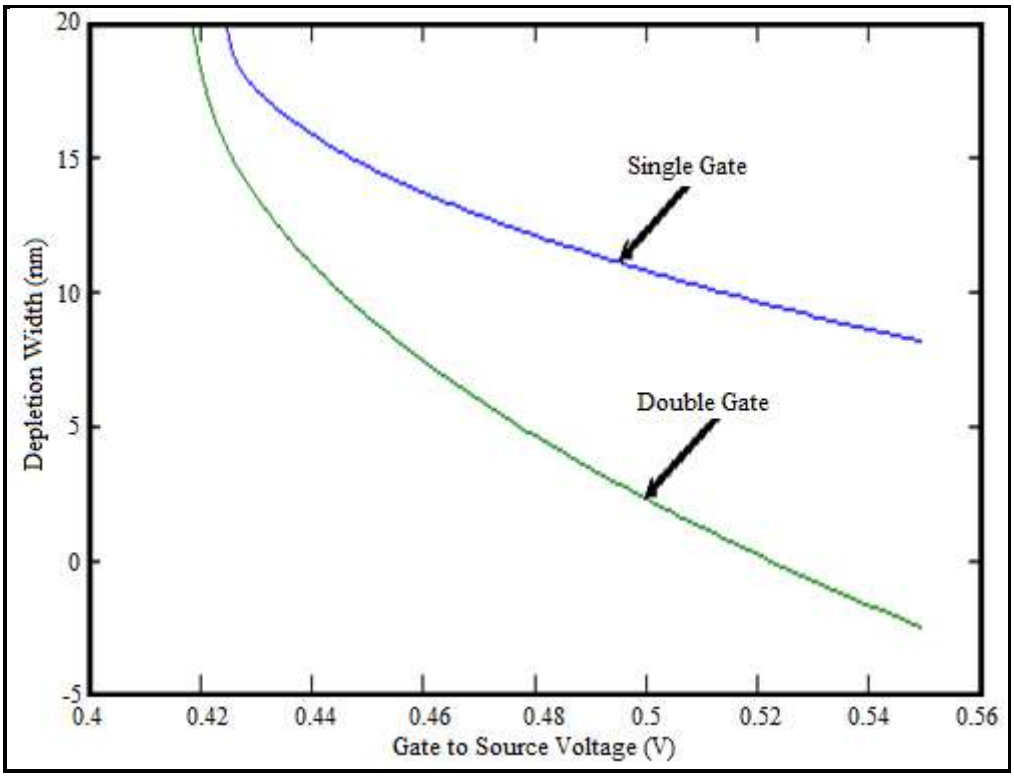

Fig. 4.7: Depletion Width variation with gate to source voltage for n-channel single gate and double gate JLT

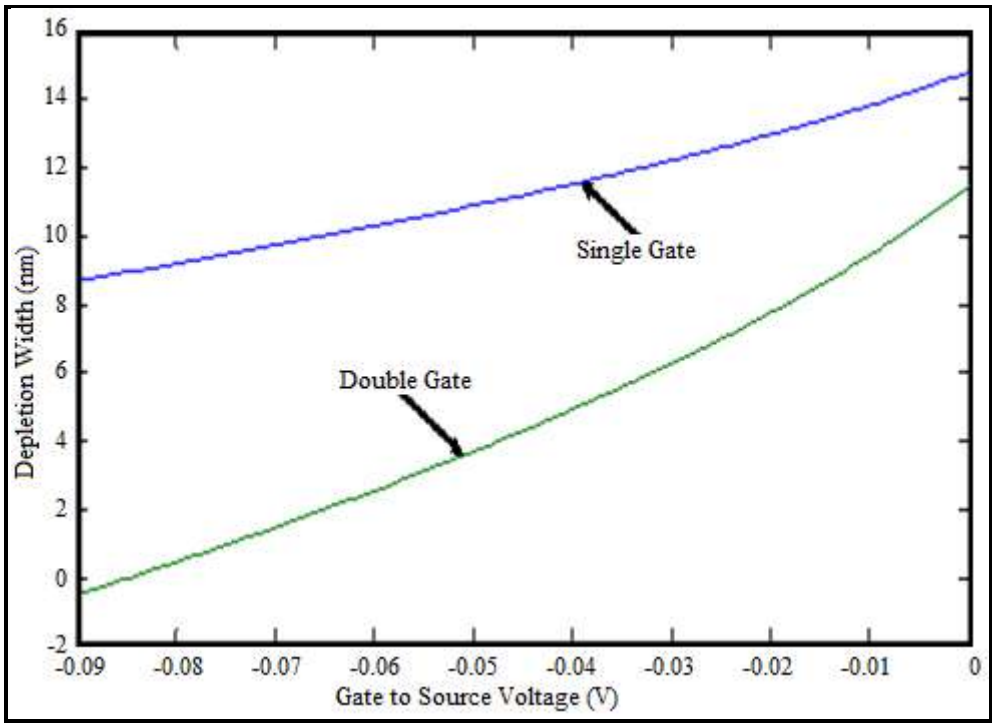

Fig. 4.8: Depletion Width variation with gate to source voltage for p-channel single gate and double gate JLT

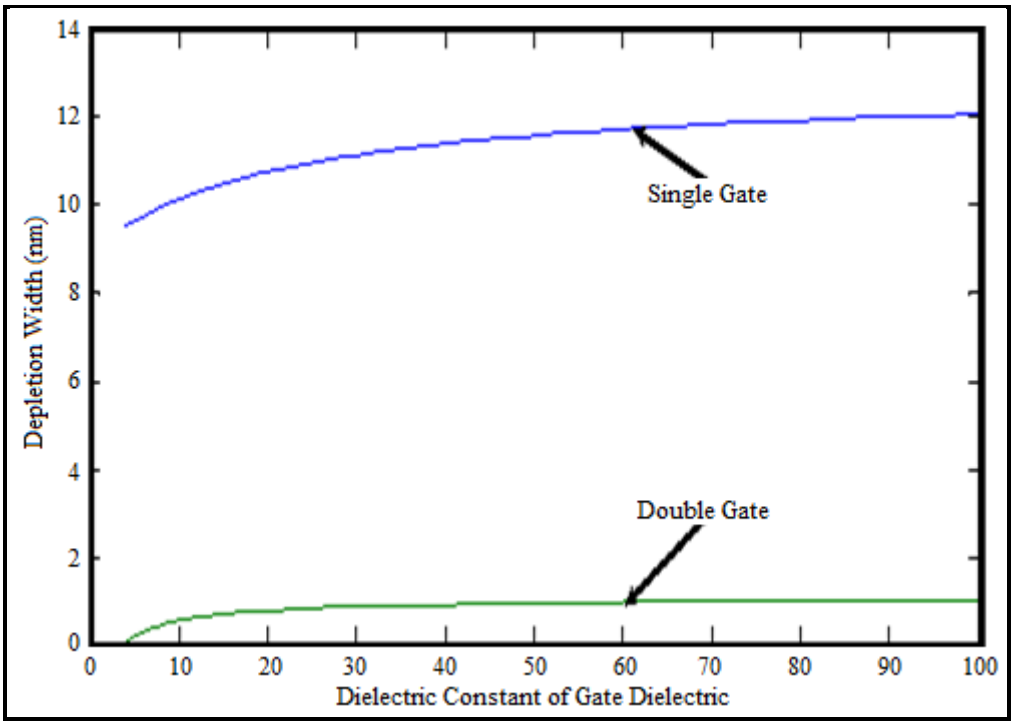

Fig. 4.9: Depletion Width variation with dielectric constant of gate dielectric for n-channel single gate and double gate JLT

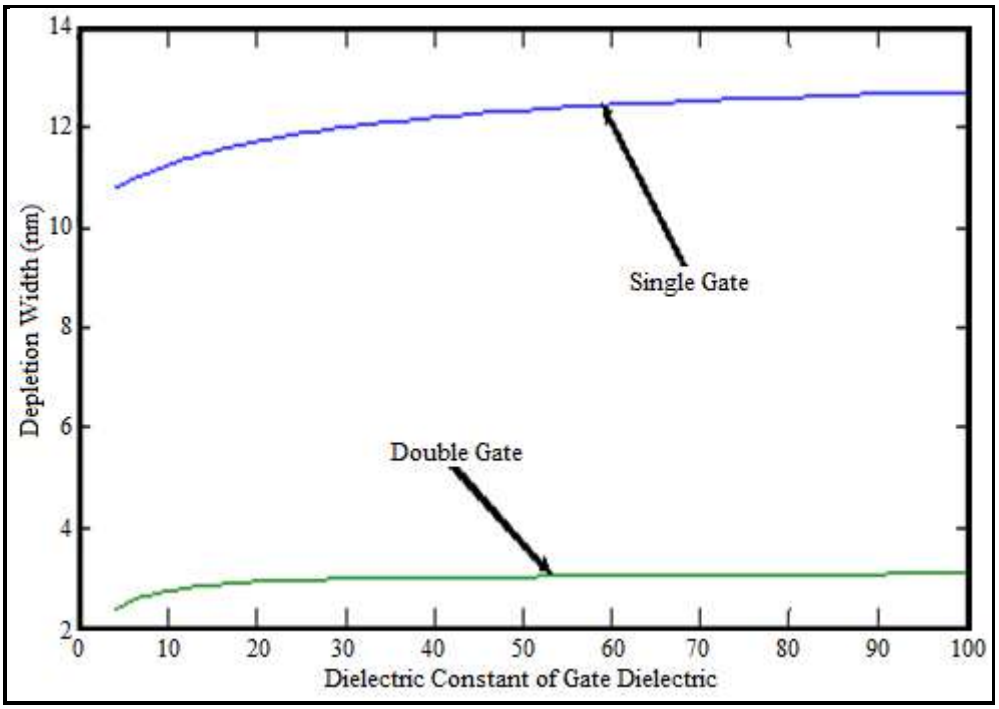

Fig. 4.10: Depletion Width variation with dielectric constant of gate dielectric for p-channel single gate and double gate JLT

4.3 Threshold Voltage Modelling of JLT

4.3.1 Mathematical Formulation

The threshold voltage model can be developed using the depletion width model. For a double gate n- channel JLT the depletion width expression obtained in section 4.2 is rewritten as ,

$$W_d = t_{si} - \sqrt{\frac{4t_{si} \in_{si} t_{ox} qN_d + \in_{ox} t_{si}^2 qN_d - 8 \in_{ox} \in_{si} (\phi_0 - \phi_{gs})}{\in_{ox} qN_d}} \tag{4.22}$$

ϕ_0 is the central potential along the channel length, which can be written as,

$$\phi_0(x) = \frac{\{V_{ds} + (\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs})\lambda^2\}e^{\frac{L}{\lambda}} - (\frac{qN_d}{\in_{si}} + \frac{1}{\lambda^2}\phi_{gs})\lambda^2}{(e^{2\frac{L}{\lambda}} - 1)} e^{\frac{x}{\lambda}}$$
$$- \frac{\{V_{ds} + (\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs})\lambda^2\}e^{\frac{L}{\lambda}} - (\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs})\lambda^2 e^{2\frac{L}{\lambda}}}{(e^{2\frac{L}{\lambda}} - 1)} e^{-\frac{x}{\lambda}}$$
$$-(\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs})\lambda^2 \tag{4.23}$$

Where, $\lambda = \sqrt{\frac{t_{si}(4 \in_{si} t_{ox} + \in_{ox} t_{si})}{8 \in_{ox}}}$ is the scale length

The threshold voltage can be defined as the maximum value of gate voltage at which the value of the depletion width is exactly equal to the Silicon layer thickness. Actually this is the maximum value of gate to source voltage from which the device starts conducting. For $V_{gs} < V_{Th}$ equation (4.22) gives imaginary value. Hence it is not valid in that region. In this

region actually the depletion width remains constant at its maximum value. This can be mathematically represented as,

At, $W_d = t_{si}, V_{gs} = V_{Th}$

From equation (4.22),

$$4t_{si} \in_{si} t_{ox} qN_d + \in_{ox} t_{si}^2 qN_d - 8 \in_{ox} \in_{si} (\phi_0^{/} - \phi_{gs}^{/}) = 0 \tag{4.24}$$

Where, $\phi_{gs}^{/} = V_{Th} - V_{fb}$ and

The central potential is,

$$\phi_0^{/}(x) = \frac{\{V_{ds} + (\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs}^{/})\lambda^2\}e^{\frac{L}{\lambda}} - (\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs}^{/})\lambda^2}{(e^{2\frac{L}{\lambda}} - 1)} e^{\frac{x}{\lambda}}$$
$$- \frac{\{V_{ds} + (\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs}^{/})\lambda^2\}e^{\frac{L}{\lambda}} - (\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs}^{/})\lambda^2 e^{2\frac{L}{\lambda}}}{(e^{2\frac{L}{\lambda}} - 1)} e^{-\frac{x}{\lambda}}$$
$$-(\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs}^{/})\lambda^2 \tag{4.25}$$

Solving (4.24) threshold voltage can be obtained

$$V_{Th}=\frac{\left[\begin{array}{l} 8\in_{ox}\in_{si}\left[\begin{array}{l} \frac{\{V_{ds}+(\frac{qN_d}{\in_{si}}+\frac{1}{\lambda^2}V_{fb})\lambda^2\}e^{\frac{L}{\lambda}}-(\frac{qN_d}{\in_{si}}+\frac{1}{\lambda^2}V_{fb})\lambda^2}{(e^{2\frac{L}{\lambda}}-1)}e^{\frac{x}{\lambda}} \\ -\frac{\{V_{ds}+(\frac{qN_d}{\in_{si}}+\frac{1}{\lambda^2}V_{fb})\lambda^2\}e^{\frac{L}{\lambda}}-(\frac{qN_d}{\in_{si}}+\frac{1}{\lambda^2}V_{fb})\lambda^2 e^{2\frac{L}{\lambda}}}{(e^{2\frac{L}{\lambda}}-1)}e^{-\frac{x}{\lambda}} \\ -(\frac{qN_d}{\in_{si}}+\frac{1}{\lambda^2}V_{fb})\lambda^2+V_{fb}\end{array}\right] \\ -4t_{si}\in_{si}t_{ox}qN_d-\in_{ox}t_{si}{}^2qN_d \end{array}\right]}{\left[\frac{(e^{\frac{L}{\lambda}}-1)e^{\frac{x}{\lambda}}+(e^{2\frac{L}{\lambda}}-e^{\frac{L}{\lambda}})e^{-\frac{x}{\lambda}}}{(e^{2\frac{L}{\lambda}}-1)}\right]8\in_{ox}\in_{si}} \quad (4.26)$$

The threshold voltage expression obtained in equation (4.26) is a function of 'x' and provides information about localized values of threshold voltage. However the threshold voltage of the device is the maximum value of V_{Th}. Mathematically, threshold voltage of the device is,

$V_T=\max(V_{Th})$

4.3.2 Results, Discussion and Validation

The physics based model developed in section 4.3.1 has been simulate in MATLAB simulation environment Result obtained in the simulation work has been compared with the simulation result obtained from Cogenda VisualTCAD 1.8.2 2D device simulator. All these simulation uses Fermi-Dirac statistics. The comparisons are shown in the figures as follows.

Fig. 4.11 shows the variation of threshold voltage with drain voltage. The threshold voltage increases almost linearly with drain voltage.

Fig. 4.12 and Fig. 4.13 shows the variation of threshold voltage with channel length for short channel and long channel JLT respectively. It is clear from the figure that for shorter device the threshold voltage is less.

Fig. 4.14 shows the variation of threshold voltage with doping concentration. At higher doping concentration the device turns on at a lower gate voltage.

Fig. 4.15 shows the variation of threshold voltage with channel thickness. At a higher channel thickness the control of gate at the middle of channel is less which causes a decrease in threshold voltage. The device may even turned on without the application of the gate voltage for a very high channel thickness.

Fig. 4.16 shows the variation of threshold voltage with gate oxide thickness. From the figure it is clear that gate loses control over the channel for thicker gate oxide. To achieve a suitable positive threshold voltage at a short channel the gate oxide and channel should be very thin. The model is in a close agreement with TCAD simulation results.

The advanced logic technologies have MOSFETs with multi threshold voltages- low threshold (thin oxide), high threshold (thick oxide) and regular threshold. As JLT is a MOS based device, multi threshold voltages can be achieved with JLT by varying the gate oxide thickness. However, threshold voltage of JLT is higher for thinner gate oxide. Thus for JLT the gate oxide should be thin for high threshold and thick for low threshold voltage.

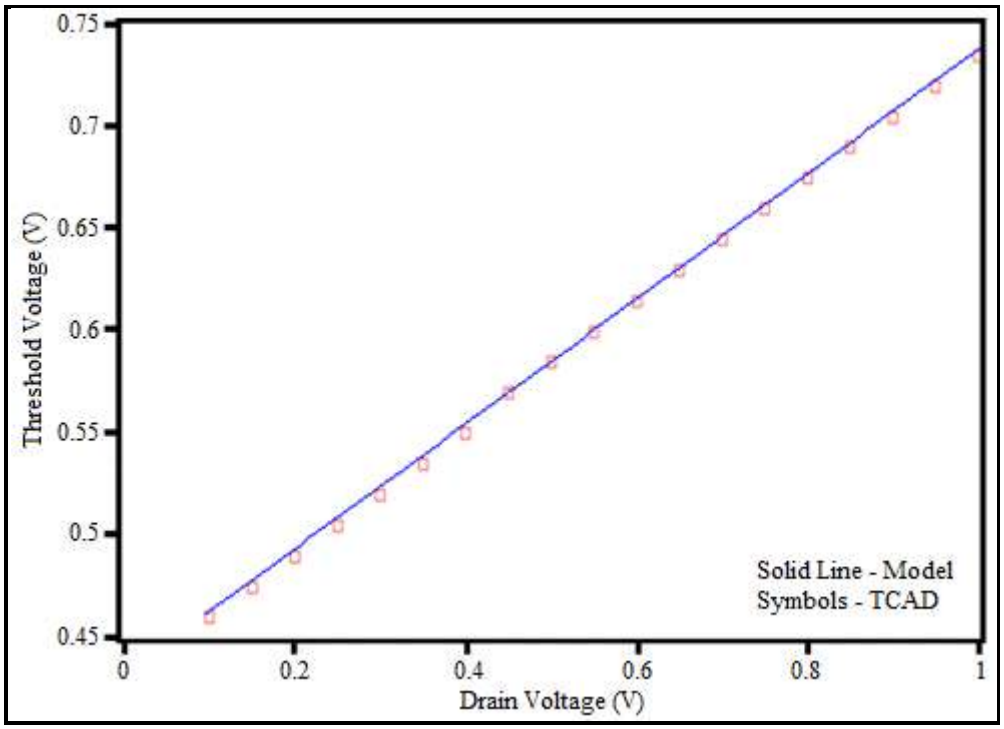

Fig. 4.11: Variation of Threshold Voltage with Drain Voltage

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm
Doping concentration (N_d)	$10^{19}/cm^3$

Average error = 1.1%
Maximum error =2.6%
Minimum error =0%

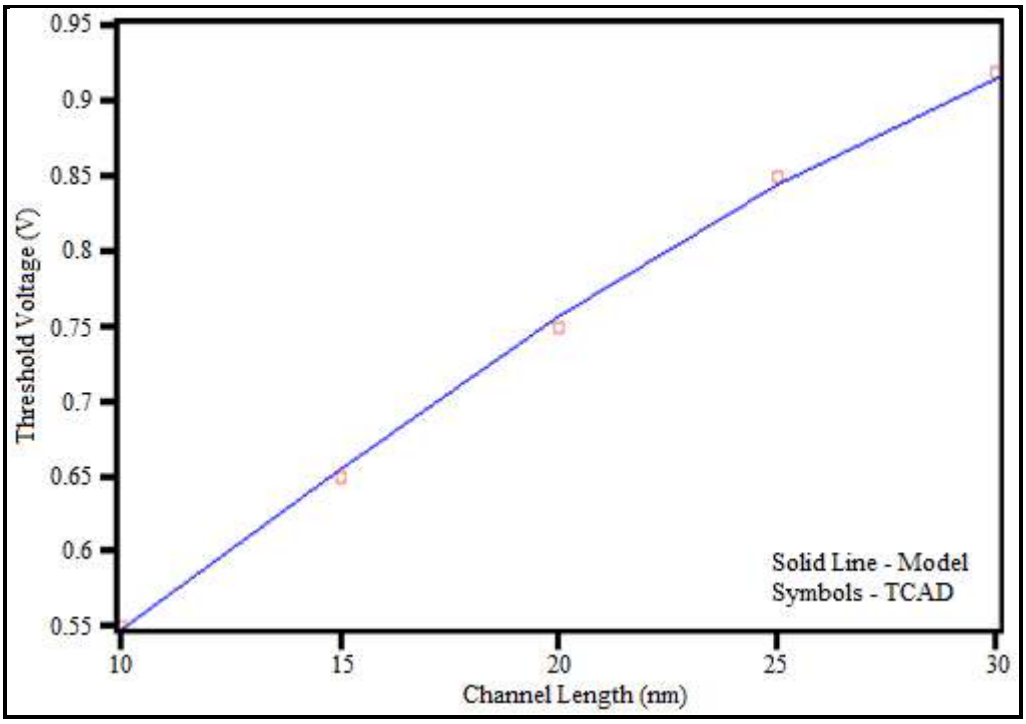

Fig. 4.12: Variation of Threshold Voltage with Channel Length (short channel)

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain Voltage (V_{ds})	0.1V
Doping concentration (N_d)	$10^{19}/cm^3$.

Average error = 1.5%
Maximum error =2.9%
Minimum error =0%

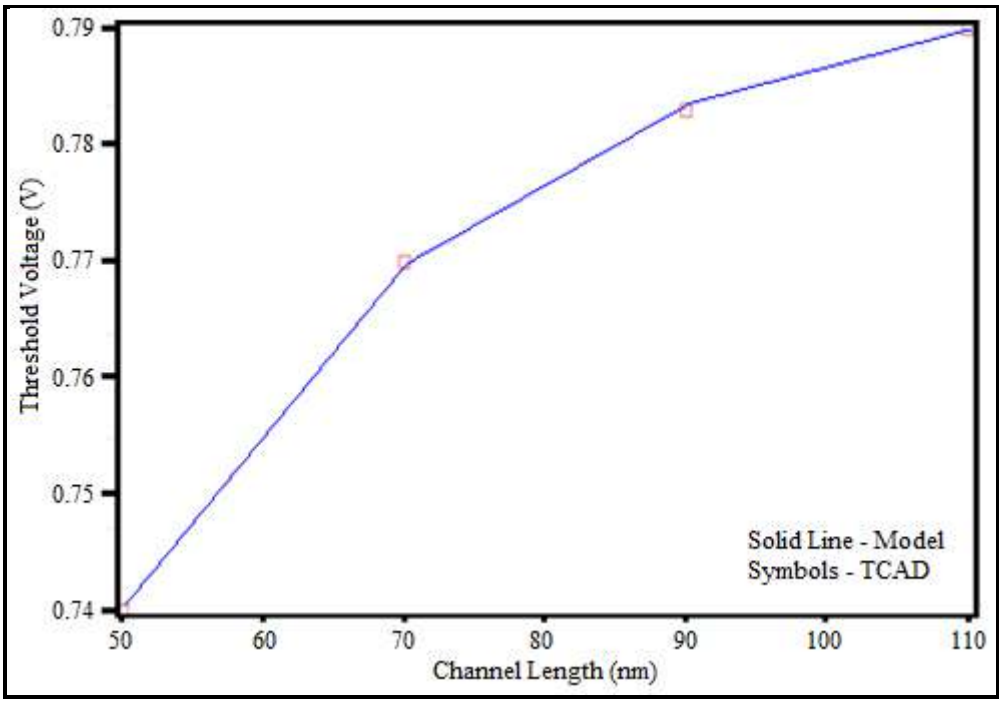

Fig. 4.13: Variation of Threshold Voltage with Channel Length (long channel)

Gate oxide thickness ($t_{ox)}$	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain Voltage (V_{ds})	0.1V
Doping concentration (N_d)	$10^{19}/cm^3$.

Average error = 0.5%
Maximum error =0.7%
Minimum error =0%

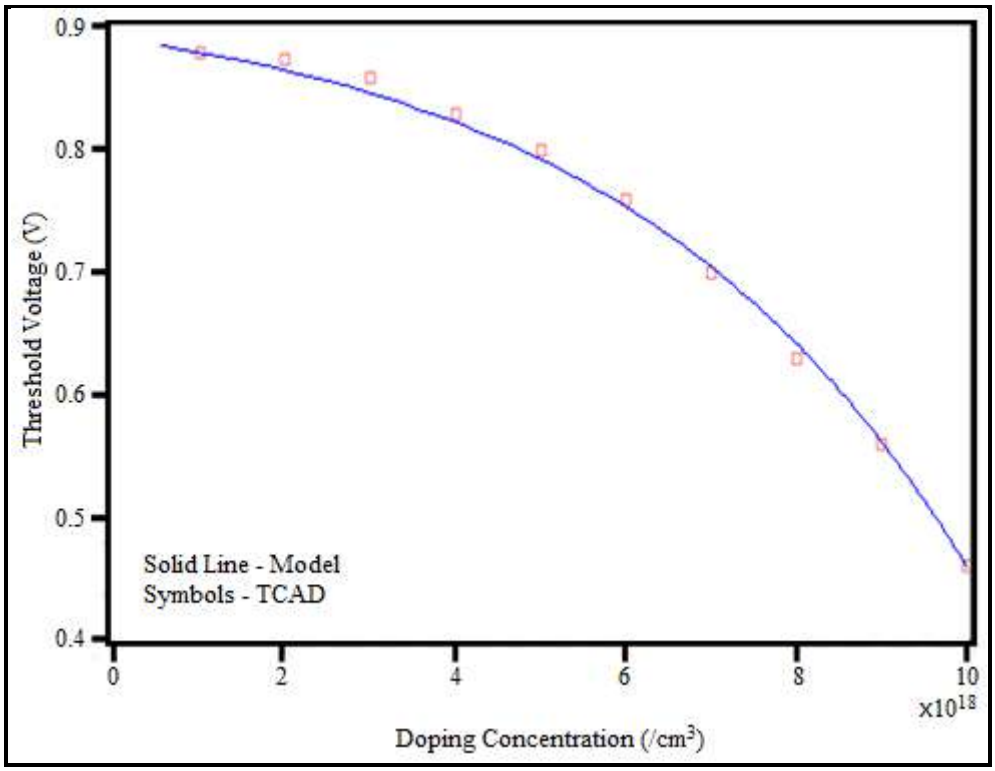

Fig. 4.14: Variation of Threshold Voltage with Doping Concentration

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm
Drain Voltage (V_{ds})	0.1V

Average error = 1.3%
Maximum error =3.1%
Minimum error =0%

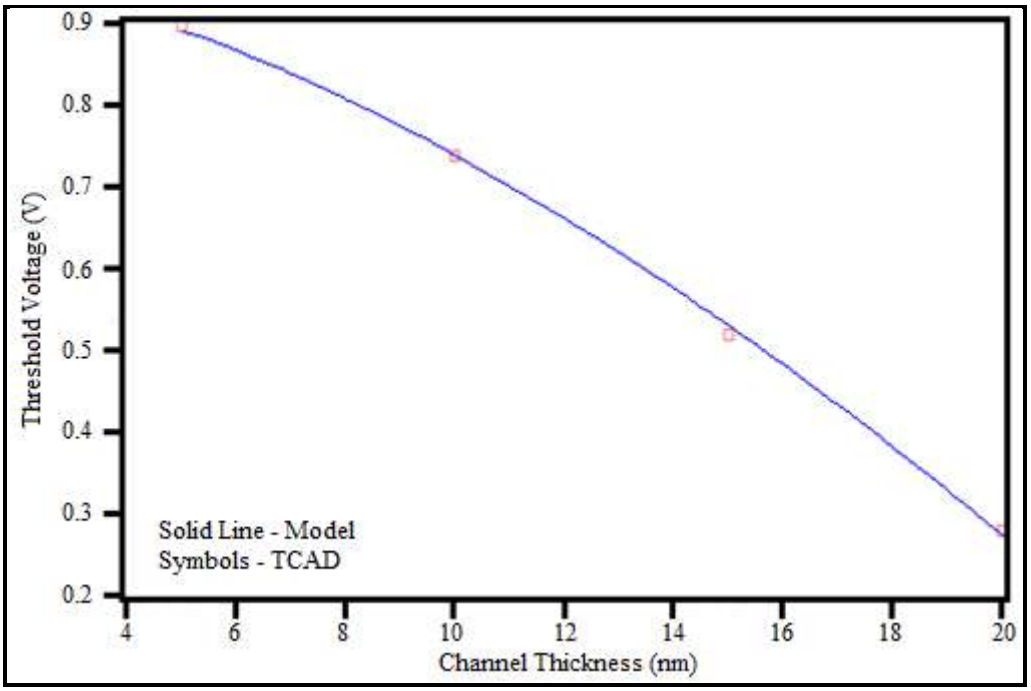

Fig. 4.15: Variation of Threshold Voltage with Channel Thickness

Gate oxide thickness (t_{ox})	2nm
Drain Voltage (V_{ds})	0.1V
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm
Doping concentration (N_d)	$10^{19}/cm^3$.

Average error = 1.9%
Maximum error =4%
Minimum error =0%

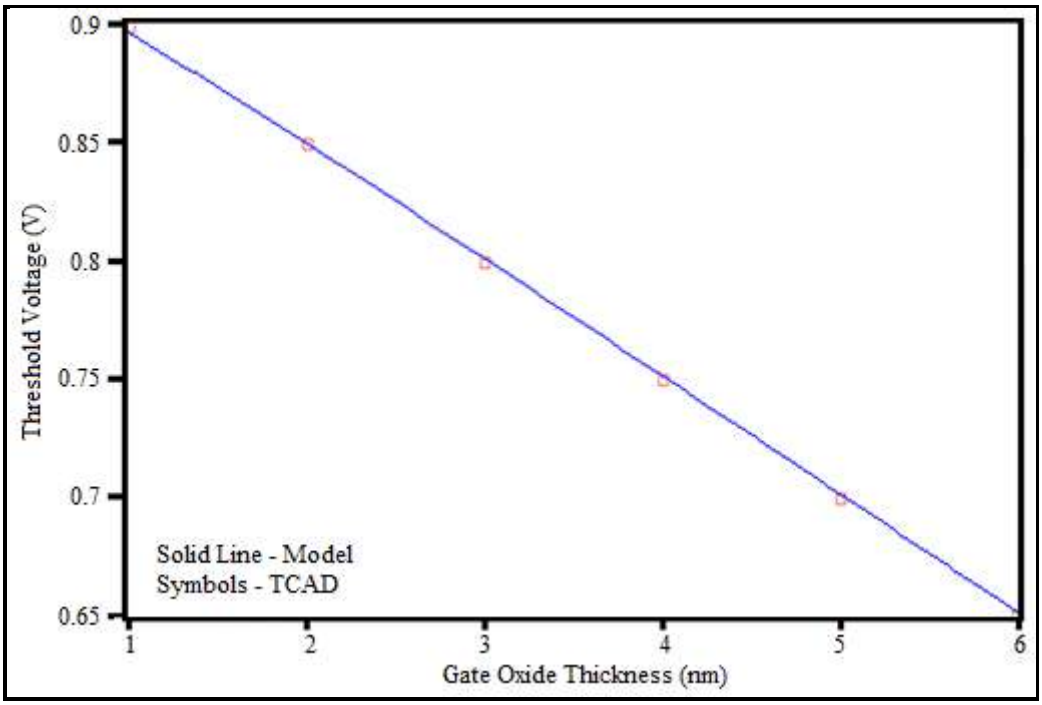

Fig. 4.16: Variation of Threshold Voltage with Gate Oxide Thickness

Drain Voltage (V_{ds})	0.1V
Channel thickness (t_{si})	10nm
Length of the source(Ls) and drain(L_d) region	5nm.
Channel length is (L)	20nm
Doping concentration (N_d)	$10^{19}/cm^3$.

Average error = 0.4%
Maximum error =0.6%
Minimum error =0%

4.4 Complete Potential Modelling of JLT

4.4.1 Channel Potential Modelling of DG JLT

In this part of the chapter, the modelling of the channel region which is directly under the influence of gate has been done. The cross-sectional view of a symmetric double gate JLT is shown in Fig. 4.2. The Poisson's equation for n-channel double gate JLT at a moderate doping concentration can be written as [19]

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = -\frac{qN_d}{\in_{si}} \tag{4.27}$$

Where,

$\phi(x,y)$ is the electrostatic potential

q is the charge of a carrier

N_d is the doping concentration

$\in_{si}$ is the permittivity of silicon.

One solution of Poisson's equation can be assumed as a parabolic function [20]

$$\phi(x,y) = C_0(x) + C_1(x)y + C_2(x)y^2 \tag{4.28}$$

The boundary conditions for double gate JLT can be used to determine the functions of 'x'.

For Double Gate JLT,

At $y = 0$,

$$\phi(x,y) = C_0(x) = \phi_0(x)$$

At $y = 0$,

$$\frac{d\phi(x,y)}{dy} = 0 = C_1(x)$$

At $y = \frac{t_{si}}{2}$, where, t_{si} is the silicon layer thickness,

$$\frac{d\phi(x,y)}{dy} = C_1(x) + t_{si}C_2(x) = \frac{\in_{ox}}{\in_{si} t_{ox}}(\phi_{gs} - \phi_s)$$

Or, $C_2(x) = \frac{\in_{ox}}{t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s)$ (4.29)

Where,

ϕ_s is the surface potential

$\in_{ox}$ is the permittivity of the gate oxide

t_{ox} is the gate oxide thickness

$\phi_{gs} = V_{gs} - V_{fb}$

where,

V_{gs} is the gate to source voltage

V_{fb} is the flat band voltage.

Therefore,

$$\phi(x,y) = \phi_0(x) + \frac{\in_{ox}}{t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s)y^2 \quad (4.30)$$

At $y = \frac{t_{si}}{2}$, from (4.30),

$$\phi(x,y) = \phi_s = \phi_0(x) + \frac{\in_{ox}}{t_{si}\ \in_{si}\ t_{ox}}(\phi_{gs} - \phi_s)\frac{t_{si}}{4}^2 \tag{4.31}$$

$$\phi_s(1 + \frac{\in_{ox}\ t_{si}}{4 \in_{si}\ t_{ox}}) = \phi_0(x) + \frac{\in_{ox}\ t_{si}}{4 \in_{si}\ t_{ox}}\phi_{gs}$$

$$\phi_s(\frac{4 \in_{si}\ t_{ox} + \in_{ox}\ t_{si}}{4 \in_{si}\ t_{ox}}) = \phi_0(x) + \frac{\in_{ox}\ t_{si}}{4 \in_{si}\ t_{ox}}\phi_{gs}$$

Or, $\phi_s = \phi_0(x)\frac{4 \in_{si}\ t_{ox}}{4 \in_{si}\ t_{ox} + \in_{ox}\ t_{si}} + \frac{\in_{ox}\ t_{si}}{4 \in_{si}\ t_{ox} + \in_{ox}\ t_{si}}\phi_{gs}$ (4.32)

From (4.32) putting ϕ_s in (4.30),

$$\phi(x,y) = \phi_0(x) + \frac{4 \in_{ox}}{t_{si}(4t_{ox}\ \in_{si} + t_{si}\ \in_{ox})}\{\phi_{gs} - \phi_0(x)\}y^2 \tag{4.33}$$

Putting $\phi(x,y)$ from (4.33) in (4.27) and $y = 0$,

$$\frac{d^2\phi_0(x)}{dx^2} + \frac{1}{\lambda^2}\{\phi_{gs} - \phi_0(x)\} = -\frac{qN_d}{\in_{si}} \tag{4.34}$$

Where, $\lambda = \sqrt{\frac{t_{si}(4t_{ox}\ \in_{si} + t_{si}\ \in_{ox})}{8 \in_{ox}}}$ is the scale length of the device [21-24].

(4.34) can also be written as,

$$\frac{d^2\phi_0(x)}{dx^2} - \frac{1}{\lambda^2}\phi_0(x) = C \tag{4.35}$$

Where, $C = -\frac{qN_d}{\in_{si}} - \frac{1}{\lambda^2}\phi_{gs}$

One solution of (4.35) will be of the form [20],

$$\phi_0(x) = Ae^{\frac{x}{\lambda}} - Be^{-\frac{x}{\lambda}} - C\lambda^2 \tag{4.36}$$

Where, A and B are constants that can be determined by boundary conditions. Influence of gate electric field on source and drain regions are taken into account while assessing the boundary conditions.

At $x = -L_s$, where L_s is the source length,

$$\phi_0(x) = Ae^{\frac{x}{\lambda}} - Be^{-\frac{x}{\lambda}} - C\lambda^2 = 0$$

Or, $$Ae^{-\frac{L_s}{\lambda}} - Be^{\frac{L_s}{\lambda}} = C\lambda^2 \tag{4.37}$$

$$B = \frac{(Ae^{-\frac{L_s}{\lambda}} - C\lambda^2)}{e^{\frac{L_s}{\lambda}}} = Ae^{-2\frac{L_s}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}$$

At $x = L + L_d$, where L_d is the drain length and L is the channel length,

$$Ae^{\frac{L+L_d}{\lambda}} - Be^{-\frac{L+L_d}{\lambda}} = V_{ds} + C\lambda^2$$

$$A(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}}) = (V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}} \tag{4.38}$$

From (4.37) and (4.38),

$$A = \frac{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}$$

$$B = \frac{\{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})e^{-\frac{L_s}{\lambda}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}$$

Therefore,

$$\phi_0(x) = \left[\frac{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}e^{\frac{x}{\lambda}}\right] - \left[\frac{\{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})e^{-\frac{L_s}{\lambda}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}e^{-\frac{x}{\lambda}}\right] - C\lambda^2 \quad (4.39)$$

4.4.2 Source-Drain Potential Modelling of DG JLT

In the source and drain region, the Poisson's equation can be written as [19],

$$\frac{d^2\phi_0(x)}{dx^2} = -\frac{qN_d}{\in_{si}} \quad (4.40)$$

A solution of (4.40) can be written as [20],

$$\phi_0(x) = ax^2 + bx + c \quad (4.41)$$

Where, $a = -\frac{qN_d}{\in_{si}}$, b and c are constants related to the boundary conditions. The boundary conditions for (4.41) can be derived from potential expression of (4.39).

At $x = 0$, from (4.39)

$$c = \phi_0(0) = \left[\frac{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})} \right] -$$

$$\left[\frac{\{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})e^{\frac{L_s}{\lambda}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})} \right] - C\lambda^2 \quad (4.42)$$

At $x = L$, from(4.39)

$$aL^2 + bL + c = \left[\frac{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})} e^{\frac{L}{\lambda}} \right] -$$

$$\left[\frac{\{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})e^{\frac{L_s}{\lambda}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})} e^{-\frac{L}{\lambda}} \right] - C\lambda^2$$

or,

$$b = \left[\frac{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}(e^{\frac{L}{\lambda}} - 1) - \frac{\{(V_{ds} + C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})e^{\frac{L_s}{\lambda}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}(e^{-\frac{L}{\lambda}} - 1) \right] / L + \frac{qN_d}{2 \in_{si}} L^2$$

$$\phi_{0sd}(x) = -\frac{qN_d}{2\in_{si}}x^2 + \left[\frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}(e^{\frac{L}{\lambda}}-1) - \frac{\{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})e^{\frac{L_s}{\lambda}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}(e^{-\frac{L}{\lambda}}-1)\right]\frac{x}{L} + \frac{qN_d}{2\in_{si}}L^2 + \left[\frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}\right] - \left[\frac{\{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\}e^{-2\frac{L_s}{\lambda}} - C\lambda^2(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})e^{\frac{L_s}{\lambda}}}{(e^{2\frac{L+L_d}{\lambda}} - e^{-2\frac{L_s}{\lambda}})}\right] - C\lambda^2 \quad (4.43)$$

Equation (4.39) is valid for channel only and (4.43) is valid for source and drain only.

4.4.3 Channel Potential Modelling of Tri-gate JLT

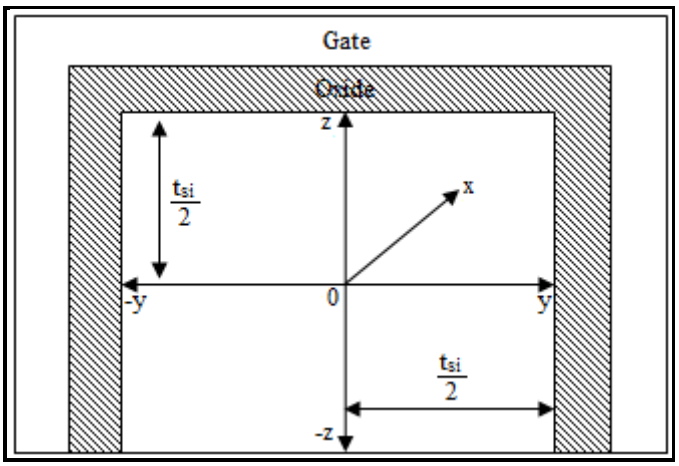

Fig. 4.17: Cross sectional view of a tri-gate JLT

The Poisson's equation for n-channel tri-gate JLT at a moderate doping concentration can be written as [19]

$$\frac{\partial^2\phi(x,y,z)}{\partial x^2}+\frac{\partial^2\phi(x,y,z)}{\partial y^2}+\frac{\partial^2\phi(x,y,z)}{\partial z^2}=-\frac{qN_d}{\in_{si}} \tag{4.44}$$

Where,

$\phi(x,y,z)$ is the electrostatic potential

q is the charge of a carrier

N_d is the doping concentration

$\in_{si}$ is the permittivity of silicon.

One solution of Poisson's equation can be assumed as a parabolic function [20]

$$\phi(x,y,z)=C_0(x)+C_1(x)y+C_2(x)y^2+C_0'(x)+C_1'(x)z+C_2'(x)z^2 \tag{4.45}$$

The boundary conditions for tri-gate JLT can be used to determine the functions of 'x'.

For tri-Gate JLT,

At y=0, z=0,

$$\phi(x,y,z) = C_0(x) + C_0'(x) = \phi_0(x)$$

At y=0, z=0

$$\frac{d\phi(x,y,z)}{dy} = 0 = C_1(x)$$

At $y = \frac{t_{si}}{2}$, where, t_{si} is the silicon layer thickness,

$$\frac{d\phi(x,y,z)}{dy} = C_1(x) + t_{si}C_2(x) = \frac{\in_{ox}}{\in_{si} t_{ox}}(\phi_{gs} - \phi_s)$$

Or, $C_2(x) = \frac{\in_{ox}}{t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s)$ (4.46)

Where,

ϕ_s is the surface potential

$\in_{ox}$ is the permittivity of the gate oxide

t_{ox} is the gate oxide thickness

$\phi_{gs} = V_{gs} - V_{fb}$

where,

V_{gs} is the gate to source voltage

V_{fb} is the flat band voltage.

At y=0, z=0

$$\frac{d\phi(x,y,z)}{dy} = 0 = C_1(x)$$

At $z = \frac{t_{si}}{2}$, y=0, where, t_{si} is the silicon layer thickness,

$$\frac{d\phi(x,y,z)}{dz} = C_1'(x) + t_{si}C_2'(x) = \frac{\in_{ox}}{\in_{si} t_{ox}}(\phi_{gs} - \phi_s) \tag{4.47}$$

At $z = -\frac{t_{si}}{2}$, y=0,

$$\frac{d\phi(x,y,z)}{dz} = C_1'(x) - t_{si}C_2'(x) = 0 \tag{4.48}$$

Solving (4.47) and (4.48),

$$C_1'(x) = \frac{\in_{ox}}{2 \in_{si} t_{ox}}(\phi_{gs} - \phi_s)$$

and

$$C_2'(x) = \frac{\in_{ox}}{2t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s)$$

Therefore,

$$\phi(x,y,z) = \phi_0(x) + \frac{\in_{ox}}{t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s)y^2 + \frac{\in_{ox}}{2 \in_{si} t_{ox}}(\phi_{gs} - \phi_s)z + \frac{\in_{ox}}{2t_{si} \in_{si} t_{ox}}(\phi_{gs} - \phi_s)z^2 \tag{4.49}$$

At $y = \frac{t_{si}}{2}$, z=0 , from (4.49),

$$\phi(x,y,z) = \phi_s = \phi_0(x) + \frac{\in_{ox}}{t_{si} \in_{si} t_{ox}} (\phi_{gs} - \phi_s) \frac{t_{si}}{4}^2 \tag{4.50}$$

$$\phi_s (1 + \frac{\in_{ox} t_{si}}{4 \in_{si} t_{ox}}) = \phi_0(x) + \frac{\in_{ox} t_{si}}{4 \in_{si} t_{ox}} \phi_{gs}$$

$$\phi_s (\frac{4 \in_{si} t_{ox} + \in_{ox} t_{si}}{4 \in_{si} t_{ox}}) = \phi_0(x) + \frac{\in_{ox} t_{si}}{4 \in_{si} t_{ox}} \phi_{gs}$$

Or, $\phi_s = \phi_0(x) \frac{4 \in_{si} t_{ox}}{4 \in_{si} t_{ox} + \in_{ox} t_{si}} + \frac{\in_{ox} t_{si}}{4 \in_{si} t_{ox} + \in_{ox} t_{si}} \phi_{gs}$ (4.51)

From (4.51) putting ϕ_s in (4.50),

$$\phi(x,y,z) = \phi_0(x) + \frac{4 \in_{ox}}{t_{si}(4 t_{ox} \in_{si} + t_{si} \in_{ox})} (\phi_{gs} - \phi_s) y^2 + \frac{2 \in_{ox}}{4 \in_{si} t_{ox} + \in_{ox} t_{si}} (\phi_{gs} - \phi_0(x)) z + \frac{2 \in_{ox}}{t_{si}(4 \in_{si} t_{ox} + \in_{ox} t_{si})} (\phi_{gs} - \phi_s) z^2 \tag{4.52}$$

Putting $\phi(x,y,z)$ from (4.52) in (4.44) and y=0, z=0,

$$\frac{d^2 \phi_0(x)}{dx^2} + \frac{1}{\lambda_1^2} \{\phi_{gs} - \phi_0(x)\} = -\frac{qN_d}{\in_{si}} \tag{4.53}$$

Where, $\lambda_1 = \sqrt{\frac{t_{si}(4 t_{ox} \in_{si} + t_{si} \in_{ox})}{12 \in_{ox}}}$ is the scale length of the device [21-24].

(4.53) can also be written as,

$$\frac{d^2\phi_0(x)}{dx^2} - \frac{1}{\lambda_1^2}\phi_0(x) = C \tag{4.54}$$

Where, $C = -\frac{qN_d}{\in_{si}} - \frac{1}{\lambda_1^2}\phi_{gs}$

One solution of (4.54) will be of the form [20],

$$\phi_0(x) = Ae^{\frac{x}{\lambda_1}} - Be^{-\frac{x}{\lambda_1}} - C\lambda_1^2 \tag{4.55}$$

Where, A and B are constants that can be determined by boundary conditions. Influence of gate electric field on source and drain regions are taken into account while assessing the boundary conditions.

At $x = -L_s$, where, L_s is the source length,

$$\phi_0(x) = Ae^{\frac{x}{\lambda_1}} - Be^{-\frac{x}{\lambda_1}} - C\lambda_1^2 = 0$$

Or, $Ae^{-\frac{L_s}{\lambda_1}} - Be^{\frac{L_s}{\lambda_1}} = C\lambda_1^2$ (4.56)

$$B = \frac{(Ae^{-\frac{L_s}{\lambda_1}} - C\lambda_1^2)}{e^{\frac{L_s}{\lambda_1}}} = Ae^{-2\frac{L_s}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_s}{\lambda_1}}}$$

At $x = L + L_d$, where L_d is the drain length and L is the channel length,

$$Ae^{\frac{L+L_d}{\lambda_1}} - Be^{-\frac{L+L_d}{\lambda_1}} = V_{ds} + C\lambda_1^2$$

$$A(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}}) = (V_{ds} + C\lambda_1^2)e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_s}{\lambda_1}}} \tag{4.57}$$

From (4.56) and (4.57),

$$A = \frac{(V_{ds} + C\lambda_1^2)e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_s}{\lambda_1}}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}$$

$$B = \frac{\{(V_{ds} + C\lambda_1^2)e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_s}{\lambda_1}}}\}e^{-2\frac{L_s}{\lambda_1}} - C\lambda_1^2(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})e^{\frac{L_s}{\lambda_1}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}$$

Therefore,

$$\phi_{0ch}(x) = \left[\frac{(V_{ds} + C\lambda_1^2)e^{\frac{L+L_d}{\lambda}} - \frac{C\lambda_1^2}{e^{\frac{L_s}{\lambda_1}}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}e^{\frac{x}{\lambda_1}}\right] -$$

$$\left[\frac{\{(V_{ds} + C\lambda_1^2)e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_s}{\lambda_1}}}\}e^{-2\frac{L_s}{\lambda_1}} - C\lambda_1^2(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})e^{\frac{L_s}{\lambda_1}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}e^{-\frac{x}{\lambda_1}}\right] - C\lambda_1^2 \tag{4.58}$$

4.4.4 Source-Drain Potential Modelling of Tri-gate JLT

In the source and drain region, the Poisson's equation can be written as [19],

$$\frac{d^2\phi_0(x)}{dx^2} = -\frac{qN_d}{\in_{si}} \tag{4.59}$$

A solution of (4.59) can be written as [20],

$$\phi_0(x) = ax^2 + bx + c \tag{4.60}$$

Where, $a = -\frac{qN_d}{\in_{si}}$, b and c are constants related to the boundary conditions. The boundary conditions for (4.60) can be derived from potential expression of (4.58).

At $x = 0$, from (4.58)

$$c = \phi_0(0) = \left[\frac{(V_{ds} + C\lambda_1^2)e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_s}{\lambda_1}}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}\right] - \left[\frac{\{(V_{ds} + C\lambda_1^2)e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^2}{e^{\frac{L_s}{\lambda_1}}}\}e^{-2\frac{L_s}{\lambda_1}} - C\lambda_1^2(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})e^{\frac{L_s}{\lambda_1}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}\right] - C\lambda_1^2 \tag{4.61}$$

At $x = L$, from(4.58)

$$aL^2+bL+c=\left[\frac{(V_{ds}+C\lambda_1^{\,2})e^{\frac{L+L_d}{\lambda_1}}-\frac{C\lambda_1^{\,2}}{e^{\frac{L_s}{\lambda_1}}}}{(e^{2\frac{L+L_d}{\lambda_1}}-e^{-2\frac{L_s}{\lambda_1}})}e^{\frac{L}{\lambda_1}}\right]-$$

$$\left[\frac{\{(V_{ds}+C\lambda_1^{\,2})e^{\frac{L+L_d}{\lambda_1}}-\frac{C\lambda_1^{\,2}}{e^{\frac{L_s}{\lambda_1}}}\}e^{-2\frac{L_s}{\lambda_1}}-C\lambda_1^{\,2}(e^{2\frac{L+L_d}{\lambda_1}}-e^{-2\frac{L_s}{\lambda_1}})e^{\frac{L_s}{\lambda_1}}}{(e^{2\frac{L+L_d}{\lambda_1}}-e^{-2\frac{L_s}{\lambda_1}})}e^{-\frac{L}{\lambda_1}}\right]-C\lambda_1^{\,2}$$

or,

$$b=\left[\frac{(V_{ds}+C\lambda_1^{\,2})e^{\frac{L+L_d}{\lambda_1}}-\frac{C\lambda_1^{\,2}}{e^{\frac{L_s}{\lambda_1}}}}{(e^{2\frac{L+L_d}{\lambda_1}}-e^{-2\frac{L_s}{\lambda_1}})}(e^{\frac{L}{\lambda_1}}-1)-\right.$$

$$\left.\frac{\{(V_{ds}+C\lambda_1^{\,2})e^{\frac{L+L_d}{\lambda_1}}-\frac{C\lambda_1^{\,2}}{e^{\frac{L_s}{\lambda_1}}}\}e^{-2\frac{L_s}{\lambda_1}}-C\lambda_1^{\,2}(e^{2\frac{L+L_d}{\lambda_1}}-e^{-2\frac{L_s}{\lambda_1}})e^{\frac{L_s}{\lambda_1}}}{(e^{2\frac{L+L_d}{\lambda_1}}-e^{-2\frac{L_s}{\lambda_1}})}(e^{-\frac{L}{\lambda_1}}-1)\right]/L$$

$$+\frac{qN_d}{2\in_{si}}L^2$$

$$\phi_{0sd}(x) = -\frac{qN_d}{2\in_{si}}x^2 +$$

$$\left[\frac{(V_{ds}+C\lambda_1^{\,2})e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^{\,2}}{e^{\frac{L_s}{\lambda_1}}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}(e^{\frac{L}{\lambda_1}}-1) - \frac{\{(V_{ds}+C\lambda_1^{\,2})e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^{\,2}}{e^{\frac{L_s}{\lambda_1}}}\}e^{-2\frac{L_s}{\lambda_1}} - C\lambda_1^{\,2}(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})e^{\frac{L_s}{\lambda_1}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}(e^{-\frac{L}{\lambda_1}}-1)\right]\frac{x}{L}$$

$$+\frac{qN_d}{2\in_{si}}L^2$$

$$+\left[\frac{(V_{ds}+C\lambda_1^{\,2})e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^{\,2}}{e^{\frac{L_s}{\lambda_1}}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}\right] -$$

$$\left[\frac{\{(V_{ds}+C\lambda_1^{\,2})e^{\frac{L+L_d}{\lambda_1}} - \frac{C\lambda_1^{\,2}}{e^{\frac{L_s}{\lambda_1}}}\}e^{-2\frac{L_s}{\lambda_1}} - C\lambda_1^{\,2}(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})e^{\frac{L_s}{\lambda_1}}}{(e^{2\frac{L+L_d}{\lambda_1}} - e^{-2\frac{L_s}{\lambda_1}})}\right] - C\lambda_1^{\,2}$$

(4.62)

4.4.3 Result, Discussion and Validation

In Fig. 4.18 scale length dependence on the dielectric constant of the gate dielectric and silicon layer thickness of the DGJLT is shown. The dielectrics considered here are SiO_2, Al_2O_3 and HfO_2 with dielectric constants 3.9, 10 and 22 respectively [19]. The scale length is lower for higher-k dielectrics. Fig. 4.19 shows the scale length dependence on gate oxide thickness. The scale length value decreases with decreasing silicon layer thickness and gate oxide thickness and increasing dielectric constant of gate oxide.

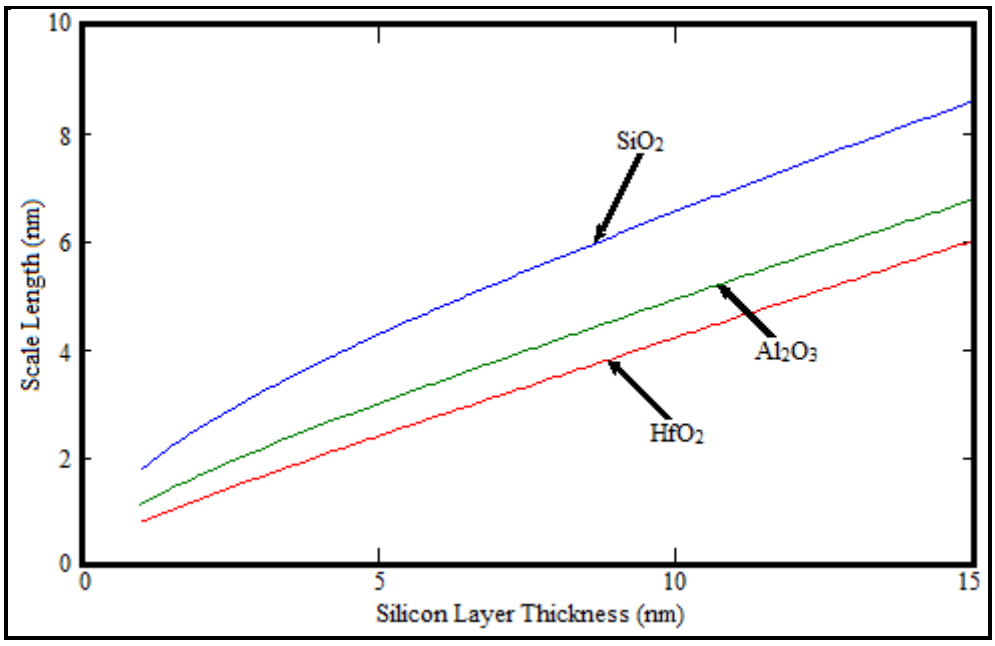

Fig. 4.18: Scale length variation with Silicon layer thickness for the dielectrics SiO_2 (3.9[19]), Al_2O_3 (10[19]) and HfO_2 (22[19]) at t_{ox} = 2nm

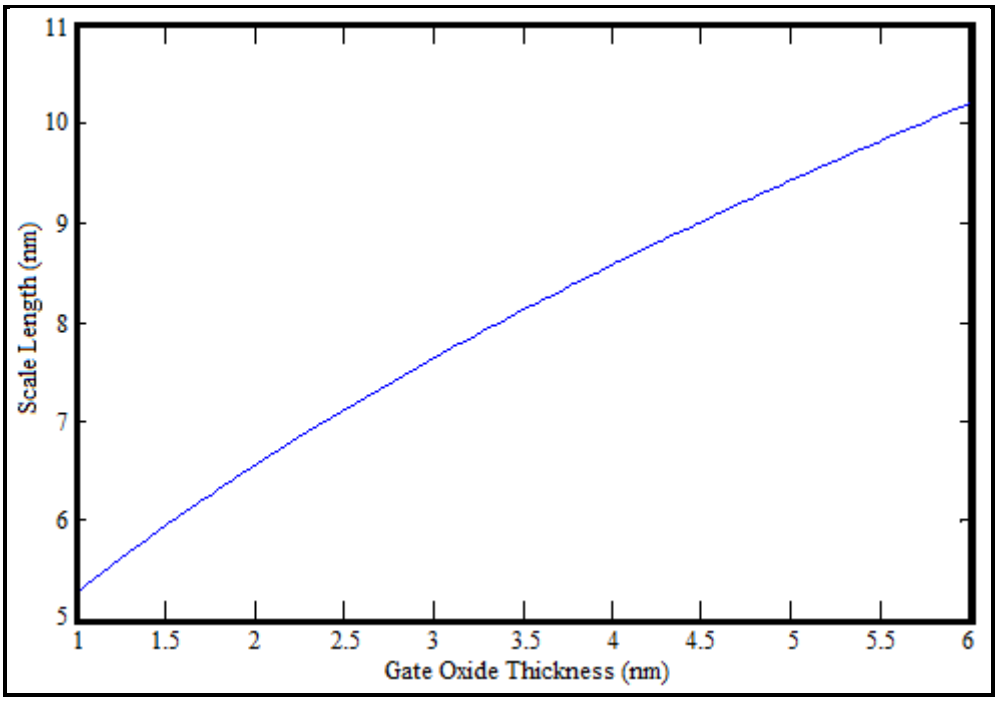

Fig. 4.19: Scale length variation with Gate Oxide thickness at t_{si} =10nm

The physics based model developed in section 4.3.2 has been simulated in MATLAB simulation environment. Result obtained in the MATLAB simulation has been compared with the simulation result obtained from Cogenda VisualTCAD 1.8.2 2D device simulator and few experimental results available in literature. All these simulation uses Fermi-Dirac statistics. For transverse field, surface effective field is used and for longitudinal field, simple E field mobility model is used for TCAD simulations. The source potential is taken as reference potential for all the calculations. The comparisons are shown in the figures as follows.

In Fig. 4.20 potential in the x-direction at y=0 is shown for different value of gate voltage (V_{gs}) ranging from 0-0.5V. For lower gate voltage the channel region is fully depleted. As the gate voltage increases beyond the threshold voltage, neutral Silicon layer starts forming in the channel. As a result, the potential distribution in the channel region becomes flatter and minimum potential in the channel is pulled up for higher gate voltage.

Fig. 4.21 shows potential in x-direction at y=0 for different values of drain voltage (V_{ds}) ranging from 0-2V. For short channel device, as the drain voltage increases, the minimum potential value decreases and position of minimum potential shifts towards the source-channel boundary which causes DIBL.

Fig. 4.22 shows potential in x-direction at y=0 for t_{ox}=2nm, t_{ox}=4nm and t_{ox} =6nm. Fig. 4.23 shows potential in x-direction at y=0 for t_{si}=5nm, t_{si}=10nm and t_{si}=15nm. With increasing gate oxide thickness and channel thickness the electric field decreases which reduces minimum potential in the channel region. When the gate oxide thickness and the channel thickness increases, effective control of the gate over the channel potential decreases.

Fig. 4.24 shows potential in x-direction at y=0 for L=20nm, 50nm and 100nm. For longer channel length, the influence of source-drain potential on channel potential towards the middle portion is less, which results in nearly a constant potential around the middle portion of the channel. When channel length decreases influence of source-drain potential results in reduction of minimum channel potential. Consequently, the channel potential does not remain constant for very short channel.

Fig. 4.25 shows potential in x-direction at y=0 for L_d=L_s=5nm, 10nm and 20nm. For shorter source-drain region, the depletion region extends over the entire source-drain length which results in a varying potential up to the source-drain ohmic contacts. As the source-drain length increases the extension of the depletion region in the source-drain region reduces and the potential tends to become constant near the ohmic contacts.

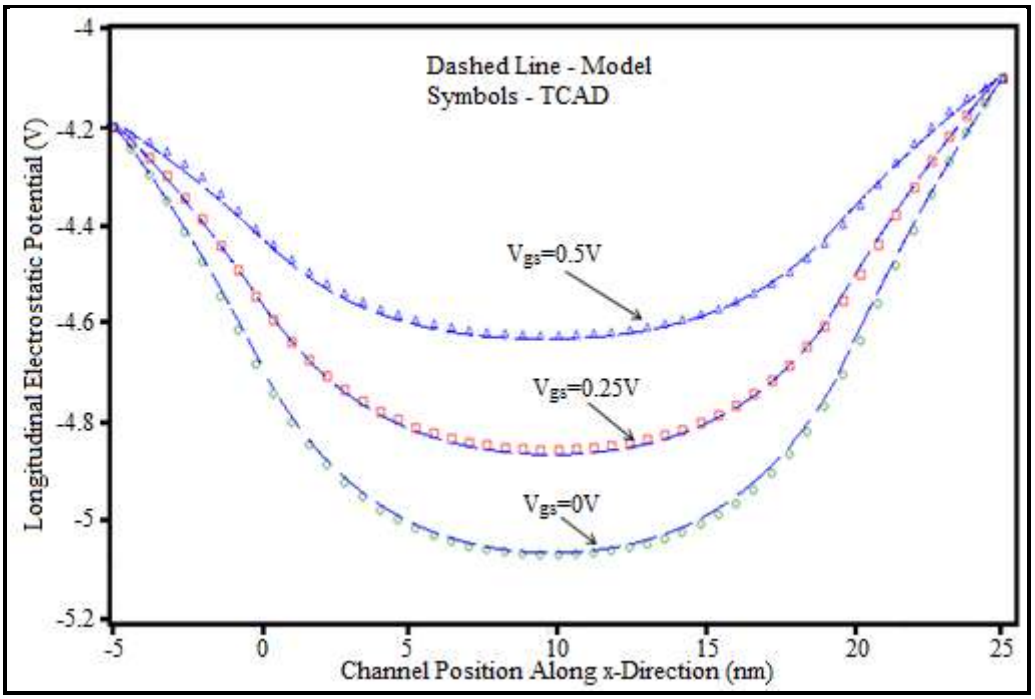

Fig. 4.20: Longitudinal Potential variation of DG JLT for V_{gs}=0V, 0.25V and 0.5V, y=0

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0.1V.

Average error = 1.4%
Maximum error =3.2%
Minimum error =0%

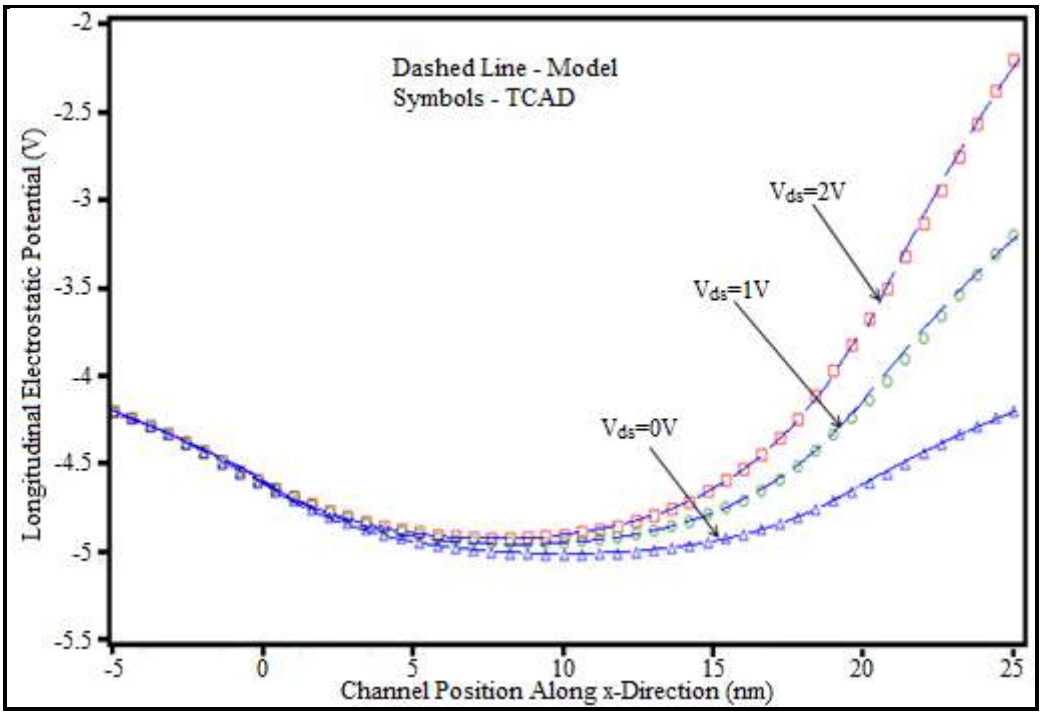

Fig. 4.21: Longitudinal Potential variation of DG JLT for $V_{ds} = 0V$, $1V$ and $2V$, $y = 0$

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Gate voltage (V_{gs})	0.1V.

Average error = 2.1%
Maximum error =4.3%
Minimum error =0%

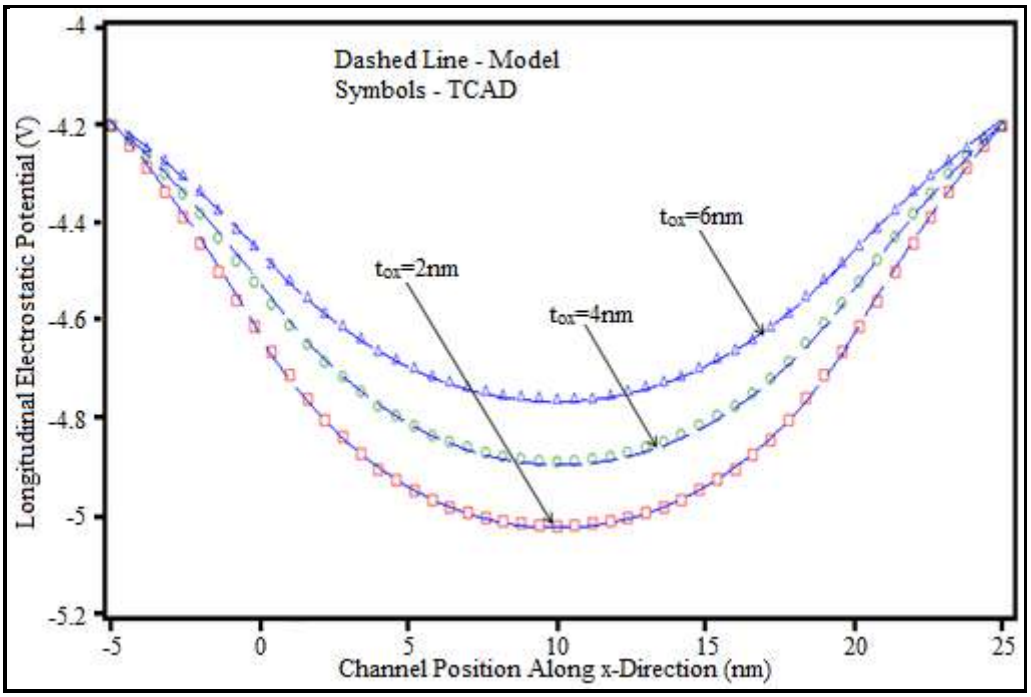

Fig. 4.22: Longitudinal Potential variation of DG JLT for t_{ox} = 2nm, 4nm and 6nm, $y = 0$

Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0.1V
Gate voltage (V_{gs})	0V

Average error = 1.5%
Maximum error =2.1%
Minimum error =0%

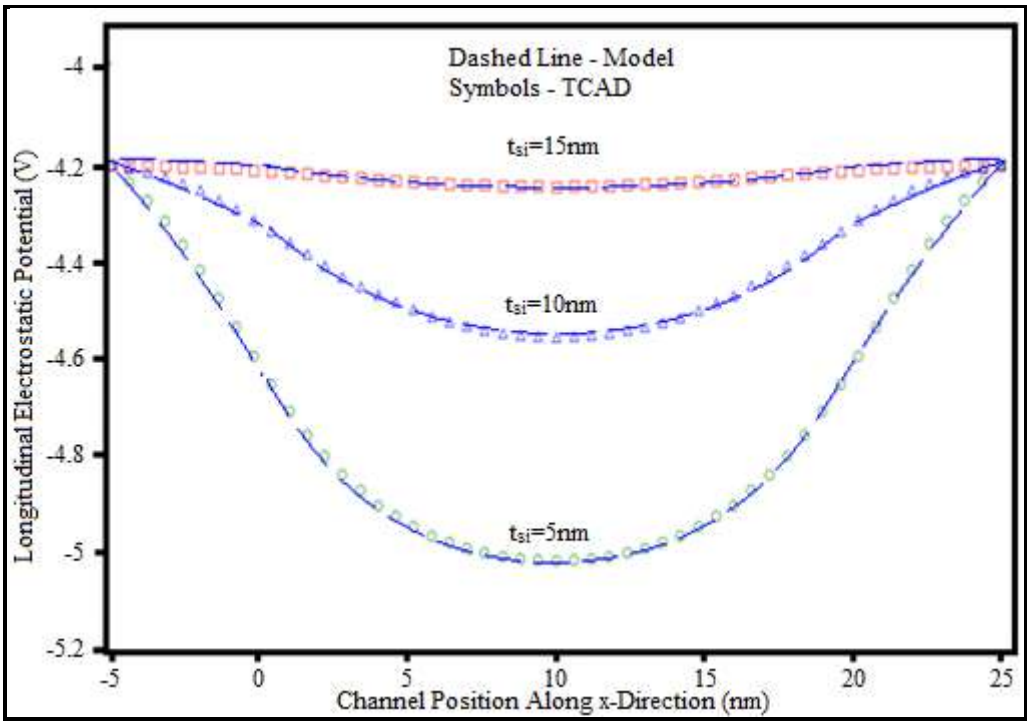

Fig. 4.23: Longitudinal Potential variation of DG JLT for t_{si} = 5nm, 10nm and 15nm, $y = 0$

Gate oxide thickness (t_{ox})	2nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0.1V
Gate voltage (V_{gs})	0V

Average error = 1.8%
Maximum error =2.3%
Minimum error =0%

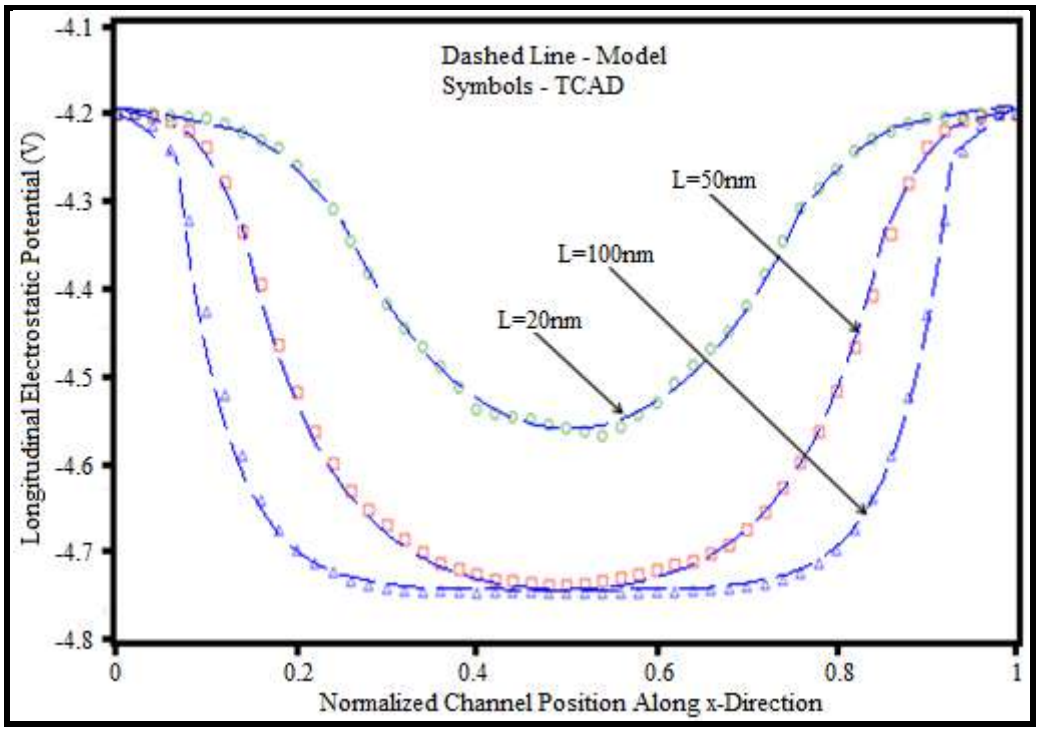

Fig. 4.24: Longitudinal Potential variation of DG JLT for L = 20nm, 50nm and 100nm, $y = 0$

Channel thickness (t_{si})	10nm
Gate oxide thickness (t_{ox})	2nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0.1V
Gate voltage (V_{gs})	0V

Average error = 1.8%
Maximum error =3.3%
Minimum error =0%

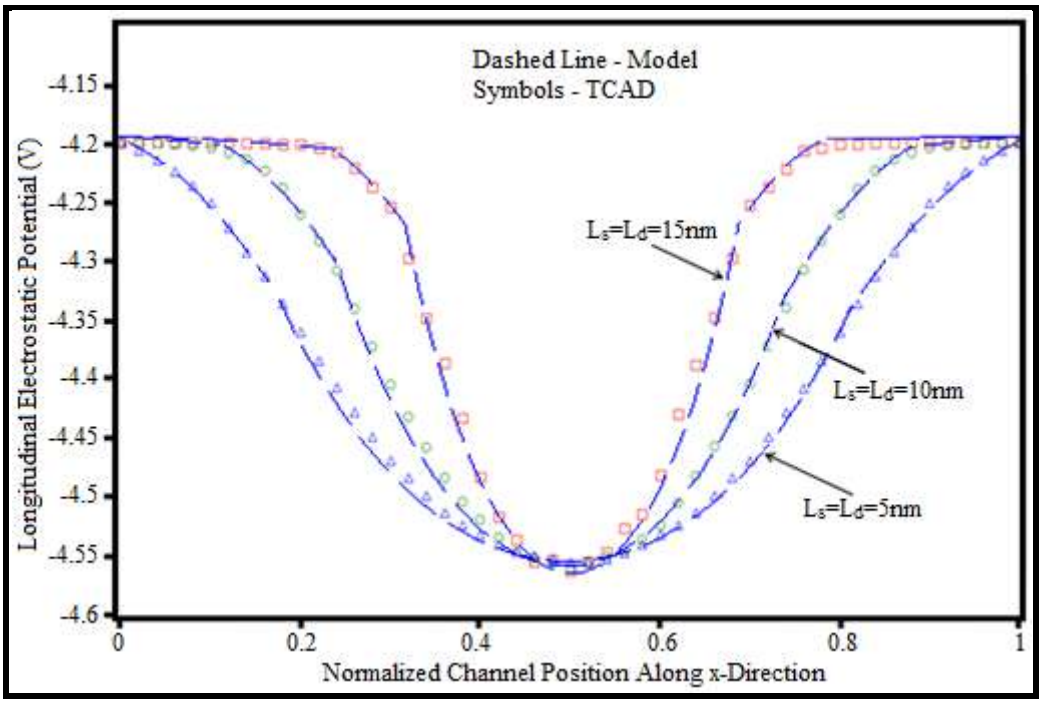

Fig. 4.25: Longitudinal Potential variation of DG JLT for $L_s = L_d$ = 5nm, 10nm and 20nm, $y = 0$

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Drain voltage (V_{ds})	0.1V
Gate voltage (V_{gs})	0V

Average error = 1.2%
Maximum error =3.15%
Minimum error =0%

Fig. 4.26 shows transverse potential at x=L/2 for V_{ds}=0V, V_{ds}=1V and V_{ds}=2V. With the increasing drain voltage the gate control over the channel decreases and variation of potential increases. This is because the electric field due to drain voltage opposes the applied gate electric field.

Fig. 4.27 shows transverse potential at x=L/2 for V_{gs}=0V, V_{gs}=0.1V and V_{gs}=0.2V. Fig. 4.28 shows transverse potential at x=L/2 for t_{ox}=2nm, t_{ox}=4nm and t_{ox}=6nm. As the oxide thickness increases the vertical electric field reduces causing a decrease in the potential value.

Fig. 4.29 shows the transverse potential at x=L/2 for L=20nm, 50nm and 100nm. For shorter channel bending degree is high, which implies that the DIBL is more significant for the shorter device.

Fig. 4.30 shows transverse potential at x=L/2 for t_{si}=5nm, 10nm and 15nm. From the figure, it is clear that when channel thickness increases the influence of gate electric field at the middle reduces causing a larger variation in the potential. In this case to plot the potential profile with respect to channel position along y-direction the normalized values of position has been taken as the gate-gate distance in different for the three curves.

For obtaining the results presented in Fig. 4.26 to Fig. 4.30 the general for potential expression in (4.33) has been used. However, it has a central potential term expression for which is obtained in (4.39) is inserted into it. In all the cases, the doping concentration is $10^{19}/cm^3$ and work function of gate is Φ_M =5.4eV. In all the cases, the model is in a very close agreement with TCAD simulation results with an average error of 1.42%. Fig. 4.31-Fig. 4.36 shows the comparison of the model for tri-gate JLT with TCAD. Fig. 4.37 shows the comparison of the model with experimental values taken from a reported work by Collinge et al. [2] in 2009. While searching for literature to compare the potential model with experimental results, the literature containing experimental results on potential of double gate JLT has not been found. Hence a potential model for tri-gate JLT following the same approach as for DGJLT has been developed and validated. The model for tri-gate JLT agrees

closely with the measured value with an average error of 1.71%, which ensures the applicability of the model.

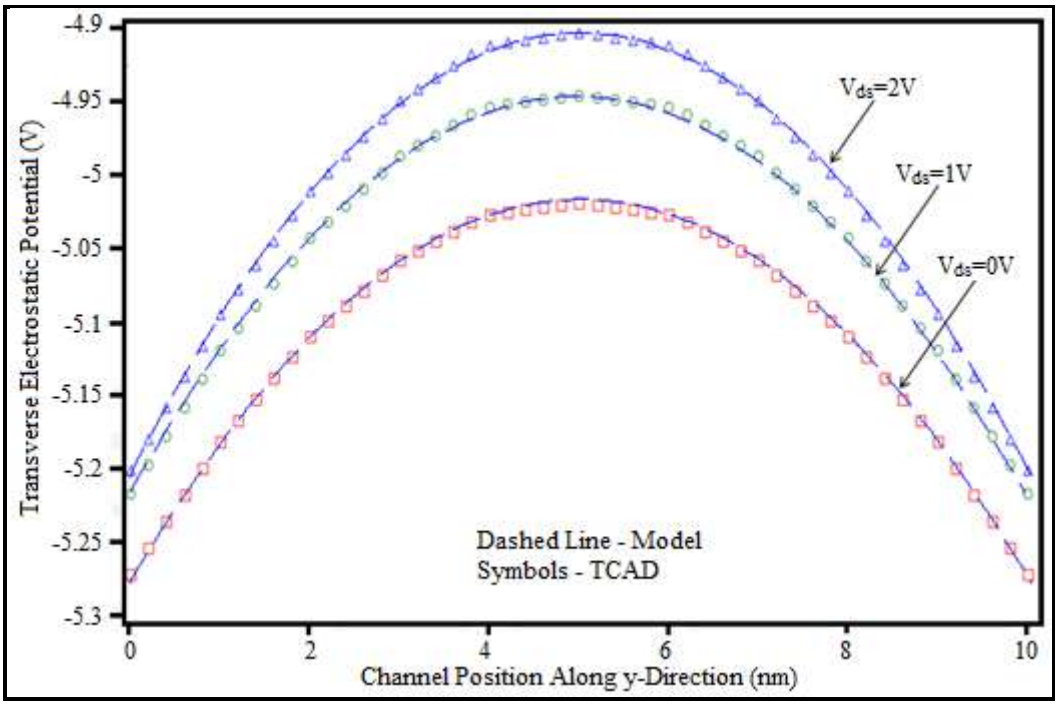

Fig. 4.26: Transverse Potential variation of DG JLT for $V_{ds} = 0V$, $1V$ and $2V$ at $x = \frac{L}{2}$

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Gate voltage (V_{gs})	0V

Average error = 0.9%
Maximum error =1.9%
Minimum error =0%

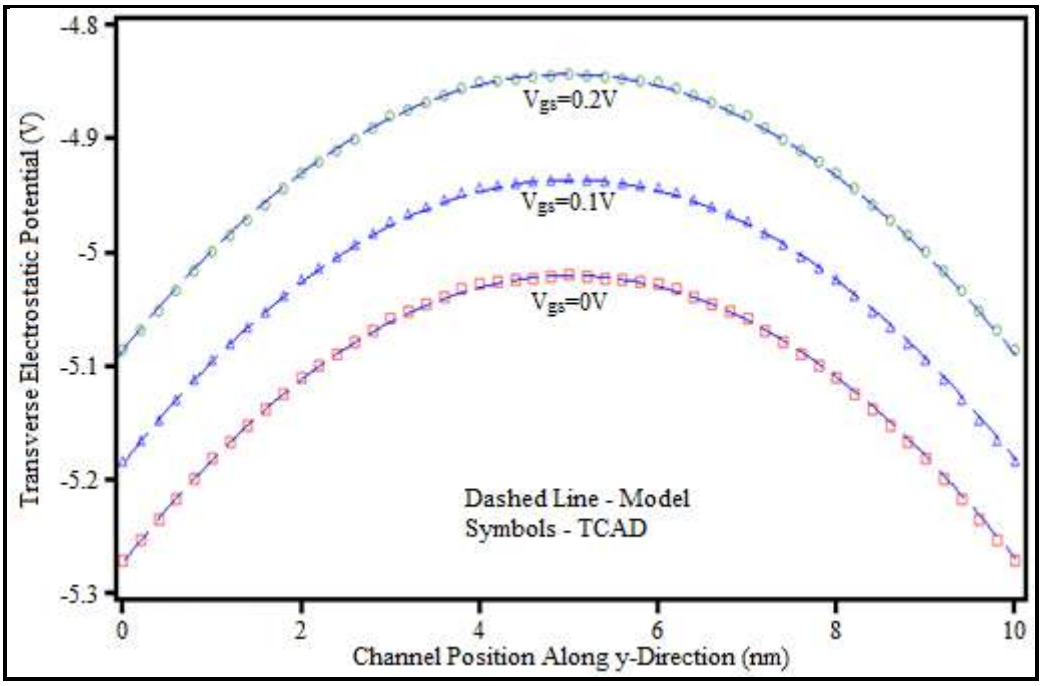

Fig. 4.27: Transverse Potential variation of DG JLT for $V_{gs} = 0V$, $0.1V$ and $0.2V$ at $x = \frac{L}{2}$

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0V.

Average error = 0.9%
Maximum error =1.8%
Minimum error =0%

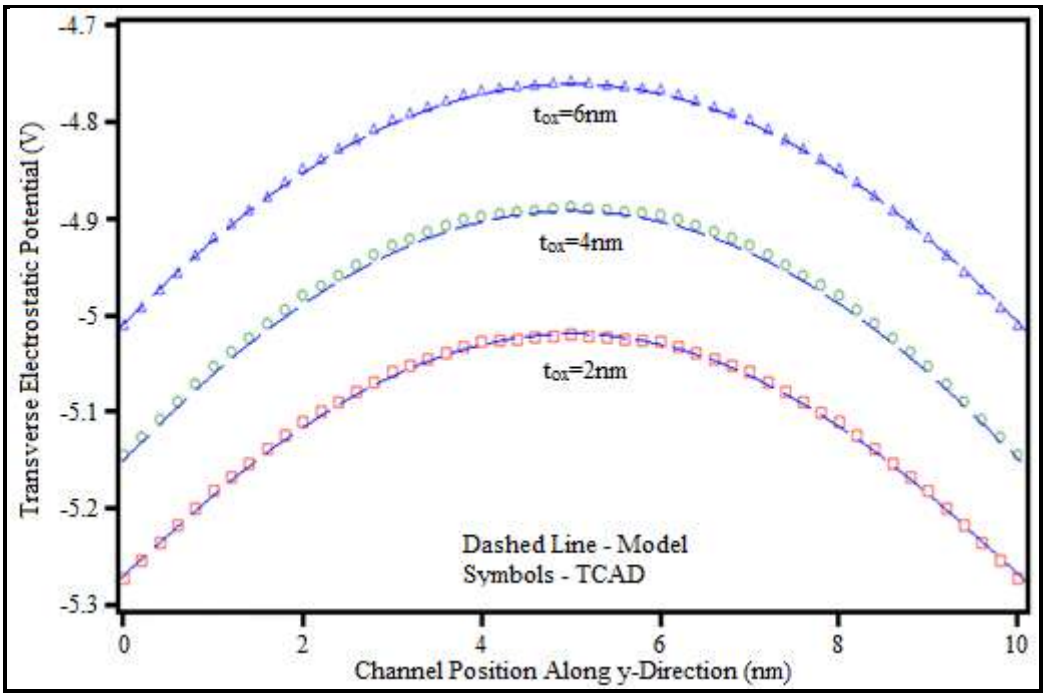

Fig. 4.28: Transverse Potential variation of DG JLT for t_{ox} = 2nm, 4nm and 6nm at $x = \frac{L}{2}$

Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0V
Gate voltage (V_{gs})	0V.

Average error = 1.3%
Maximum error =4.2%
Minimum error =0%

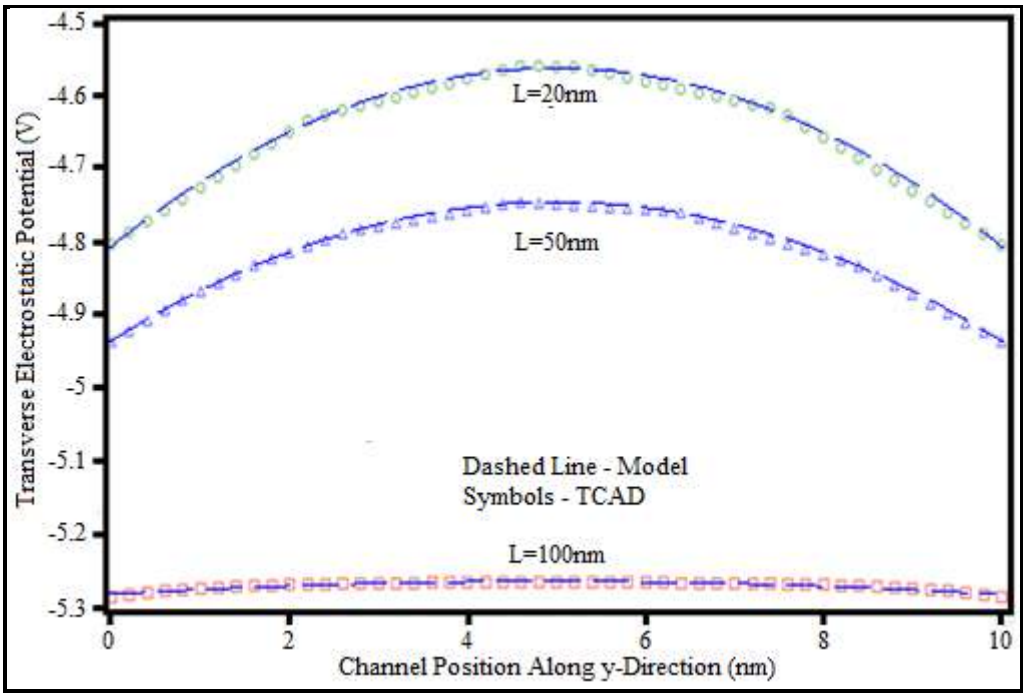

Fig. 4.29: Transverse Potential variation of DG JLT for L = 20nm, 50nm and 100nm at $x = \frac{L}{2}$

Channel thickness (t_{si})	10nm
Gate oxide thickness (t_{ox})	2nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0V
Drain voltage (V_{ds})	0V.

Average error = 1.2%
Maximum error =2.8%
Minimum error =0%

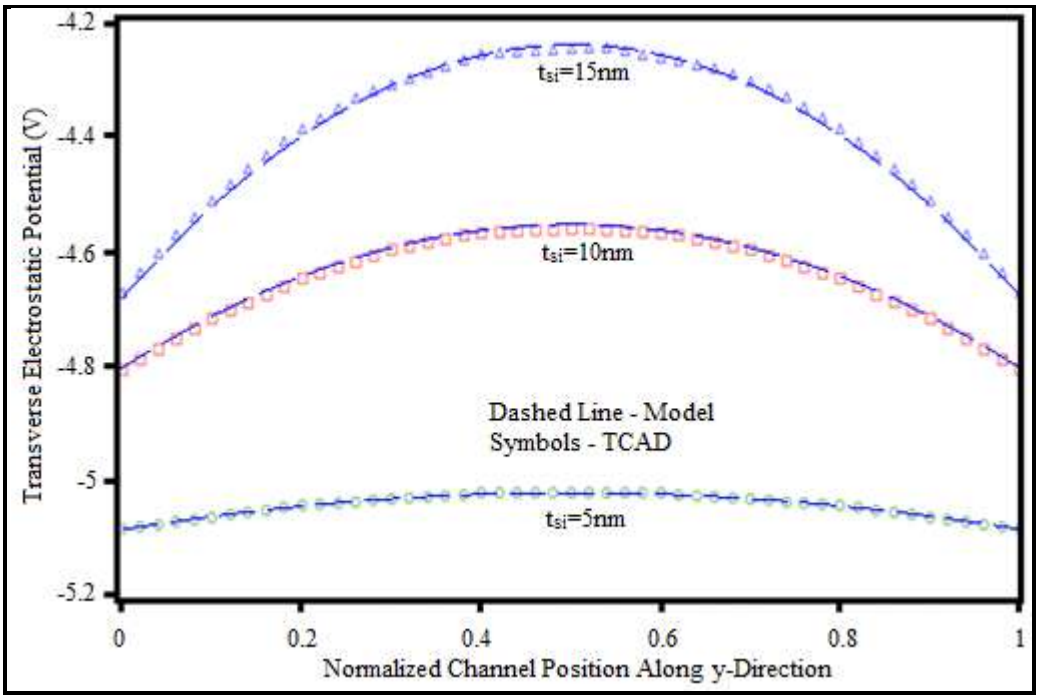

Fig. 4.30: Transverse Potential variation of DG JLT for t_{si} = 5nm, 10nm and 15nm at $x = \frac{L}{2}$

Gate oxide thickness (t_{ox})	2nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0V
Gate voltage (V_{gs})	0V.

Average error = 1.5%
Maximum error =2.5%
Minimum error =0%

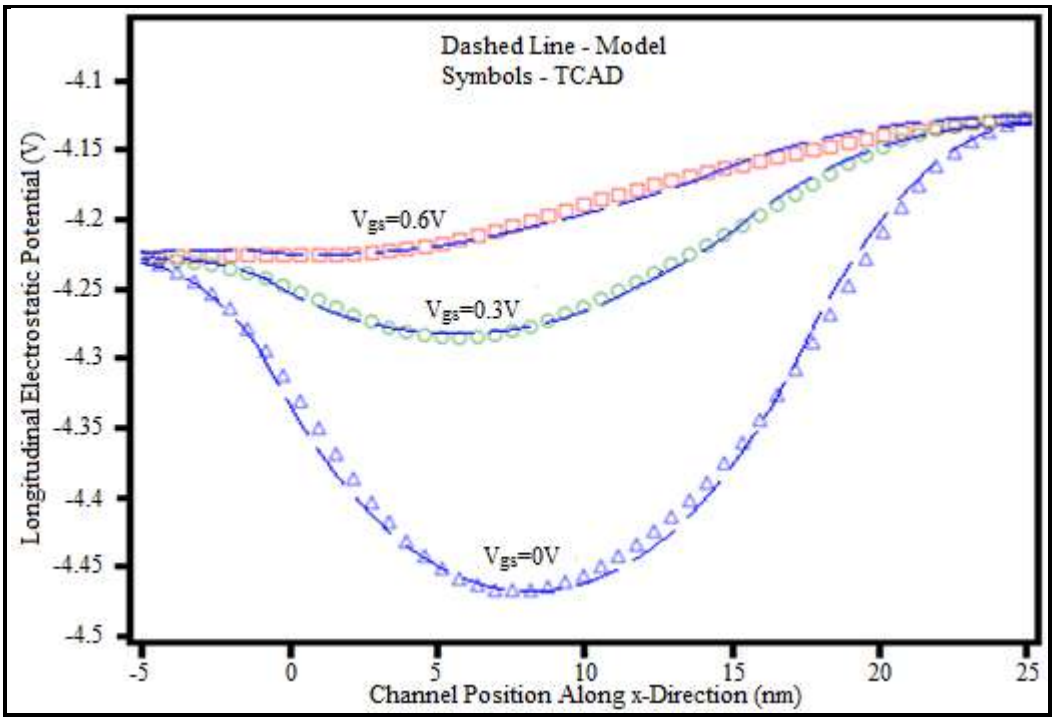

Fig. 4.31: Longitudinal potential variation with channel position along x- direction at y=0 for V_{gs}=0V, 0.3V and 0.6V for tri-gate JLT.

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0.1V.

Average error = 1.4%
Maximum error =3.9%
Minimum error =0%

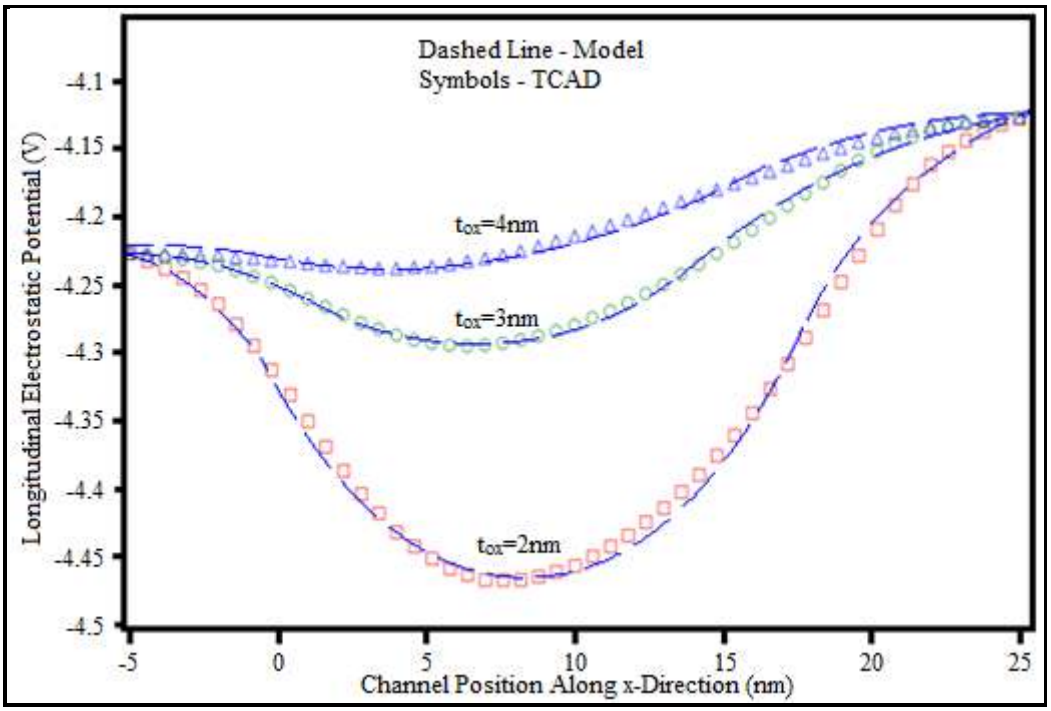

Fig. 4.32: Longitudinal potential variation with channel position along x- direction at y=0 for t_{ox}=2nm, 3nm and 4nm for tri-gate JLT.

Gate to source voltage (V_{gs})	0V
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0.1V.

Average error = 1.5%
Maximum error =3.6%
Minimum error =0%

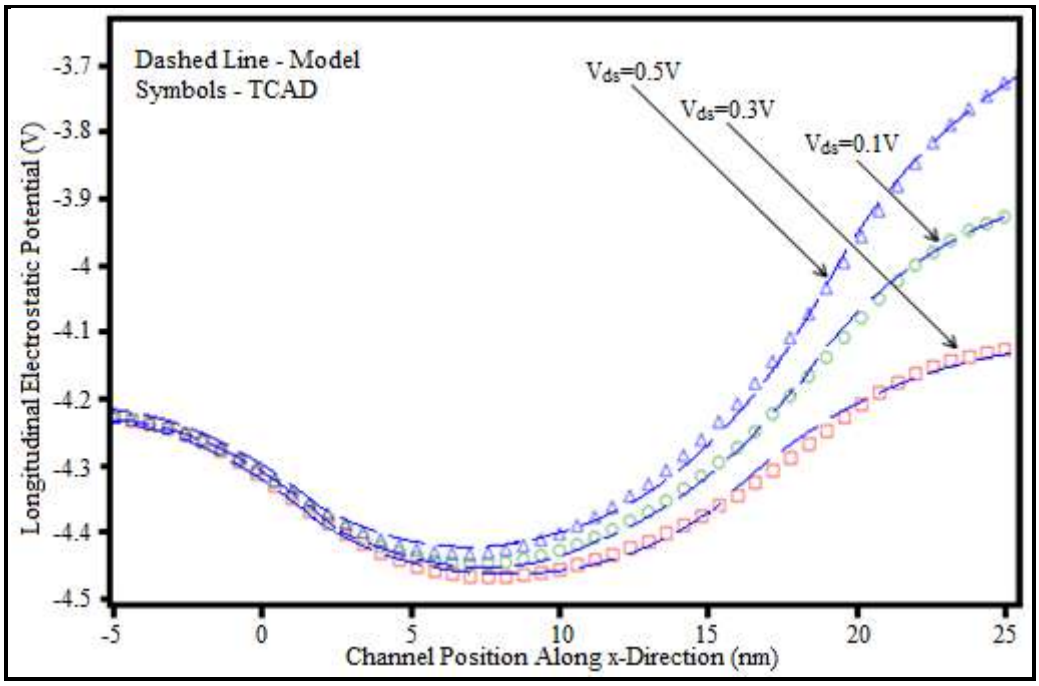

Fig. 4.33: Longitudinal potential variation with channel position along x- direction at y=0 for V_{ds}=0.1V, 0.3V and 0.5V for tri-gate JLT.

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Gate to source voltage (V_{gs})	0V.

Average error = 1.1%
Maximum error =2.5%
Minimum error =0%

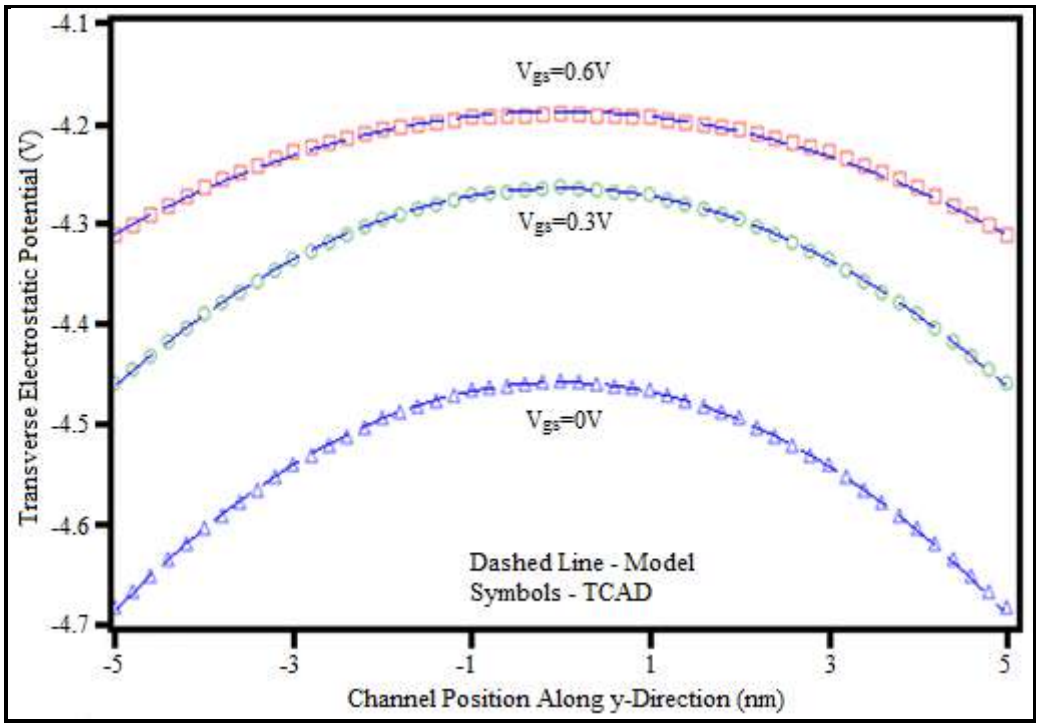

Fig. 4.34: Transverse potential variation with channel position along y-direction at x=L/2 for V_{gs}=0V, 0.3V and 0.6V

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0.1V.

Average error = 1.3%
Maximum error =3.2%
Minimum error =0%

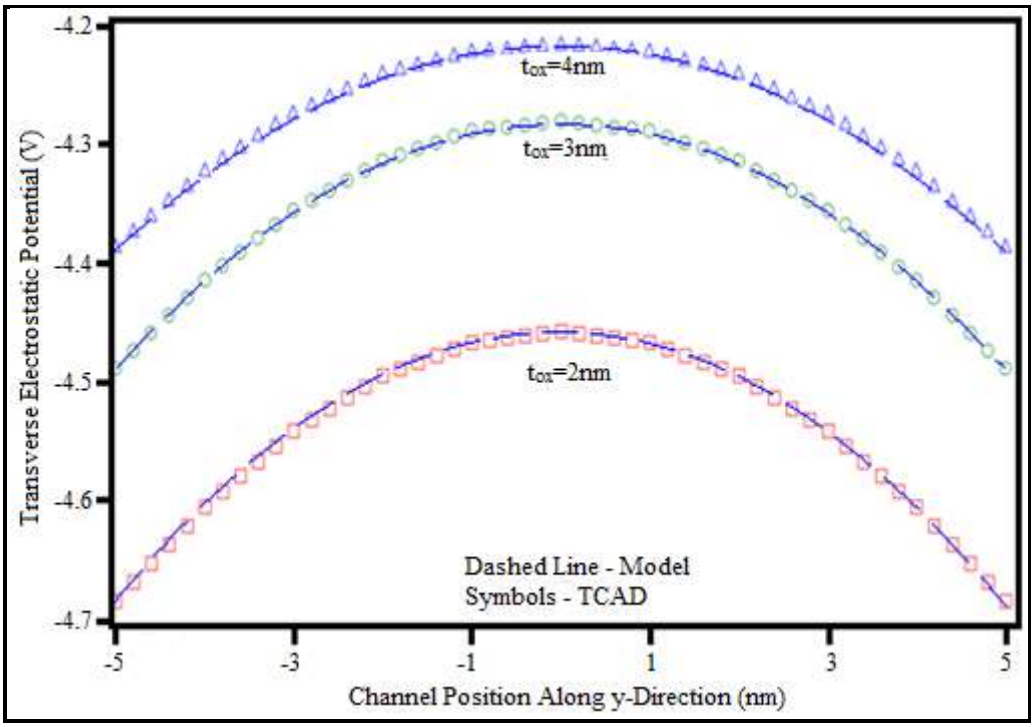

Fig. 4.35: Transverse potential variation with channel position along y-direction at x=L/2 for t_{ox}=2nm, 3nm and 4nm for tri-gate JLT.

Gate to source voltage (V_{gs})	0V
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0.1V.

Average error = 1.2%
Maximum error =2.2%
Minimum error =0%

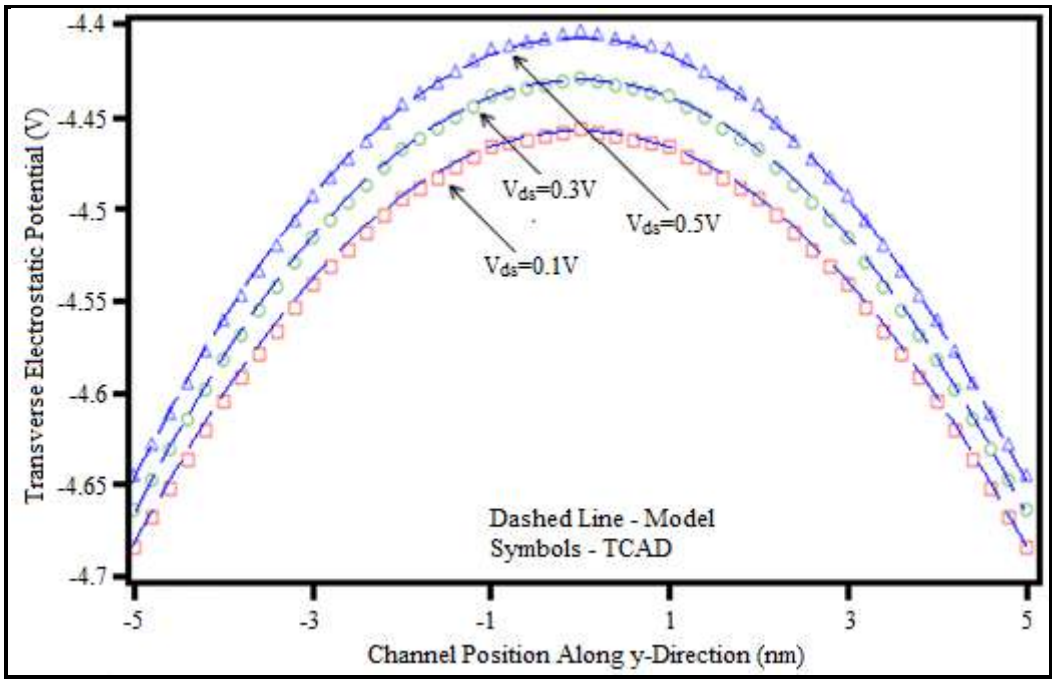

Fig. 4.36: Transverse potential variation with channel position along y-direction at x=L/2 for V_{ds}=0.1V, 0.3V and 0.5V for tri-gate JLT.

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Channel length (L)	20nm
Length of the source(L_s) and drain(L_d) region	5nm.
Gate to source voltage (V_{gs})	0V.

Average error = 0.9%
Maximum error =1.3%
Minimum error =0%

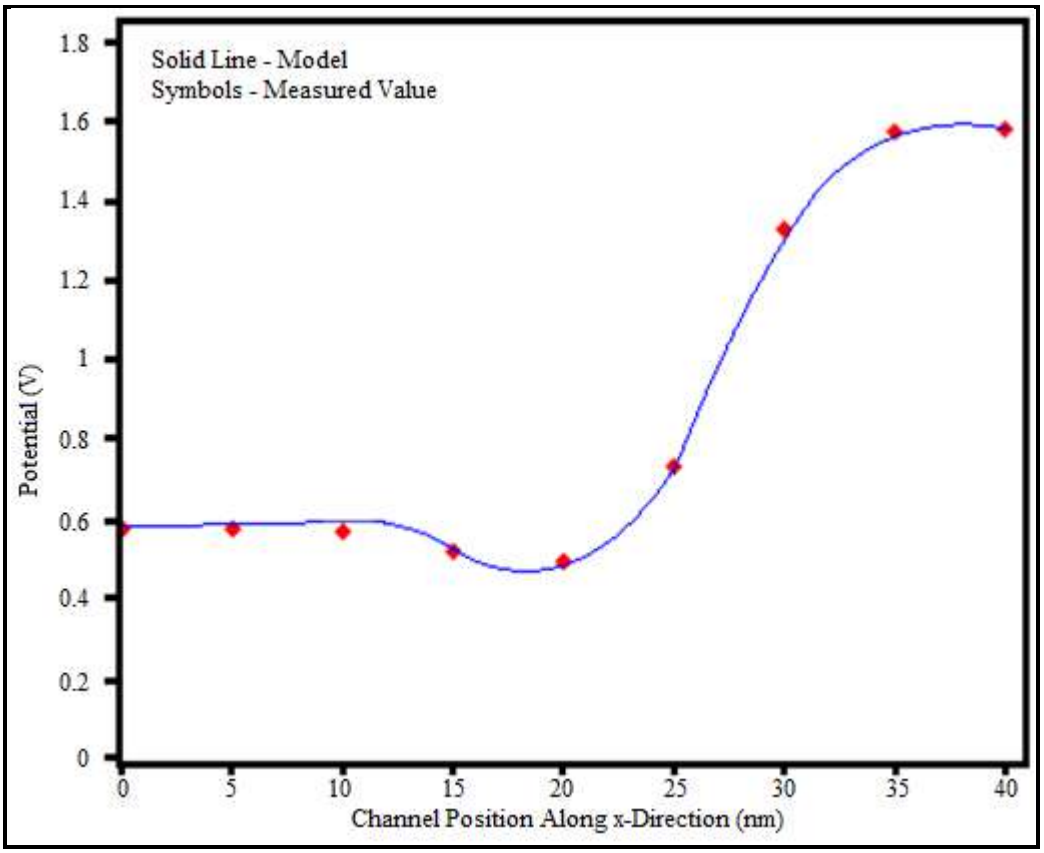

Fig. 4.37: Comparison of potential model with experimental results [2]

Average error = 1.3%
Maximum error =4.2%
Minimum error =0%

4.5 Conclusions

An analytical model for depletion width of a double and single gate JLT is obtained and the threshold voltage of a symmetric double gate JLT is obtained using the depletion width expression. A simple definition of threshold voltage is also given. The model is validated using TCAD simulations. The model is in a close agreement with the simulated results with an average error of 1.12%. From the model it is clear that, in order to achieve a suitable positive threshold voltage at ultra short channel length, high doping concentration is required and the gate oxide and channel should be very thin. The model is valid for both short-channel and long-channel JLTs. An analytical model for potential in channel region as well as source-drain region is also obtained for a symmetric double gate JLT and tri-gate JLT. The potential model is also validated using TCAD simulation results and experimental results available in literature. While comparing the simulation results with the results obtained from TCAD an average error of 1.42% has been observed. While an average error of 1.71% has been observed when compared with experimental results available in literature. As all the models are fully analytical they are useful for compact modelling.

Contributions

In this chapter depletion width, threshold voltage and potential model of junctionless transistor has been reported, which shows accuracy in both short channel and long channel devices as evident from the comparison with TCAD simulation results. The factor behind this high level of accuracy is the inclusion of the influence of the electrostatic forces on the source and drain region. The knowledge of the space charge width, threshold voltage and internal electrostatic potential can give vital information regarding performance of the device.

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