Chapter 5

Drain Current Modelling of Double Gate JLT

5.1 Introduction

In a junctionless transistor, the variation gate voltage causes variation of depletion width leading to channel resistance variation. When the gate voltage is below the threshold voltage, the channel is devoid of carriers resulting in a very high channel resistance. Due to this practically no current can flow through the device [1-18]. As the gate voltage increases above the threshold voltage the depletion width starts decreasing. As a consequence, channel resistance decreases which results in a decrease in the channel potential barrier to initiate the flow of current through the channel. Further increase in the gate voltage reduces the depletion width until the condition of zero depletion width. When the depletion width becomes zero the channel resistance drops to a very small value resulting in a large current. The increase of gate voltage beyond this point also causes an increase in the drain current due to accumulation of charges near the oxide semiconductor boundary. However the current due to accumulated charges is negligible compared to the bulk current which dominates on-state characteristics of JLT. Thus the drain current in a JLT is directly related to the channel resistance which varies with the depletion region thickness.

In this chapter a fully analytical approach for drain current modelling of a symmetric double gate junctionless transistor is presented. This approach involves the division of the channel into a number of elementary segments. An approach for drain current modelling for a MOSFET that involves consideration of an elementary segment is already available in literature [19]. However, in the process of formulation of mathematical model for the drain current of JLT, a non-linear channel potential profile is considered, where as in case of MOSFET normally a linear channel potential is considered. For modelling purpose the entire length of channel has been divided into some elementary segments consisting mainly of two types of regions, viz. depleted and non-depleted, spread over three different regions across the width of the device. The resistance of different segments are obtained from the depletion width model, which finally used to obtain the effective channel resistance of the JLT. The total channel resistance can be obtained by adding the resistances of all of the segments as they are connected in series. The drain current can be obtained from the resistance expression

by using ohm's law. The model is validated by comparing to the results obtained from TCAD simulations and also few experimental results available in the literature.

5.2 Drain Current Modelling

5.2.1 Mathematical Formulation

The cross-sectional view of a double gate JLT is shown in Fig. 5.1. The body of the device is divided into a number of elementary segments along the channel length as shown in Fig. 5.2. The length of one segment is equal to the atomic diameter of Silicon, i.e. 0.333 nm. Each segment consists of

i) a depletion region with a resistance $R_d(x, V_{gs}, V_{ds})$ for $V_{gs} \leq V_{th}$ or
ii) a neutral semiconductor region with a resistance $R_{nd}(x, V_{gs}, V_{ds})$ for $V_{gs} \geq V_{fb}$ or
iii) both depletion region and a neutral semiconductor region for $V_{th} \leq V_{gs} \leq V_{fb}$. One segment can be considered as a parallel combination of three resistances- one non-depleted layer resistance, $R_{nd}(x, V_{gs}, V_{ds})$ and two depleted layer resistance, $R_d(x, V_{gs}, V_{ds})$ as shown in Fig. 5.2.

The equivalent circuit of one segment is a parallel combination of three resistances, $R_d(x, V_{gs}, V_{ds})$, $R_{nd}(x, V_{gs}, V_{ds})$ and $R_d(x, V_{gs}, V_{ds})$ as shown in Fig. 5.3(a). If one segment consists of only neutral semiconductor region the equivalent circuit reduces to $R_{nd}(x, V_{gs}, V_{ds})$ as shown in Fig. 5.3(b) and if the segment consists of only depletion region then the equivalent circuit reduces to $R_d(x, V_{gs}, V_{ds})$ as shown in Fig. 5.3(c).

The resistance of the non-depleted region of each segment is given as,

$$R_{nd}(x, V_{gs}, V_{ds}) = \frac{1}{q\mu n}\frac{\Delta L}{W(t_{si} - W_d)} \tag{5.1}$$

Where,

W_d is the depletion width

W is the device width

ΔL is the length of one segment

μ is the mobility

n is the carrier concentration

q is charge of one electron.

The depletion width as obtained in chapter 4 can be given as,

$$W_d = t_{si} - \sqrt{\frac{4t_{si} \in_{si} t_{ox} qN_d + \in_{ox} t_{si}^2 qN_d - 8 \in_{ox} \in_{si} (\phi_0 - \phi_{gs})}{\in_{ox} qN_d}} \tag{5.2}$$

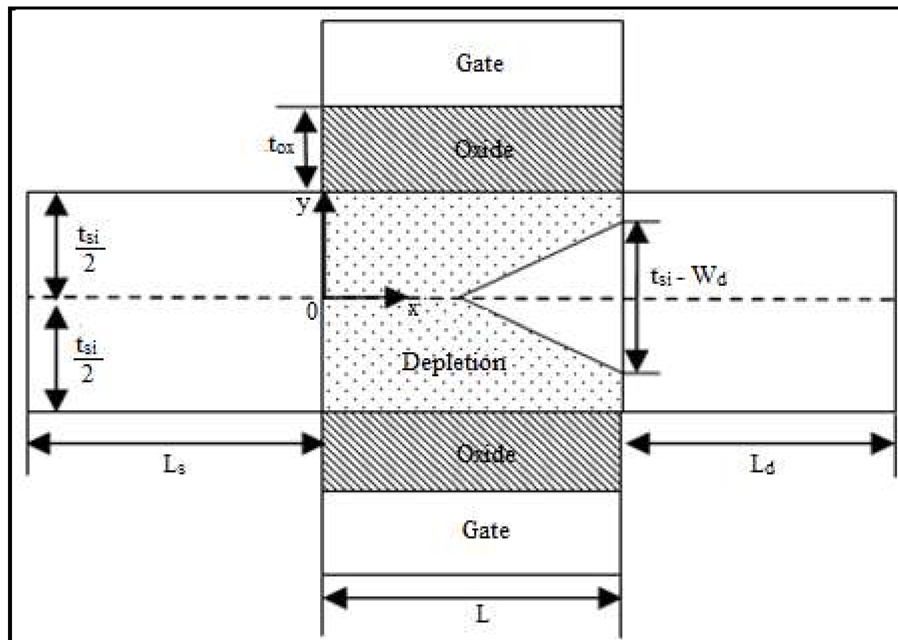

Fig. 5.1: Cross sectional view of a Double Gate JLT

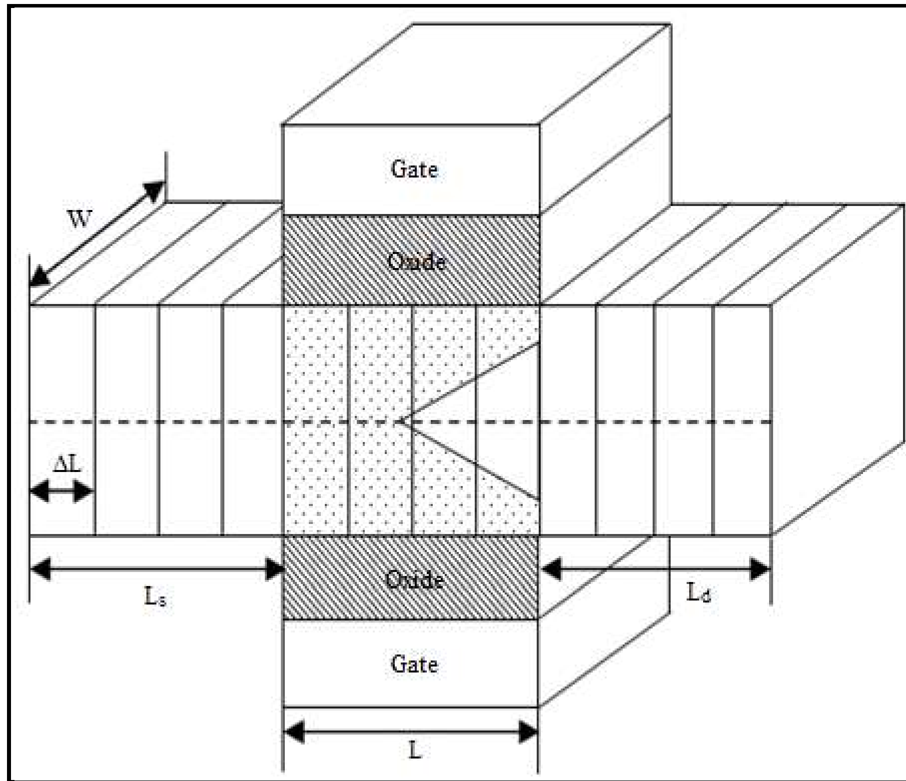

Fig. 5.2: A Double Gate JLT with body divided into a number of small segments of length ΔL

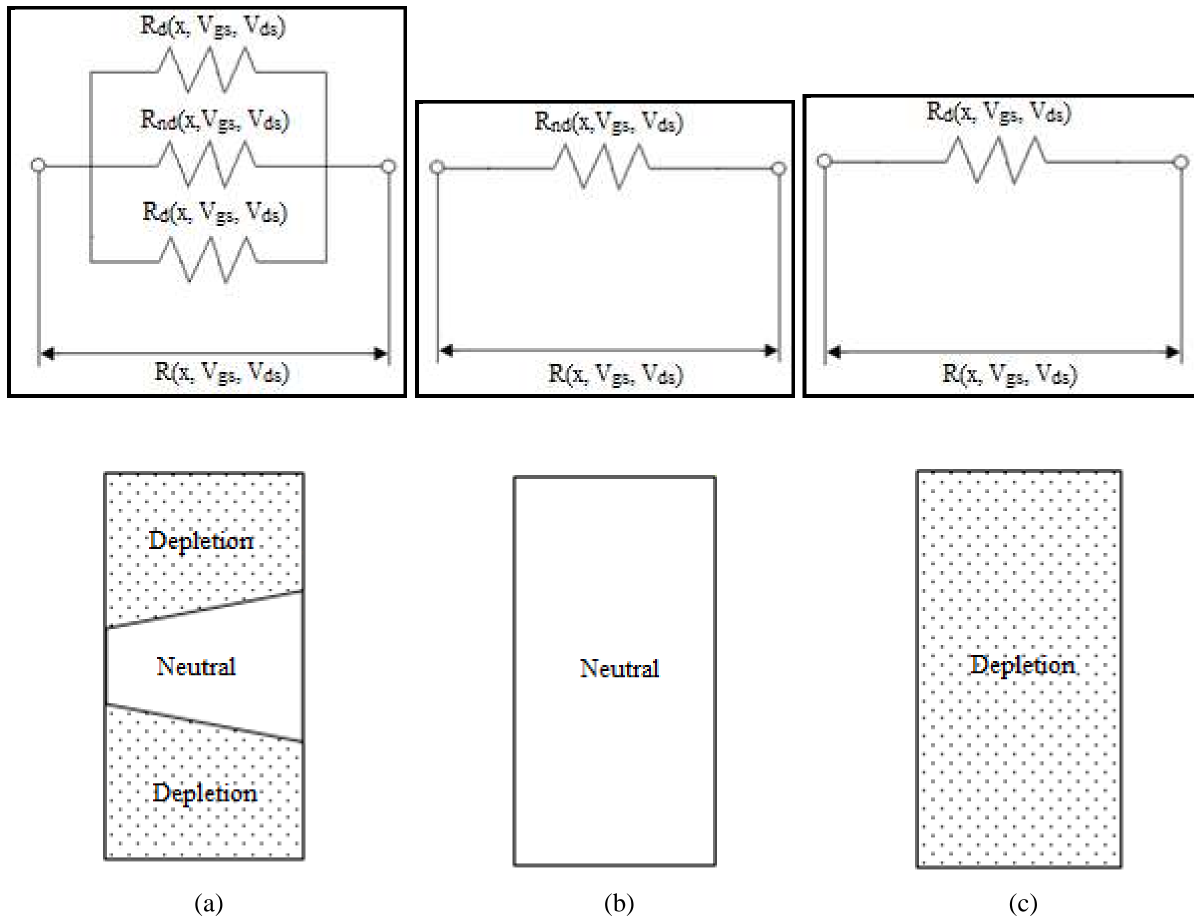

Fig. 5.3: Equivalent circuit of a segment (a) A segment with combination of depletion and neutral semiconductor region (b) A non depleted segment (c) A fully depleted segment

Where, ϕ_0 is central electrostatic potential which is given as,

$$\phi_0(x)=\left[\frac{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}}-\frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}}{(e^{2\frac{L+L_d}{\lambda}}-e^{-2\frac{L_s}{\lambda}})}e^{\frac{x}{\lambda}}\right]-$$

$$\left[\frac{\{(V_{ds}+C\lambda^2)e^{\frac{L+L_d}{\lambda}}-\frac{C\lambda^2}{e^{\frac{L_s}{\lambda}}}\}e^{-2\frac{L_s}{\lambda}}-C\lambda^2(e^{2\frac{L+L_d}{\lambda}}-e^{-2\frac{L_s}{\lambda}})e^{\frac{L_s}{\lambda}}}{(e^{2\frac{L+L_d}{\lambda}}-e^{-2\frac{L_s}{\lambda}})}e^{-\frac{x}{\lambda}}\right]-C\lambda^2 \tag{5.3}$$

Where, $\lambda=\sqrt{\frac{t_{si}(4\in_{si}t_{ox}+\in_{ox}t_{si})}{8\in_{ox}}}$ is the scale length

Inserting (5.2) in (5.1) the resistance of the non-depleted region can be written as,

$$R_{nd}(x,V_{gs},V_{ds})=\frac{1}{q\mu n}\frac{\Delta L}{W\sqrt{\frac{4t_{si}\in_{si}t_{ox}qN_d+\in_{ox}t_{si}^2qN_d-8\in_{ox}\in_{si}(\phi_0-\phi_{gs})}{\in_{ox}qN_d}}} \tag{5.4}$$

Similarly, the resistance of the depleted region of each segment is given as,

$$R_d(x,V_{gs},V_{ds})=\frac{1}{q\mu p}\frac{\Delta L}{W(t_{si}-\sqrt{\frac{4t_{si}\in_{si}t_{ox}qN_d+\in_{ox}t_{si}^2qN_d-8\in_{ox}\in_{si}(\phi_0-\phi_{gs})}{\in_{ox}qN_d}})} \tag{5.5}$$

Since the substrate is heavily doped, the approximate carrier density of the non-depleted region is given as,

$$n = \frac{N_d}{2} + \sqrt{\frac{N_d^{\,2}}{4} + n_i^{\,2}} \tag{5.6}$$

The carrier density of the depleted region is given as,

$$p = \frac{n_i^{\,2}}{\frac{N_d}{2} + \sqrt{\frac{N_d^{\,2}}{4} + n_i^{\,2}}} \tag{5.7}$$

Where, n_i is intrinsic carrier concentration.

The equivalent resistance of one segment can be given as,

$R(x, V_{gs}, V_{ds}) = R_d(x, V_{gs}, V_{ds}) || R_{nd}(x, V_{gs}, V_{ds}) || R_d(x, V_{gs}, V_{ds})$

Where,

$$x = 0, \Delta L, ..., z\Delta L$$

Where,

$$z = \frac{L}{\Delta L} - 1 \qquad x = m\Delta L$$

$$m = 0, 1, 2, ..., z$$

In the subthreshold region the equivalent resistance reduces to a single depletion layer resistance and in the flatband region it reduces to a single non-depletion layer resistance.

Considering the quantum mechanical effects, the depletion layer and non-depletion layer resistance can be written as,

$$R_d(x,V_{gs},V_{ds}) = \frac{1}{q\mu_{eff}p}\frac{\Delta L}{W\left(t_{si}-\sqrt{\frac{4t_{si}\in_{si}t_{ox}qN_d+\in_{ox}t_{si}^2qN_d-8\in_{ox}\in_{si}(\phi_0-\phi_{gs}^{/})}{\in_{ox}qN_d}}\right)} \tag{5.8}$$

and

$$R_{nd}(x,V_{gs},V_{ds}) = \frac{1}{q\mu_{eff}n}\frac{\Delta L}{W\sqrt{\frac{4t_{si}\in_{si}t_{ox}qN_d+\in_{ox}t_{si}^2qN_d+8\in_{ox}\in_{si}(\phi_0-\phi_{gs}^{/})}{\in_{ox}qN_d}}} \tag{5.9}$$

Where, the effective mobility considering the velocity saturation effect can be written as [11],

$$\mu_{eff} = \frac{\mu}{\left[1+\left(\frac{\mu V_{ds,eff}}{v_{sat}L}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{5.10}$$

and $\phi_{gs}^{/} = \phi_{gs} - \Delta V_{th}$, ΔV_{th} is the threshold voltage shift due to quantum mechanical effects given as [20],

$$\Delta V_{th} = \frac{kT}{q}\ln\frac{\alpha Erf\left(\frac{t_{si}}{2}\sqrt{\frac{q^2N_d}{2\in_{si}kT}}\right)}{\frac{4\pi kT}{h^2}\frac{N_d}{N_c}[2m_{d,1}^{*}\sum_n e^{-E_{1,n}/kT}+4m_{d,2}^{*}\sum_n e^{-E_{2,n}/kT}]} \tag{5.11}$$

Using 1D Poisson's equation the applied potential variation along the channel can be determined. The 1D Poisson's equation can be given as [21],

$$\frac{d^2\phi(x)}{dx} = -\frac{qN_d}{\in_{si}} \tag{5.12}$$

One of the possible solution can be written as [22],

$$\phi(x) = c_0 + c_1 x + c_2 x^2 \tag{5.13}$$

Where,

$$c_2 = -\frac{qN_d}{2\in_{si}}$$

At, x= - L_s

$$\phi(-L_s) = c_0 - c_1 L_s + c_2 L_s^{\ 2} = 0$$

$$c_0 - c_1 L_s - \frac{qN_d}{2\in_{si}} L_s^{\ 2} = 0$$

At, x=L + L_d

$$\phi(L+L_d) = c_0 + c_1(L+L_d) + c_2(L+L_d)^2 = V_{ds} \tag{5.14}$$

$$c_0 + c_1(L+L_d) - \frac{qN_d}{2\in_{si}}(L+L_d)^2 = V_{ds} \tag{5.15}$$

From (5.14) and (5.15),

$$c_1 = \frac{V_{ds} + \frac{qN_d}{2\in_{si}}\{(L+L_d)^2 - L_s^{\ 2}\}}{(L+L_d+L_s)} \tag{5.16}$$

$$c_0 = \frac{V_{ds} + \frac{qN_d}{2\in_{si}}\{(L+L_d)^2 - L_s^2\}}{(L+L_d+L_s)} L_s + \frac{qN_d}{2\in_{si}} L_s^2 \tag{5.17}$$

Thus the applied potential along the channel can be written as,

$$\phi(x) = \frac{V_{ds} + \frac{qN_d}{2\in_{si}}\{(L+L_d)^2 - L_s^2}{(L+L_d+L_s)} L_s + \frac{qN_d}{2\in_{si}} L_s^2 + \frac{V_{ds} + \frac{qN_d}{2\in_{si}}\{(L+L_d)^2 - L_s^2}{(L+L_d+L_s)} x - \frac{qN_d}{2\in_{si}} x^2 \tag{5.18}$$

The current through one segment can be written as,

$$I_d = \frac{\phi((m+1)\Delta L) - \phi(m\Delta L)}{R(V_{gs}, V_{ds})} \tag{5.19}$$

Since all the segments are in series, the current through one segment is the total drain current through the device. Considering the complete channel the drain current expression can also be written as,

$$I_d = \frac{\phi(L) - \phi(0)}{\sum_{x=0}^{L} R(x, V_{gs}, V_{ds})} \tag{5.20}$$

5.2.2 Results, Discussion and Validation

The model developed in the chapter has been simulated in MATLAB simulation environment. Result obtained in the MATLAB simulation has been compared with the simulation result obtained from Cogenda VisualTCAD 1.8.2 2D device simulator and few experimental results available in literature. In all the simulations Fermi-Dirac statistics is used. The comparisons are shown in the figures as follows.

Fig. 5.4 and Fig. 5.5 shows transfer characteristics for channel length values L=10nm, 15nm, 20nm. In Fig. 5.4 drain current is shown in logarithmic scale while in Fig. 5.5 linear scale is used to show drain current. For shorter channel the leakage through the depleted channel in the sub threshold region is more. As a result the sub threshold current for shorter channel is higher compared to longer channel device as the channel resistance is higher for longer channel device.

Fig. 5.6 shows output characteristics for channel length values L= 10nm, 15nm, 20nm. As channel length reduces the channel resistance reduces causing a higher drain current to flow.

Fig. 5.7 shows transfer characteristics for gate oxide thickness values t_{ox}=2nm, 4nm, 6nm. Fig. 5.8 shows output characteristics for gate oxide thickness values t_{ox}=2nm, 4nm, 6nm. The decrease in gate oxide thickness results in a better control of gate over the channel which causes the subthreshold current to reduce as shown in Fig. 5.7 and Fig. 5.8.

Fig. 5.9 shows transfer characteristics for channel thickness values t_{si}=10nm, 20nm, 30nm. Fig. 5.10 shows output characteristics for channel thickness values t_{si}=10nm, 20nm, 30nm. With an increase in channel thickness the channel cross sectional area increases which results in an increase in drain current.

Fig. 5.11 and Fig. 5.12 shows transfer characteristics for drain voltage values V_{ds}=0.1V, 0.2V, 0.3V. In Fig. 5.11 drain current is shown in logarithmic scale while in Fig. 5.12 linear scale is used to show drain current. The curves are very close to each other as the effect of drain voltage on channel resistance is low.

Fig. 5.13 shows Output characteristics for gate to source voltage values V_{gs}=0.8V, 0.85V, 0.9V, 0.95V, 1V, 1.05V, 1.1V. With increase in gate voltage the depletion width reduces resulting in an increase in the drain current.

Fig. 5.14 shows the variation of drain resistance with drain voltage for different value of gate to source voltage, V_{gs}=0.8V, 0.9V, 1V. The depletion width decreases with increase in

gate voltage as the applied gate electric field opposes the internally induced electric field due to work function difference between the gate and the substrate. As a result the channel resistance decreases.

Fig. 5.15 shows transconductance variation with gate voltage for channel length values L=10nm, 15nm, 20nm. As the gate voltage increases beyond threshold value the drain current rises sharply causing an increase in the transconductance also.

Fig. 5.16 shows transconductance variation with gate voltage for drain voltage values V_{ds}=0.1V, 0.2V, 0.3V. As the drain voltage increases the variation of drain current decreases causing a decrease in transconductance.

Fig. 5.17 shows output-conductance variation with drain voltage for channel length values L=10nm, 15nm, 20nm. The higher variation of drain voltage causes the output-conductance to decrease.

Fig. 5.18 shows output-conductance variation with drain voltage for gate voltage values V_{gs}=0.8V, 0.9V, 1V. The increase in gate to source voltage causes the depletion width to reduce resulting in decrease of channel resistance. As a consequence the output-conductance decreases.

In all the simulations the gate work function is taken as ϕ_M=5.4eV and the doping concentration of the substrate is taken as $N_d=10^{19}/cm^3$. From all the plots it is seen that the model is in a close agreement with the simulated results. The average error is found to be 2.4%. Fig. 5.19 and Fig. 5.20 shows transfer characteristics and output characteristics comparison with experimental values taken from a reported work by Collinge et al. [2] in 2009. The model agrees closely with the measured value which ensures the applicability of the model. The average error is found to be 4.35%.

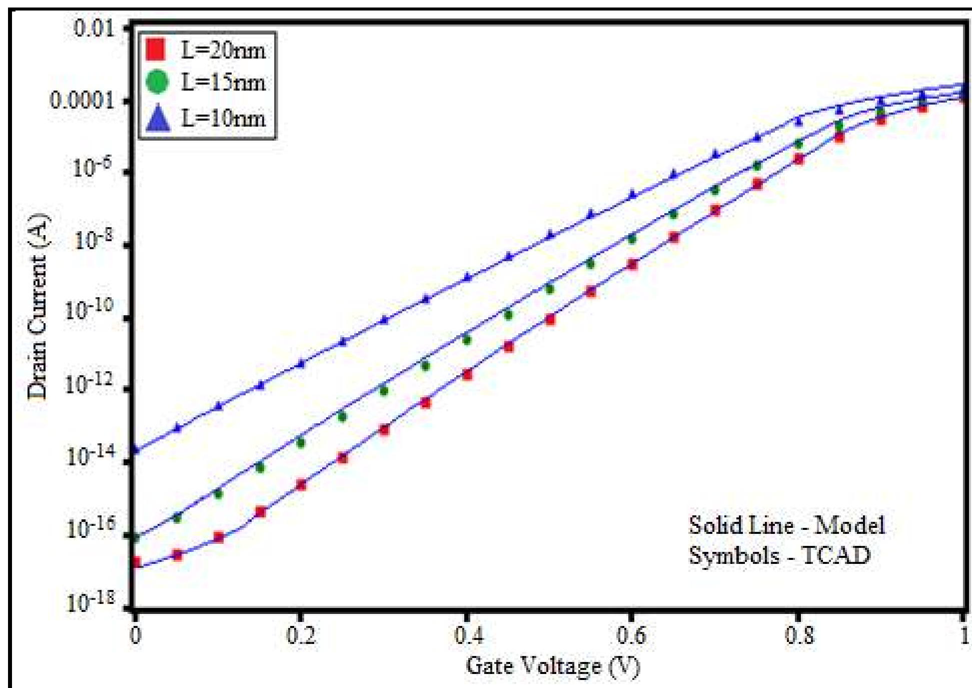

Fig. 5.4: Transfer characteristics for different value of channel length

Parameter	Value
Channel thickness (t_{si})	10nm
Gate oxide thickness (t_{ox})	2nm
Drain to source voltage (V_{ds})	0.1V
length of the source(L_s) and drain(L_d) region	5nm.

Average error = 4.1%

Maximum error =11.5%

Minimum error =0%

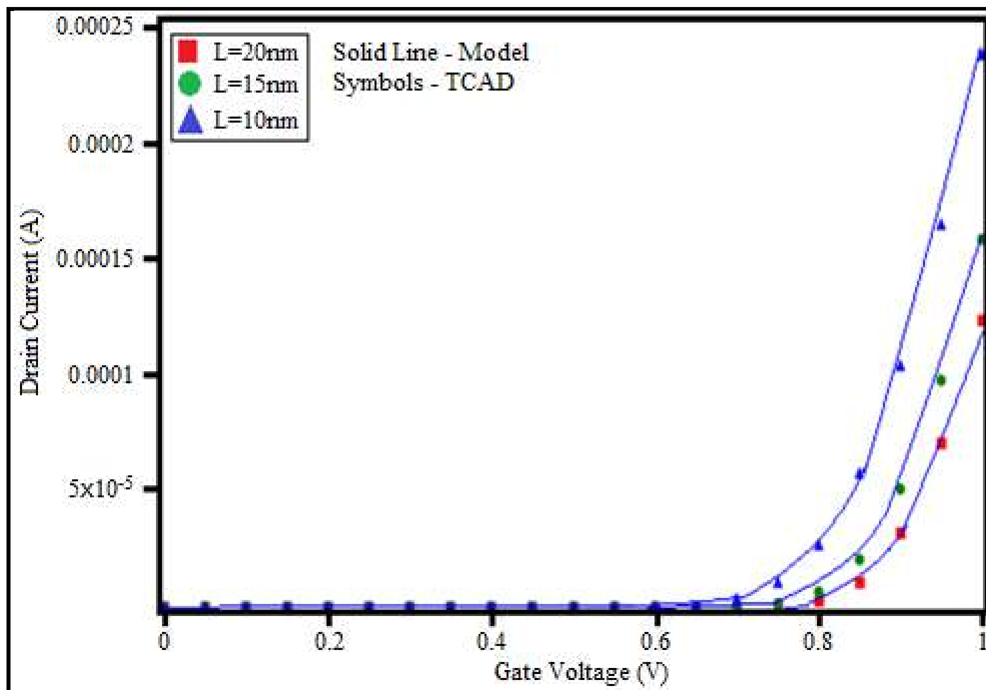

Fig. 5.5: Transfer characteristics for different value of channel length (linear scale)

Channel thickness (t_{si})	10nm
Gate oxide thickness (t_{ox})	2nm
Drain to source voltage (V_{ds})	0.1V
length of the source(L_s) and drain(L_d) region	5nm.

Average error = 4.1%

Maximum error =11.5%

Minimum error =0%

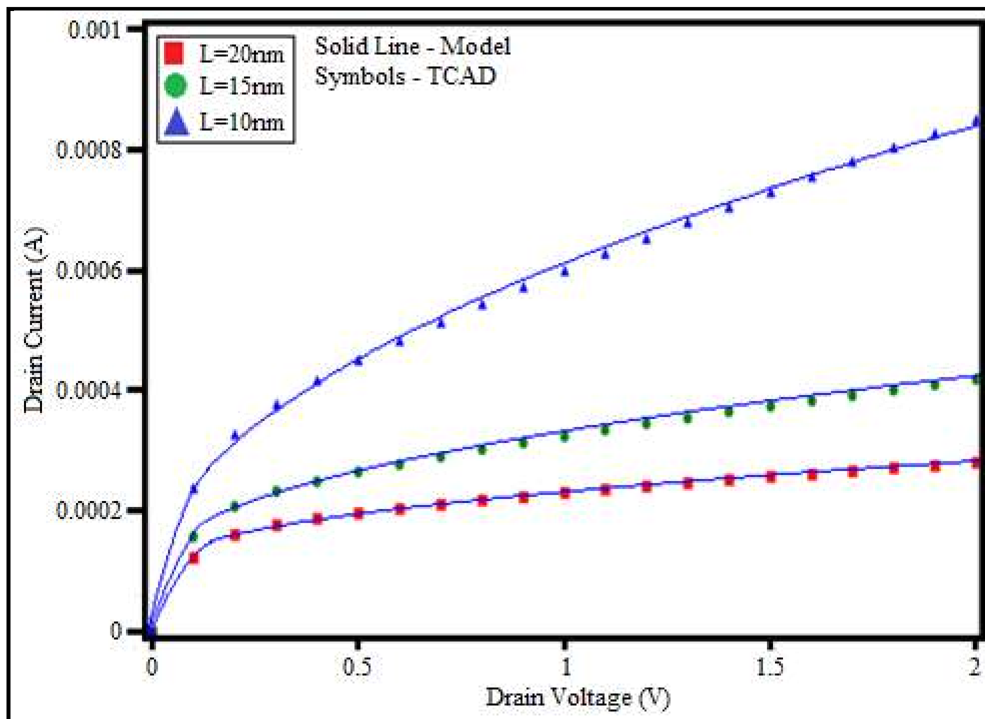

Fig. 5.6: Output characteristics for different value of channel length

Channel thickness (t_{si})	10nm
Gate oxide thickness (t_{ox})	2nm
Gate to source voltage (V_{gs})	1V
length of the source(L_s) and drain(L_d) region	5nm.

Average error = 1.8%
Maximum error =4.8%
Minimum error =0%

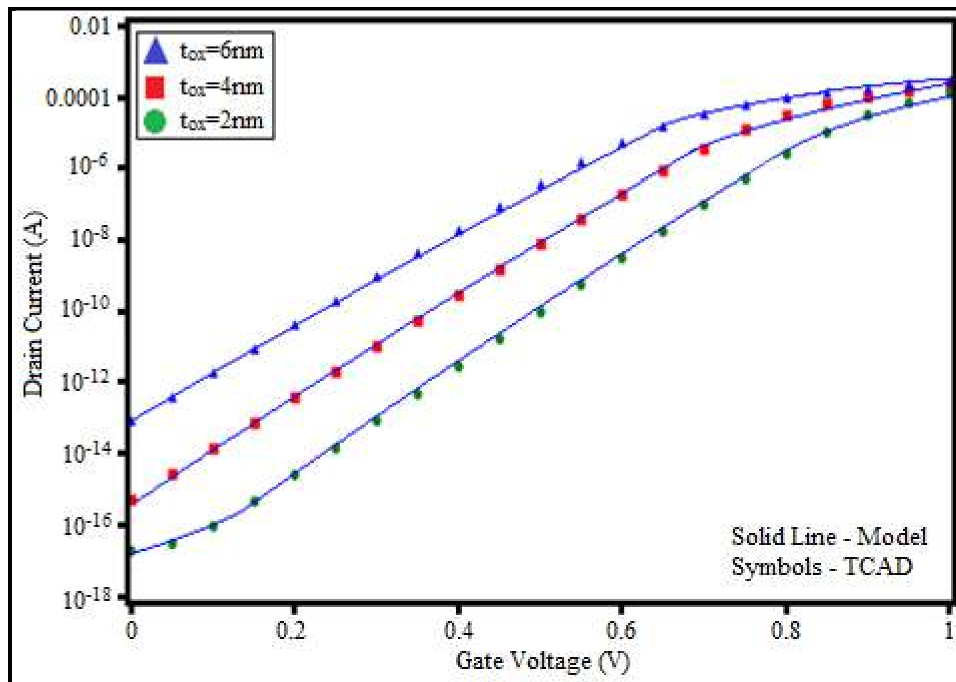

Fig. 5.7: Transfer characteristics for different value of Gate oxide thickness

Channel thickness (t_{si})	10nm
Drain to source voltage (V_{ds})	0.1V
Length of the source(L_s) and drain(L_d) region	5nm
Channel length is (L)	20nm

Average error = 2.3%
Maximum error =4.3%
Minimum error =0%

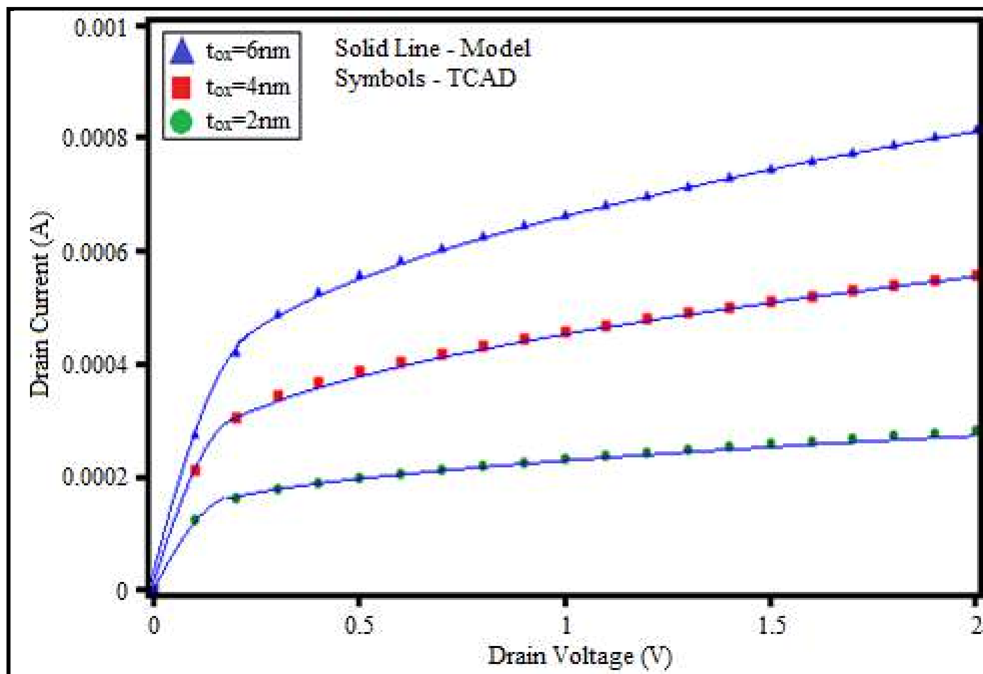

Fig. 5.8: Output characteristics for different value of Gate oxide thickness

Channel thickness (t_{si})	10nm
Gate to source voltage (V_{ds})	1V
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm

Average error = 1.4%
Maximum error =2.35%
Minimum error =0%

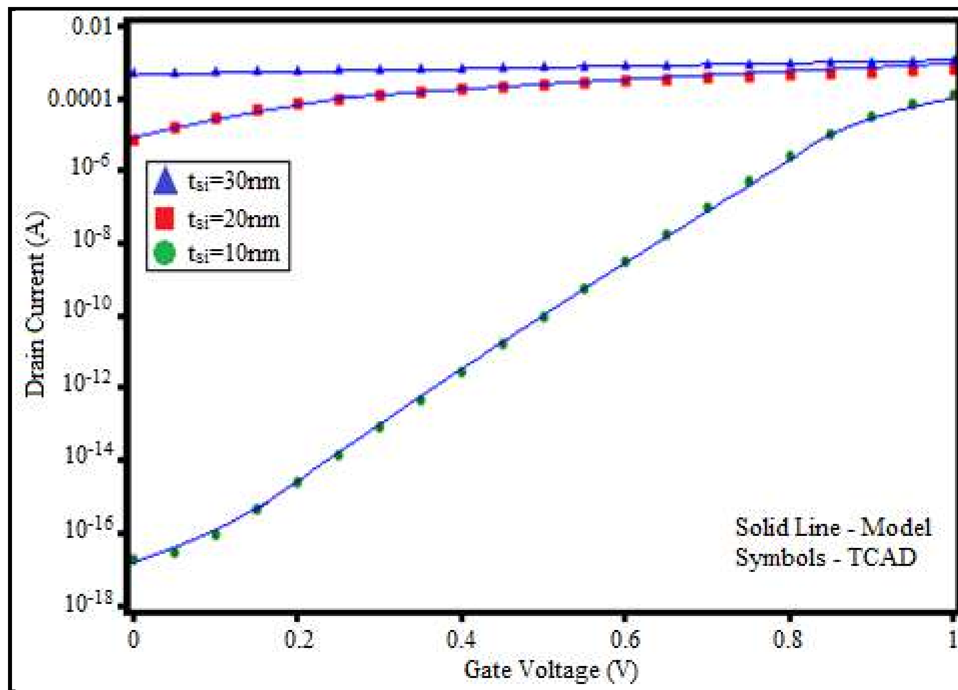

Fig. 5.9: Transfer characteristics for different value of channel thickness

Gate oxide thickness (t_{ox})	2nm
Drain to source voltage (V_{ds})	0.1V
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm

Average error = 2%
Maximum error =3.7%
Minimum error =0%

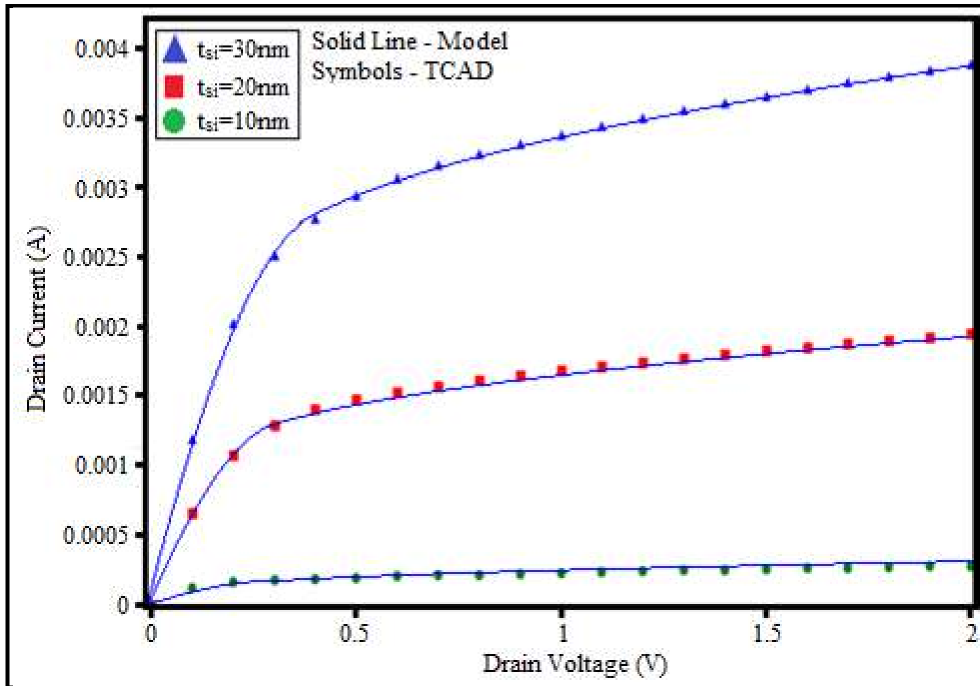

Fig. 5.10: Output characteristics for different value of channel thickness

Gate oxide thickness (t_{ox})	2nm
Gate to source voltage (V_{ds})	1V
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm

Average error = 1.3%
Maximum error =3.35%
Minimum error =0%

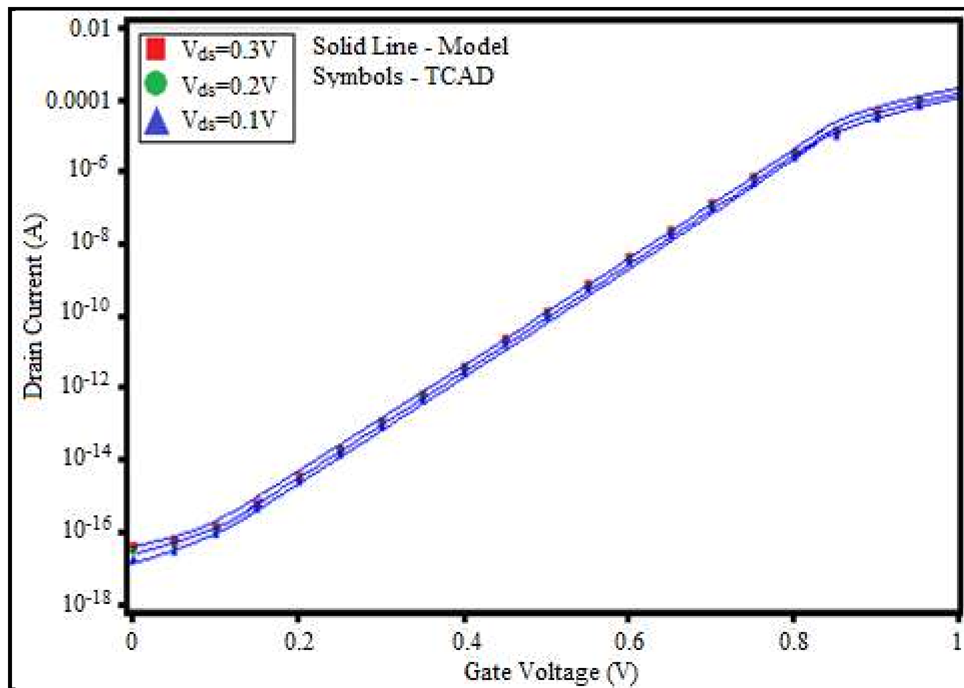

Fig. 5.11: Transfer characteristics for different value of Drain to source voltage

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm

Average error = 2.5%

Maximum error =8.9%

Minimum error =0%

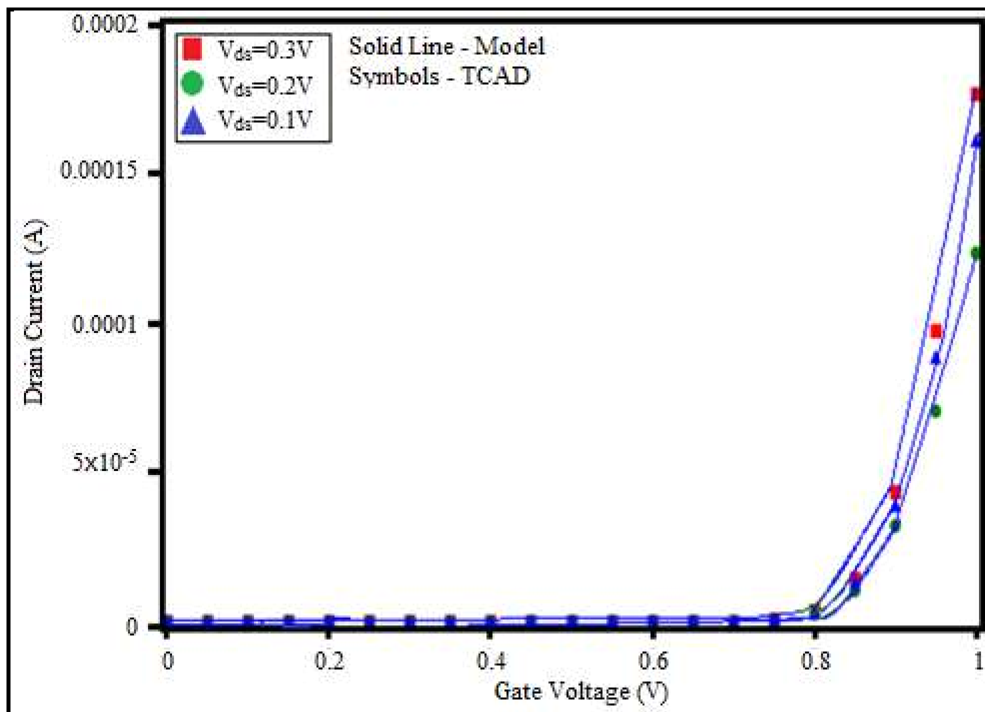

Fig. 5.12: Transfer characteristics for different value of Drain to source voltage (linear scale)

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm

Average error = 2.5%
Maximum error =8.9%
Minimum error =0%

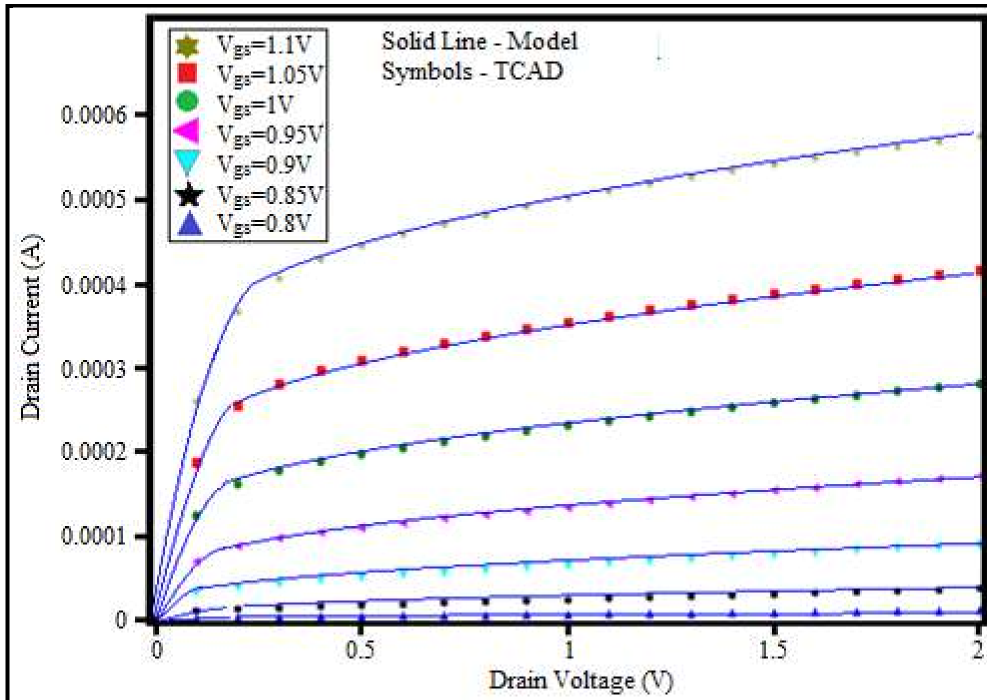

Fig. 5.13: Output characteristics for different value of Gate to source voltage

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm

Average error = 2.5%

Maximum error =4.3%

Minimum error =0%

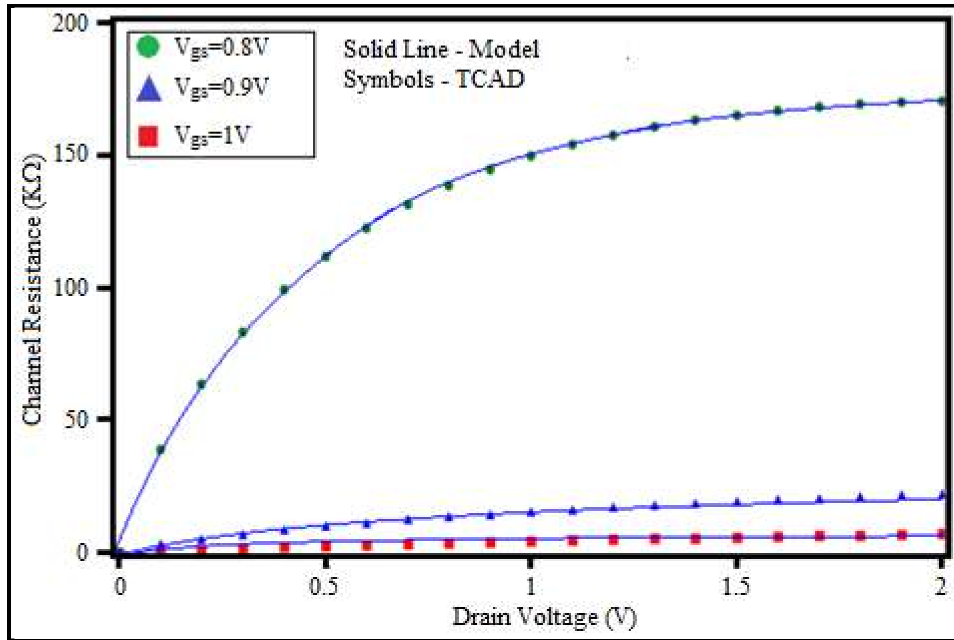

Fig. 5.14: Variation of Drain resistance with drain voltage

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Drain to source voltage (V_{ds})	0.1V
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm

Average error = 2.1%
Maximum error =4.4%
Minimum error =0%

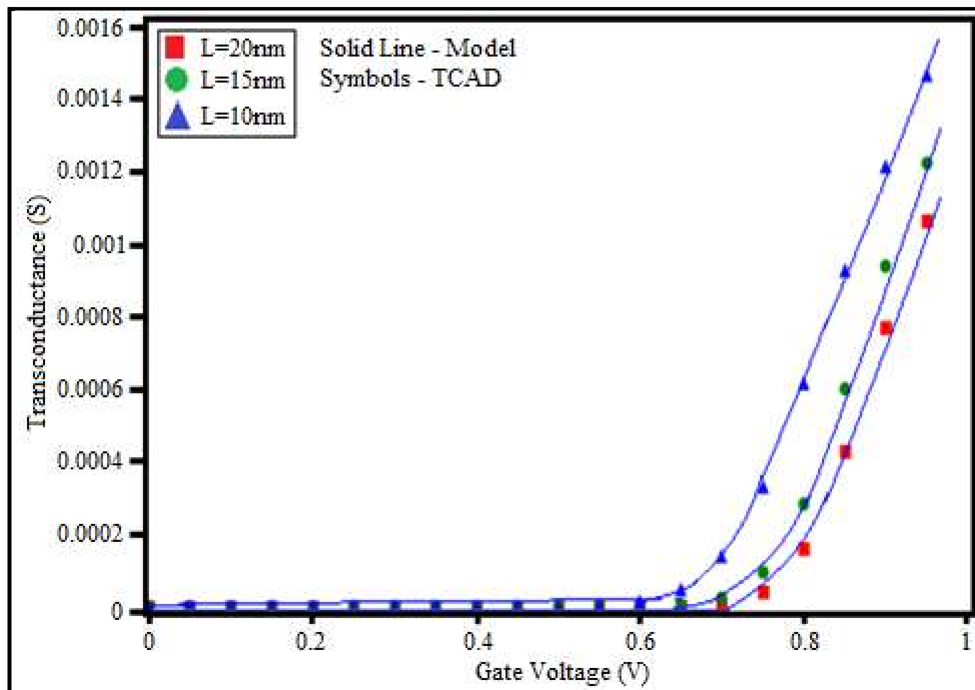

Fig. 5.15: Transconductance variation with gate voltage for different values of channel length

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Drain voltage (V_{ds})	0.1V

Average error = 1.3%
Maximum error =4.3%
Minimum error =0%

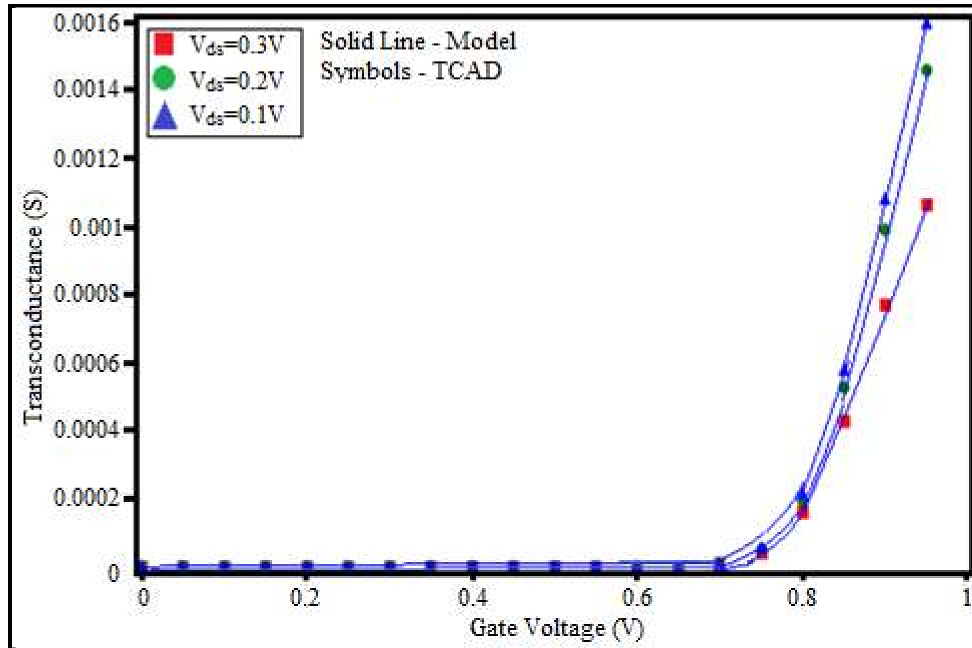

Fig. 5.16: Transconductance variation with gate voltage for different values of drain voltage

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Gate to source voltage (V_{gs})	1V
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm

Average error = 2.7%
Maximum error =6.3%
Minimum error =0%

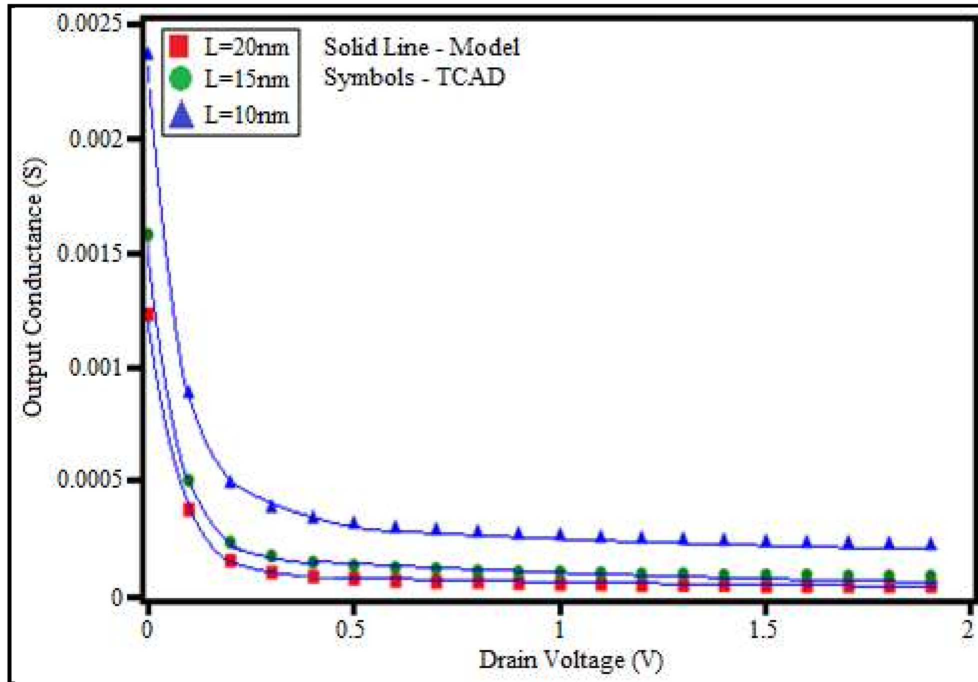

Fig. 5.17: Outputconductance variation with drain voltage for different values of channel length

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Gate to source voltage (V_{gs})	1V

Average error = 2.3%
Maximum error =4.5%
Minimum error =0%

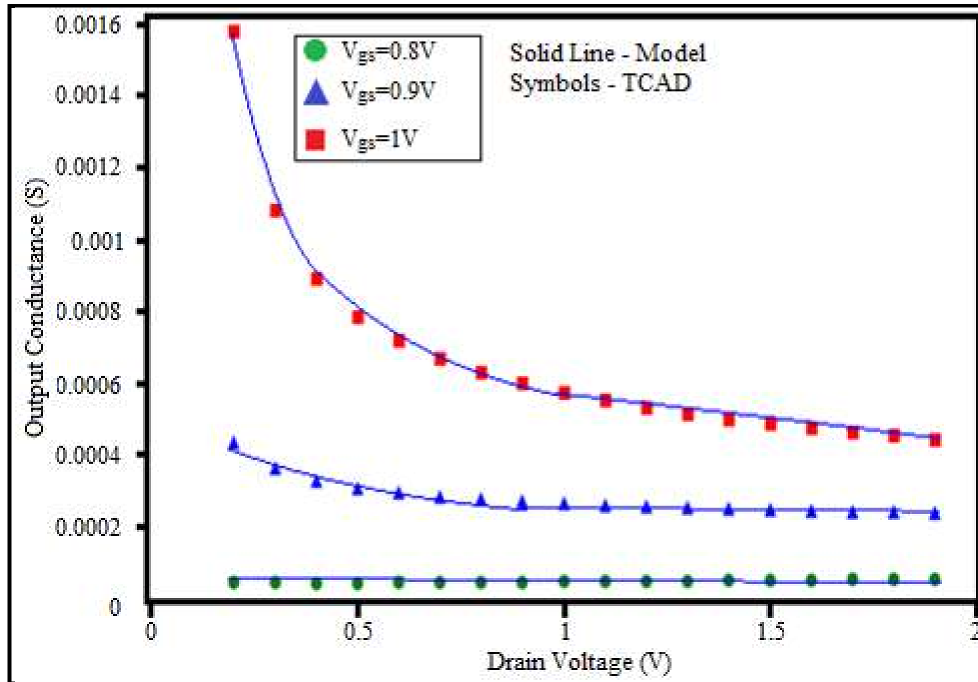

Fig. 5.18: Outputconductance variation with drain voltage for different values of gate to source voltage

Gate oxide thickness (t_{ox})	2nm
Channel thickness (t_{si})	10nm
Length of the source(L_s) and drain(L_d) region	5nm.
Channel length is (L)	20nm

Average error = 2.5%
Maximum error =5%
Minimum error =0%

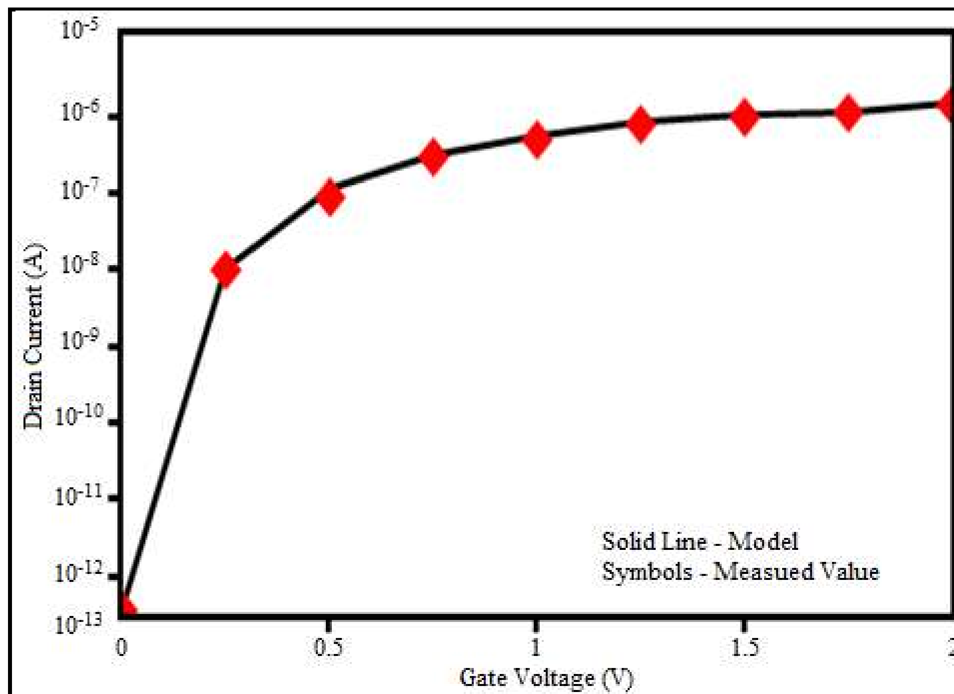

Fig. 5.19: Transfer characteristics comparison with experimental value [2]

Gate oxide thickness (t_{ox})	10nm
Channel thickness (t_{si})	10nm
Drain to Source Voltage (V_{ds})	1V
Channel length is (L)	1μm

Average error = 4.8%
Maximum error =12.2%
Minimum error =0%

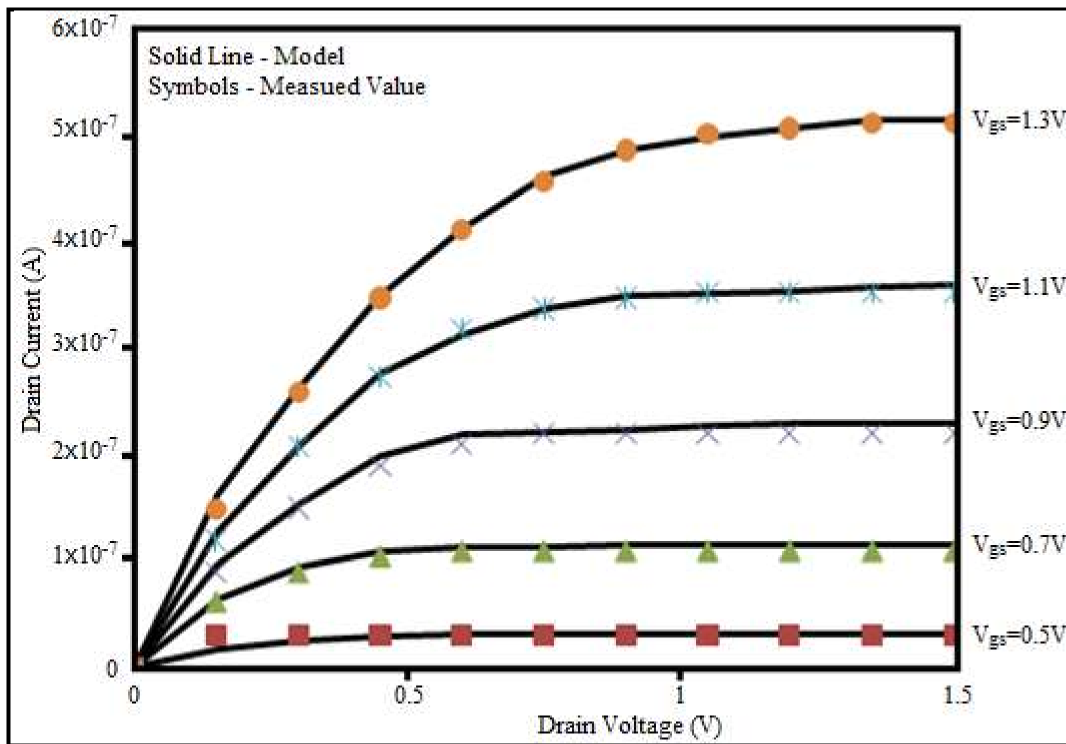

Fig. 5.20: Output characteristics comparison with experimental value [2]

Gate oxide thickness (t_{ox})	10nm
Channel thickness (t_{si})	10nm
Gate to Source Voltage (V_{gs})	0.5-1.3V
Channel length is (L)	1µm

Average error = 3.9%
Maximum error =8.7%
Minimum error =0.2%

Simulation time required for different values of drain voltage, silicon layer thickness, channel length and gate oxide thickness are given in table 5.1, table 5.2, table 5.3 and table 5.4 respectively. System configuration for simulation is

Processor	Intel(R) Core(TM) i5-3230M CPU @ 260GHz
RAM	8GB
System Type	64 bit operating system, x64-based processor
BUS speed	5 GT/s DMI

Table 5.1: Simulation time required for different drain voltages

Drain Voltage	TCAD Simulation Time	Average TCAD Simulation time	Average MATLAB Simulation time
0.1V	12 sec	0.923 sec	0.153 sec
0.2V	12.2 sec	0.938 sec	0.155 sec
0.3V	12.4 sec	0.954 sec	0.158 sec

Table 5.2: Simulation time required for different silicon layer thickness

Silicon Layer Thickness	TCAD Simulation Time	Average TCAD Simulation time	Average MATLAB Simulation time
5nm	7 sec	0.538 sec	0.148 sec
10nm	12 sec	0.923 sec	0.153 sec
15nm	15 sec	1.154 sec	0.160 sec

Table 5.3: Simulation time required for different channel length

Channel Length	TCAD Simulation Time	Average TCAD Simulation time	Average MATLAB Simulation time
10nm	10 sec	0.769 sec	0.149 sec
20nm	12 sec	0.923 sec	0.153 sec
30nm	24 sec	1.846 sec	0.176 sec

Table 5.4: Simulation time required for different gate oxide thickness

Gate Oxide Thickness	TCAD Simulation Time	Average TCAD Simulation time	Average MATLAB Simulation time
2nm	12 sec	0.923 sec	0.153 sec
4nm	10.6 sec	0.815 sec	0.145 sec
6nm	7.6 sec	0.585 sec	0.138 sec

5.4 Conclusions

A very simple and fully analytical model for drain current of a symmetric double gate JLT has been obtained. The model has been validated by using simulation results obtained from TCAD and experimental results available in literature. While comparing the simulation results obtained from MATLAB with the results obtained from TCAD, an average error of 2.4% has been observed. While an average error of 4.35% has been observed when compared with experimental results available in literature. The simulation time required for different values of drain voltage, silicon layer thickness, channel length and gate oxide thickness are also presented in this chapter. As the model developed here is analytical in nature, the simulation time required for the model simulated in MATLAB is much lower compared to TCAD simulation time.

Contributions

This chapter provides a fully analytical physics based model of drain current of a junctionless transistor which is universally applicable excluding the accumulation mode. This model is helpful in designing a JLT having considerable accuracy at a much lower computational time.

Bibliography

[1] Lee, C. W., Afzalian, A., Akhavan, N. D., Yan, R., Ferain, I., and Colinge. J. P. Junctionless Multigate Field Effect Transistor. *Applied Physics Letters*, 94(5), pages 053511, 2009

[2] Colinge J. P., Lee, C. W., Afzalian, A., Dehdashti, N., Yan, R., Ferain, I., Razavi, P., O'Neill, B., Blake, A., White, M., Kelleher, A. M., McCarthy B., and Murphy R. SOI Gated Resistor: CMOS without Junctions. In *IEEE International SOI Conference*, pages 1-2, Foster City, California, USA , 2009

[3] Nazarov, A., Balestra, F., Raskin, J. P., Gamiz, F., and Lysenko, V.S. *Semiconductor-On-Insulator Materials for Nanoelectronics Applications*, Springer, 2011

[4] Gnani, E., Gnudi, A., Reggiani, S., and Baccarani, G. Theory of the Junctionless Nanowire FET. *IEEE Transactions on Electron Devices*, 58(9), pages 2903 - 2910, 2011

[5] Colinge, J. P., Lee, H. W., Afzalian, A., Akhavan, N. D., Yan, R., Ferain, I., Razavi, P., O'Neill, B., Blake, A., White, M., Kelleher, A. M., McCarthy, B., and Murphy, R. Nanowire Transistors without Junctions. *Nature Nanotechnology*, 5, pages 225–229, 2010

[6] Colinge, J. P. Junctionless Transistors. In *IEEE International Meeting for Future of Electron Devices*, pages 1-2, Kansai (IMFEDK), 2012

[7] Colinge, J. P., Kranti, A., Yan, R., Lee, C. W., Ferain, I., Yu, R., Akhavan, N. D., and Razavi P. Junctionless Nanowire Transistor (JNT): Properties and Design Guidelines. *Solid- State Electronics*, 65–66, pages 33-37, 2011

[8] Park, C. H., Ko, M. D., Kim, K. H., Baek, R. H., Sohn, C. W., Baek, C. K., Park, S., Deen, M. J., Jeong, Y. H., and Lee, J. S. Electrical Characteristics of 20-nm Junctionless Si Nanowire Transistors. *Solid-State Electronics,* 73, pages 7–10, 2012

[9] Gnudi, A., Reggiani, S., Gnani, E. and Baccarani, G. Analysis of Threshold Voltage Variability Due to Random Dopant Fluctuations in Junctionless FETs. *IEEE Electron Device Letters*, 33(3), pages. 336–338, 2012.

[10] Lou, H., Zhang, L., Zhu, Y., Lin, X., Yang, S., He, J., and Chan M. A Junctionless Nanowire Transistor with A Dual-material Gate. *IEEE Transactions on Electron Devices*, 59(7), pages 1829–1836, 2012.

[11] Duarte J. P., Kim M. S., Choi S. J. and Choi Y. K. A Compact Model of Quantum Electron Density at The Subthreshold Region for Double-gate Junctionless Transistors. *IEEE Transactions on Electron Devices*, 59(4), pages 1008–1012, 2012.

[12] Gnudi, A., Reggiani, S., Gnani, E. and Baccarani, G. Semi Analytical Model of the Subthreshold Current in Short-Channel Junctionless Symmetric Double-Gate Field-Effect Transistors. *IEEE Transactions on Electron Devices*, 60(4), 2013

[13] Li, C., Zhuang, Y., Di, S., and Han, R. Subthreshold Behaviour Models for Nanoscale, Short-Channel Junctionless Cylindrical Surrounding-Gate MOSFETs. *IEEE Transactions on Electron Devices*, 60(11), pages 3655-3662, 2013

[14] Holtij, T., Schwarz, T., Kloes, A., and Iñiguez, B. 2D Analytical Potential Modelling of Junctionless DG MOSFETs in Subthreshold Region Including Proposal for Calculating The Threshold Voltage. In *13th International Conference on ULIS*, pages 81-84, MINATEC Grenoble, France, 2012

[15] Chiang, T. K., A New Subthreshold Current Model for Junctionless Tri-gate MOSFETs to Examine Interface Trapped Charge Effects. *IEEE Transactions on Electron Devices*, 62 (9), pages 2745–2750, 2015

[16] Chiang, T. K., A Quasi-two-dimensional Threshold Voltage Model for Short-Channel Junctionless Double-gate MOSFETs. *IEEE Transactions on Electron Devices*, 59(9) pages 2284–2289, 2012

[17] Chiang, T. K., A New Quasi-2-D Threshold Voltage Model for Short Channel Junctionless Cylindrical Surrounding Gate (JLCSG) MOSFETs. *IEEE Transactions on Electron Devices*, 59(11), pages 3127–3129, 2012

[18] Trevisoli, R. D., Doria, R. T., de Souza, M., Das, S., Ferain, I., and Pavanello, M.A. Surface Potential Based Drain Current Analytical Model for Triple Gate Junctionless Nanowire Transistors. *IEEE Transactions on Electron Devices*, 59(11), pages 3510–3518, 2012

[19] Uyemera, J. P. *CMOS Logic Circuit Design*, Kluwer Academic Publishers, 2002

[20] Paz, B. C., Avilla-Herrera, F., Cerdeira, A., and Pavenello, M. A., Double gate Junctionless Transistor Model Including Short Channel Effects. *Semiconductor Science and Technology*, 30, pages 055011, 2015

[21] Colinge, J. P. and Colinge, C. A. *Physics of Semiconductor Devices*, Kluwer Academic Publishers, 2011

[22] Gerald, T. *Ordinary Differential Equations and Dynamical Systems*, American Mathematical Society, Providence, 2011