Chapter 7

Conclusions

The thesis focuses on method for determination of scale length of four non conventional structures of JLT and modelling of depletion width, threshold voltage, potential and drain current. Moreover techniques for enhancement of two performance parameters-

- off state leakage current
- carrier mobility

has also been proposed in the thesis. The reduction of corner effect has also been presented in the thesis.

In chapter 3 scale length determination of four non-conventional structures of JLTs-pentagonal, hexagonal, octagonal and rectangular has been presented. The scale length is determined by solving Poisson's equation for transverse electrostatic potential using trial function method. The scale length varies with geometrical parameters for all the structures. A comparative study for scale length of the structures shows that in order to reduce channel length of a device the gate oxide thickness should also be decreased so that the gate controllability is maintained. Use of high-k dielectric can push the channel length minimization limit even further. The scale length decreases nonlinearly with increasing width to thickness ratio. Among the pentagonal, hexagonal, octagonal structures, the hexagonal JLT exhibits lowest value of scale length. However, the rectangular structure with a higher width to thickness ratio has a lower scale length value as compared to the hexagonal one.

These structures have not been reported so far may be due to the fabrication difficulties. As the fabrication technologies are improving rapidly, possibility of fabrication of the structures mentioned above cannot be denied. Moreover the fabrication of JLT is much simpler compared to devices with junctions. So a theoretical study has been carried out to evaluate the potential of the structures in ultranano regime. From the study it can be concluded that the hexagonal and rectangular JLT have suitability for VLSI application if it becomes possible to overcome the fabrication issues

In chapter 4 analytical model for the following parameters has been developed.

- depletion width
- threshold voltage
- potential

Depletion width model has been obtained by solving 1D Poisson's equation at moderately high doping concentration. The Poisson's equation has been solved by using trial function method and boundary conditions. The depletion width variation with doping concentration, drain to source voltage, gate to source voltage and dielectric constant for n-channel and p-channel single and double gate JLT has been shown. Depletion width for n-channel device decreases and p-channel device increases with increasing doping concentration and gate to source voltage. This is because the resultant of applied gate electric field and internal electric field is the difference between the two electric fields for n type device and the sum of the fields for p-type device for positive gate voltage. Hence a negative gate voltage has to be applied to turn on the p-type device. Depletion width for n-channel device increases and p-channel device decreases with increasing drain to source voltage. The drain to voltage also result in an electric field the direction of which is same as the direction of longitudinal electric field of n-type device and opposite in the case of a p-type device. However, depletion width for both n-channel and p-channel device increases with increase in dielectric constant of gate insulator due to increased capacitive coupling. For a single gate JLT the depletion width is found to be higher as compared to double gate device. In double gate device the lateral electric field in the central axis of the device is zero due to the cancellation of the two electric fields from the two gates.

One of the most important parameters in any MOS based switching device is the threshold voltage. The threshold voltage model for a double gate JLT has been obtained from the depletion width model. A physics based definition for threshold voltage taking into account of depletion width of the device has also been put forward in this chapter. The threshold voltage model has been simulated in MATLAB simulation environment. Result obtained in the simulation work in MATLAB has been compared with the simulation result

obtained from TCAD. The model is in a close agreement with the simulated results with an average error of 1.12%. To achieve a suitable positive threshold voltage at ultra short channel length, high doping concentration is required and the gate oxide and channel should be very thin. The model has been found to be valid for both short-channel and long-channel JLTs. The simulation time required for different values of drain voltage, silicon layer thickness, channel length and gate oxide thickness are also presented. The analytical nature of the model reduces time consumption and makes it suitable for compact modelling. Like MOSFET multi threshold voltages such as, low, regular and high threshold voltage can be offered by JLT. However, threshold voltage of JLT is higher for thinner gate oxide. Thus for JLT the gate oxide should be thin for high threshold and thick for low threshold voltage.

A complete potential model for a symmetric double gate JLT has been developed in the last part of this chapter. In this model influence of the source and drain region has also been taken into account. In this part of the chapter although the model has been developed for a symmetric double gate structure of JLT, it is possible to extend the same approach for all other structures only by varying the geometrical parameters. While taking the boundary conditions for the channel potential along the channel length, effect of source and drain region has been taken into account. The boundary conditions for source and drain potential model are derived from longitudinal potential expression of the channel. The simulation result obtained from the potential model has been compared with the TCAD simulation results and few other experimental results available in literature. The model is found to be in close agreement with TCAD simulation results as well as experimental results with an average error of 1.42% and 1.71% respectively. Since the potential in source and drain regions does not remain constant this model can show reasonable amount of accuracy at considerably lesser computation time.

In chapter 5 a new approach for the drain current modelling a symmetric double gate JLT has been presented. This approach involves the division of the channel into a number of elementary segments. The resistance of different segments are obtained from the depletion width model, which finally used to obtain the effective channel resistance. The total channel

resistance can be obtained by series combination resistances of all of the segments. The drain current can be obtained from the resistance expression by using ohm's law. The model has been simulated in MATLAB simulation environment. Result obtained in the MATLAB simulation has been compared with the simulation result obtained from Cogenda VisualTCAD 1.8.2 2D device simulator and few experimental results available in literature. The model is in close agreement with the TCAD simulation results and experimental results with an average error of 2.4% and 4.35% respectively. Most of the models reported so far are semi analytical in nature involving numerical integration. The model presented here is fully analytical which makes it useful for compact modelling.

Junctionless transistor posses numerous advantages as compared to conventional MOS devices due to absence of a junction. However, JLT suffers from several drawbacks also. Two major drawbacks of JLT that causes performance degradation of the device are-

- higher off-state current
- carrier mobility degradation

Leakage current in any MOS device imposes limitation on the gate length minimization. A method for obtaining the minimum possible gate length upto which a JLT can be scaled down is presented in this part. The gate leakage as well as drain leakage are considered for obtaining the minimum gate length of JLT. Techniques for enhancement of device performance by considering the parameters- off-state leakage current and carrier mobility has been presented in chapter 6. In order to reduce the off-state leakage current of the device a layer of dielectric has been placed at the centre of the JLT. As major portion of leakage current flows through the centre, placing a dielectric at the centre will reduce the leakage current to large extent. The drain current model for the proposed technique has also been developed. The drain current model developed in chapter 5 has been modified by considering the resistance of the dielectric at the centre. The model is simulated in MATLAB simulation environment. Result obtained in the MATLAB simulation has been compared with the simulation result obtained from Cogenda VisualTCAD 1.8.2 2D device simulator. The simulation results show that the JLT with dielectric layer placed at the centre has lower

subthreshold current compared to the conventional JLT. Two techniques for enhancement of carrier mobility of a DG JLT has also been presented in chapter 6. The first technique uses two gate dielectrics placed diagonally each other. The dielectrics used are SiO_2 and HfO_2 with dielectric constants 3.9 and 22 respectively. The second technique uses a gradual doping concentration variation in the channel with minimum at the middle and constant in the source drain region. The mobility and drain current models for the proposed techniques are developed. The models for the proposed structures has been simulated in MATLAB simulation environment. Result obtained in the MATLAB simulation has been compared with the simulation result obtained from Cogenda VisualTCAD 1.8.2 2D device simulator. Simulation study shows that the mobility in the subthreshold region for the proposed structures are less compared to the conventional one while in the on-state the proposed structures show much higher mobility compared to the conventional one. Among the proposed structures the structure with gradual variation of channel doping concentration shows the best results. This is because of lower Coulombic scattering due lower doping concentration. Transfer characteristics comparison shows that the structure has better subthreshold characteristic also. The gradual doping concentration variation retains all the features of JLT with enhanced carrier mobility.

The proposed structures for leakage current reduction and carrier mobility enhancement are implemented in a CMOS based inverter. The voltage transfer characteristics and transient responses of the structures are compared using TCAD simulation. The structure with gradual doping concentration variation and with centre dielectric shows maximum noise margin. However, the structure with centre dielectric shows higher propagation delay compared to the structures proposed for carrier mobility enhancement.

In addition to the drawbacks such as higher off-state current and reduced carrier mobility, another performance issue that is observed in some non-conventional structures of JLT such as, rectangular, pentagonal, hexagonal etc. is the corner effect. The extent of corner effect in JLT is much lower compared to the MOSFET as major portion of drain current in JLT is the bulk current. However, it may create some serious issue regarding gate

controllability in JLT also. A technique for reduction of corner effect has also been presented in this chapter. In this technique the width of the gate is reduced from both ends for all the sides of the structures. The technique is known as gate underlap. The analytical model for the proposed technique has also been developed. The same has been simulated in MATLAB. The results obtained from MATLAB has been compared with the results obtained from TCAD. The simulation shows a reduced corner effect in the structures with gate underlap.

Future Scope: In this thesis the scale length determination of four non-conventional structures of JLT has been presented. The modelling of four parameters of JLT has also been developed. Some techniques for performance enhancement of JLT has also been modelled, analyzed and presented. However, there are lot of scopes in the thesis that can be explored in future. Some of the major future scopes of the thesis are enlisted here.

1. Potential modelling by solving the Poisson's equation using different trial functions such as exponential, logarithmic, trigonometric etc..
2. There is no known way of fabrication of the structure with two dielectrics placed in a diagonal manner as it is reported for the first time. Thus the fabrication of the structure is another future scope of the thesis.