Abstract

As the VLSI design is advancing towards the end of Moore's law with MOS based devices reaching its scaling limit, concept of Junctionless Transistor (JLT) has been introduced to move further into the nanoscale regime. The thesis focuses on the modelling of various parameters as well as enhancement of two performance parameters of JLT- off state leakage current and carrier mobility and reduction of corner effect.

The first part of this work focuses on scale length determination of some non-conventional structures of JLTs. The structures considered here are- pentagonal, hexagonal, octagonal and rectangular shapes. The scale length is determined by solving Poison's equation for transverse electrostatic potential using trial function method. The scale length varies with geometrical parameters for the structures. Variation of scale length with gate oxide thickness and dielectric constant of gate dielectric for all the structures of JLT is shown. Variation of scale length with side length of pentagonal, hexagonal and octagonal JLTs and width to thickness ratio of rectangular JLTs is also shown. It can be seen that in order to reduce channel length of a device the gate oxide thickness should also be decreased so that the gate controllability is maintained. Use of high K dielectric can push the channel length minimization limit even further. The scale length decreases nonlinearly with increasing width to thickness ratio. Among the pentagonal, hexagonal, octagonal structures, the hexagonal JLT exhibits a lower value of scale length. The rectangular structure with a higher width to thickness ratio has a lower scale length value as compared to the hexagonal one.

The operation of a JLT is mainly based on the depletion width value. During off state condition, the channel is fully depleted. When the value of gate voltage is more than the threshold voltage, a neutral region is created in the channel region and the device is turned on. The drain current value increases with decreasing depletion width value. Based on this phenomena a model of depletion width of single and double gate JLT has been developed. By solving 1D Poisson’s equation the depletion width expression is obtained. The depletion width variation with doping concentration, drain to source voltage, gate to source voltage and dielectric constant variation for n-channel and p-channel single and double gate JLT is

shown. Depletion width for n-channel device decreases and p-channel device increases with increasing doping concentration and gate to source voltage while depletion width for n-channel device increases and p-channel device decreases with increasing drain to source voltage. Depletion width for both n-channel and p-channel device increases with increasing dielectric constant of gate dielectric. In all cases for single gate depletion width value is higher compared to double gate.

The threshold voltage model for double gate JLT has also been obtained from the depletion width model. A simple definition of threshold voltage based on the depletion width model is also given. For a JLT the threshold voltage can be defined as the maximum value of gate voltage at which the value of the depletion width exactly equals to the Si-layer thickness. If the gate voltage is above the threshold voltage, the depletion width value is less than the Si-layer thickness and the device is turned on. The threshold voltage model has been simulated in MATLAB simulation environment. Result obtained in the simulation work in MATLAB has been compared with the simulation result obtained from TCAD. The model is in a close agreement with the simulated results with an average error of 1.12%. To achieve a suitable positive threshold voltage at ultra short channel length, high doping concentration is required and the gate oxide and channel should be very thin. The model is valid for both short-channel and long-channel JLTs. The validation of threshold voltage model indirectly validates the depletion width model also. The simulation time required for different values of drain voltage, silicon layer thickness, channel length and gate oxide thickness are also presented. Like MOSFET multi threshold voltages such as, low, regular and high threshold voltage can be offered by JLT. However, threshold voltage of JLT is higher for thinner gate oxide. Thus for JLT the gate oxide should be thin for high threshold and thick for low threshold voltage.

The channel potential model has been used for determination of the scale length expression as well as the depletion width and threshold voltage model. The potential in the source drain region is considered to be constant throughout the length of the source and drain region. But the potential in source and drain region is not always constant as the depletion

layer of the channel extends into the source and drain region. So an approach is made towards the complete 2-D analytical potential modelling of JLT taking into account of the non uniform potential in the source and drain regions. Only a symmetric double gate structure is considered for this part of work. The same approach can be extended for other structures only by varying the geometrical parameters. The boundary conditions for channel potential along the channel length has been taken into consideration including the effect of source and drain region. The boundary conditions for source and drain potential model has been derived from longitudinal potential expression of the channel. The potential model has been simulated in MATLAB simulation environment. Result obtained in the MATLAB simulation has been compared with the simulation result obtained from TCAD and few experimental results available in literature. The model is in close agreement with TCAD simulation results and experimental results with an average error of 1.42% and 1.71% respectively. This model is very useful for compact modelling as the model is fully analytical.

A fully analytical approach for drain current modelling of a symmetric double gate junctionless transistor has also been developed in this work. In this approach the channel is divided into a number of elementary segments where length of each segment equal to the diameter of a silicon atom. Each of the segments may consists of either a depletion region or a neutral semiconductor region or both. When the value of gate voltage lies between threshold voltage and flatband voltage, a segment can be considered as parallel combination of three resistances, i.e., one non-depleted layer resistance and other two are depleted layer resistances. In the subthreshold region the equivalent resistance reduces to a single depletion layer resistance and in the flatband region it reduces to a single non-depletion layer resistance. The equivalent resistance and potential difference for each segment is determined and hence using ohms law, current through each segment is determined. The current through one segment is nothing but the drain current flowing through the channel. The model has been simulated in MATLAB simulation environment. Result obtained in the MATLAB simulation has been compared with the simulation result obtained from Cogenda VisualTCAD 1.8.2 2D device simulator and few experimental results available in literature.

The model is in close agreement with the TCAD simulation results and experimental results with an average error of 2.4% and 4.35% respectively.

In the last part of the thesis, emphasis has been given on performance enhancement of JLT. Two performance parameters of JLT has been taken into account in this part of the work.

- The off state leakage current and
- The carrier mobility

In JLT the channel region should be fully depleted in order to turn it off. To achieve full depletion the gate material should have high work function value as well as the body should be thin enough. If this criteria is not taken care of then the leakage current will be high and the achievement of proper turn off condition will not be possible. Leakage current in any MOS devices imposes limitation on the gate length minimization. A method for obtaining the minimum possible gate length upto which a JLT can be scaled down is presented in this part. The gate leakage as well as drain leakage are considered for obtaining the minimum gate length of JLT. A high-k gate dielectric can be used to reduce the leakage current. However most of the high k dielectrics are not compatible with Silicon. Use of high-k dielectric also leads to reduction of carrier mobility. So a new technique for leakage current reduction as well as improvement of subthreshold slope is proposed here. In this technique a layer of dielectric has been placed at centre of the JLT. As major portion of leakage current flows through the centre, placing a dielectric at the centre will reduce the leakage current to large extent. Simulation study is done for the method using TCAD. The simulation results show that the JLT with dielectric layer placed at the centre has lower subthreshold current compared to the conventional JLT. Two techniques are also proposed to enhance the carrier mobility of a DG JLT. The first technique uses two gate dielectrics placed diagonally each other. The dielectrics used are SiO_2 and HfO_2 with dielectric constants 3.9 and 22 respectively. The second technique uses a gradual doping concentration variation in the channel with minimum at the middle and constant in the source drain region. Simulation

study for the structures is done using TCAD. Simulation study shows that the mobility in the subthreshold region for the proposed structures are less compared to the conventional one while in the on state the proposed structures show much higher mobility compared to the conventional one. Among the proposed structures the structure with gradual variation of channel doping concentration shows the best results. Transfer characteristics comparison shows that the structure has better subthreshold characteristic also. The gradual doping concentration variation retains all the features of JLT with enhanced carrier mobility.

The proposed structures for leakage current reduction and carrier mobility enhancement are implemented in a CMOS based inverter. The voltage transfer characteristics and transient responses of the structures are compared using TCAD simulation. The structure with gradual doping concentration variation and with centre dielectric shows maximum noise margin. However, the structure with centre dielectric shows higher propagation delay compared to the structures proposed for carrier mobility enhancement.

In addition to the drawbacks such as higher off-state current and reduced carrier mobility, corner effect is also observed in some non-conventional structures of JLT such as, rectangular, pentagonal, hexagonal etc. In such devices two electric flux lines at the corner are not parallel and mutually crossed at a point away from the oxide semiconductor interface. At that point the resultant electric field is considerably higher causing premature local turn on of the device. A technique for reduction of the corner effect is also presented, modelled and analyzed. The width of the gate is reduced from both ends for all the sides of the structures. The technique is termed as gate underlap. The model for the proposed technique has been simulated in MATLAB simulation environment. Result obtained in the MATLAB simulation has been compared with the simulation result obtained from TCAD. The simulation shows a reduced corner effect in the structures with gate underlap.