# List of Publications

## Journal Publications

[1] Sarma, K. C. D. and Sharma, S. An Approach for Complete 2-D Analytical Potential Modelling of Fully Depleted Symmetric Double Gate Junction Less Transistor. *Journal of Computational Electronics*, 14(3), pages 717-725, 2015.

[2] Sarma, K. C. D. and Sharma, S. Scale Length Determination of Gate All Around (Regular Hexagonal Cross Section) Junctionless Transistor. *International Journal of Applied Engineering Research (IJAER)* , 10(2), pages 4751-4762, 2015.

[3] Sarma, K. C. D. and Sharma, S. Carrier Mobility Enhancement of Symmetric Double Gate Junctionless Transistor. *Journal of Nanoelectronics and Optoelectronics*, Accepted.

[4] Sharma, S. and Sarma, K. C. D. An Analytical Approach for Drain Current Modelling of A Symmetric Double Gate Junctionless Transistor. *Journal of Nanoelectronics and Optoelectronics*, Accepted.

## Book Chapter

[5] Sarma, K. C. D. and Sharma, S. A Review on Evolution of MOSFET with Special Emphasis on Junctionless Transistor, In Ajaykumar, B. S. and Sarkar, D., editors, *Advanced Engineering Research and Applications*, ISBN:978-93-84443-48-1, Research India Publications, Accepted.

## Conference Publications

[6] Sarma, K. C. D. and Sharma, S. Scale Length Determination of Gate All Around (Regular Pentagonal Cross Section) Fully Depleted Junctionless Transistor. In *IEEE International Conference on Advances in Engineering and Technology Research (ICAETR)*, Dr. Virendra Swarup Group of Institutions, Unnao, UP, pages 1-5, 1-2 August, 2014.

[7] Sarma, K. C. D. and Sharma, S. Scale Length Determination of Gate All Around (Octagonal Cross Section) Junctionless Transistor. In *International Conference on Electronic Design, Computer Networks & Automated Verification (EDCAV)*, NIT, Meghalaya, pages 1-5, 29-30 January, 2015.

[8] Sarma, K. C. D. and Sharma, S. A Method for Determination of Depletion Width of Single and Double Gate Junction Less Transistor. In *International Conference on Electronic Design, Computer Networks & Automated Verification (EDCAV)*, NIT, Meghalaya, pages 114-119, 29-30 January, 2015.

[9] Sarma, K. C. D., Sharma, S., and Hazarika, C. Scale Length Determination of a Fully Depleted Surrounding Gate (Rectangular Cross Section) Junction Less Transistor. In *International Conference on Electrical, Electronics, Signals, Communication & Optimization-EESCO*, pages 1-4, Visakhapatnam, Andhra Pradesh, 24-25 January, 2015.

**Papers Under review**

[10] Sarma, K. C. D. and Sharma, S. An Analytical Method for Determination of Threshold Voltage of A Symmetric Double Gate Junction less Transistor. *Journal of Low Power Electronics*.

[11] Sarma, K. C. D. and Sharma, S. A Novel Method for Reducing the Off State Leakage Current in Symmetric Double Gate Junction less Transistor. *IETE Journal of Research*.