Chapter 3

Threshold voltage modeling using capacitance voltage characteristics

3.1 Introduction

Threshold voltage is an important electrical parameter for any field effect transistor (FET) device since it indicates the onset of a significant flow of the drain current. When the applied gate voltage is equal to the value of threshold voltage of the device, it results in the transition from weak to strong inversion [1-4]. Various methods are available to determine the threshold voltage based on the measurement of the transfer characteristics of the devices. Many of them involve the use of strong inversion region and some employ the weak inversion region [5-12]. In one of the methods proposed by Sasaki et al. involving the strong inversion region, transconductance is calculated from the measured drain current and the gate voltage for the maximum transconductance (g_m) is found. Further, from the slope and the intercept of $I_d/(g_m)^{0.5} = (\beta V_d)^{0.5} (V_G - V_t)$ plot the threshold voltage is obtained [7]. Hardillier et al. devised a technique to calculate the threshold voltage as the function of mobility attenuation factor, source drain series resistance and variation of low field mobility [8]. A simpler method of measuring threshold voltage using GMLE method (transconductance g_m -linear-extrapolation method) was put forward by Tsuno et al. [9]. Inspite being simple and effective these methods had the disadvantage of being dependent on parasitic components for the threshold voltage calculation and any change in these components have a significant effect on the threshold voltage calculation. To mitigate these unwanted effects, methods have been employed where capacitance has been considered as a function of voltage. A technique for threshold voltage calculation using a gate to substrate capacitance was proposed by Lau et al [13-14]. This method though independent of drain to source resistance or mobility factor requires elaborate high resolution equipment for measurement. In this work, a comparatively simple theoretical method to obtain the threshold voltage based on capacitance voltage characteristics is stated. It is to be noted that the MOS structure though it resembles a capacitor; its capacitance is not merely a ratio of charge to voltage. Rather the voltage is not only the function of charges stored but also depends on the surface potential. It is infact a capacitor that consists of gate oxide as well as depletion capacitance. Therefore for precise modeling of threshold voltage capacitance voltage characteristics can be considered. This will help to minimize

the error in the measuring process as an accuracy of the model depends upon the appropriate parameters considered for threshold voltage extraction.

3.2 Theory

The threshold voltage for a semiconductor device can be defined in numerous ways such as [15]

- i) The gate voltage at which the inversion charge density is equal to zero.
- ii) The gate voltage at which the channel current is linearly extrapolated to zero for the non-saturated region of MOSFET.
- iii) Gate voltage at which the surface potential becomes twice the bulk Fermi potential.

The third definition explicitly relates surface potential to the threshold voltage [15].

The flatband voltage is the summation of work function difference between the metal and semiconductor along with the potential due to trapped, mobile ionic and fixed charges of the oxide layer as depicted by equation 3.1.

$$V_{fb} = \phi_m - \phi_{Si} + \frac{(Q_f + Q_m + Q_{tt})}{C_{ox}}$$
(3.1)

Here, $\phi_m - \phi_{Si}$ is the work function difference between metal and semiconductor

 Q_f is the fixed charge (within 3nm of Si-SiO₂)

- Q_m is the mobile ionic charge
- Q_{tt} is the oxide trapped charge

In an ideal case, the flatband voltage is considered to be zero. Therefore from Shockley's model, the threshold voltage is considered to be the summation of surface potential and voltage across the oxide layer.

3.3 Proposed model description

In the proposed model, threshold voltage of a MOSFET based on MOS capacitance property has been presented. The MOS capacitance variation in the depletion region is taken as the basis for the threshold voltage modeling. A change in the space charge width brings a change in the voltage across the depletion layer and also the input capacitance. Dividing the whole space charge width into smaller depleted layers, the summation of the individual voltages of each depleted layers at the maximum width gives the threshold voltage of the MOSFET.

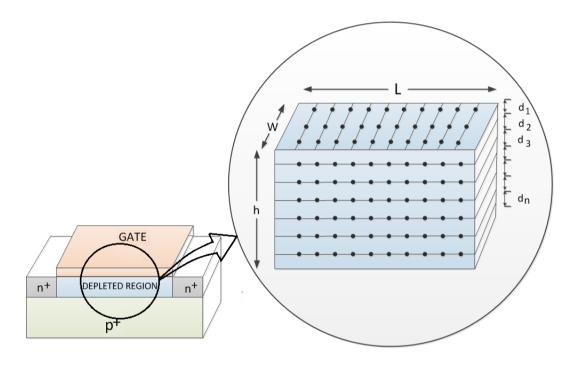


Figure 3.1 The depleted regions assumed to be in a rectangular shape, with the atoms at equidistant from each other in the same plane and also in the adjacent plane

In this model as illustrated in figure 3.1, the depletion layer of the device, where the charges present are considered to be prorated into equidistant crystallographic planes. These planes are assumed to have the same atomic planar density and also the atoms present in each plane are considered to be equidistant. Therefore, the maximum depletion width in the direction of depth is the summation of each equal depth planes, i.e. if the maximum depth is W_m , then $W_m = d_1 + d_2 + d_3 \dots + d_n$. Here $d_1 = d_2 = d_3 \dots = d_n$, where *n* being the total number of layers. The number of layers varies with the concentration of the dopants and it is the ratio of the maximum depletion depth to the depth of a single layer.

Boron is assumed to be diffused into the semiconductor at a temperature of 1000° C for an hour. The diffusion length obtained is 1.687×10^{-7} m governed by the formula $2\sqrt{DT}$. Here *D* is the diffusion coefficient of Boron and *T* is the time of diffusion.

The diffusion length is taken as the height of the rectangular planes (*h*). For the mathematical formulation length (*L*) and width (*W*) is considered as 500nm and 1µm respectively. Atoms present in this volume ($L \times W \times h$) are 848.5×10⁻³ number/volume. The distance between atoms in the first plane i.e. d_1 is given by

$$d_1 = 3\sqrt{\frac{(L \times W \times h)}{848.5 \times 10^{-3}}} = 4.6415 \times 10^{-7} m$$

The maximum depletion width (W_m) of the depletion region is given by the formula [4]

$$W_m = 2\sqrt{\frac{\varepsilon_{si}kT\ln\left(\frac{N_a}{n_i}\right)}{q^2N_a}}$$
(3.2)

Here thermal voltage kT/q is 0.026V (300K), intrinsic carrier concentration of silicon $n_i = 1.5 \times 10^{10}$ /cm³, permittivity of silicon $\varepsilon_{si} = 11.68\varepsilon_o$, W_m is calculated as 6.8942×10^{-6} m. Since the diffusion length is smaller than the maximum depletion (which is not possible) hence a factor (*h*) is introduced which is the ratio of diffusion length to the maximum depletion width. For the concentration of 10^{13} atoms/cm³, *h* is found to be 0.0244. This factor is to be multiplied with the bulk voltage (factor *h* is to be considered till the concentration is 10^{16} atoms/cm³. Beyond that, *h* becomes greater than unity and the factor is not considered).

The number of dopants along the Length is denoted by N_L and is given by

$$N_L = \frac{L}{d_1} + 1 \tag{3.3}$$

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Width is denoted by N_W and is given by

$$N_W = \frac{W}{d_1} + 1 \tag{3.4}$$

Therefore, charge per sheet, denoted by Q_{sh} and is expressed as

$$Q_{sh} = q N_L N_W \tag{3.5}$$

Charge per unit area is denoted by Q_b which is given by

$$Q_b = \frac{Q_{sh}}{(L \times W)} \tag{3.6}$$

Total number of depleted layers in the depletion region, assuming the planes to be rectangular in nature is

$$n = \frac{W_m}{d_1} \tag{3.7}$$

Therefore, for the dopant concentration of 10^{13} atoms/cm³, N_L = 1.077 and N_W = 2.15447. Q_{sh} and Q_b are found to be 3.7133×10^{-19} C and 7.4266×10^{-7} C /m² respectively. Using these values the *n* is found to be 14.8.

The capacitance of each layer has been calculated. The equation 3.8 illustrates the capacitance for the first layer d_1

$$C(1) = \frac{1}{\left[\frac{X_{ox}}{\varepsilon_{ox}} + \frac{d_1}{\varepsilon_{si}}\right]}$$
(3.8)

$$V(1) = \frac{Q_b}{C(1)} \tag{3.9}$$

Similarly, for d_2 the capacitance can be expressed as

$$C(2) = \frac{1}{\left[\frac{X_{ox}}{\varepsilon_{ox}} + \frac{d_1}{\varepsilon_{si}} + \frac{d_2}{\varepsilon_{si}}\right]}$$
(3.10)

As, $d_1 = d_2$ equation (3.10) becomes –

$$C(2) = \frac{1}{\left[\frac{X_{ox}}{\varepsilon_{ox}} + 2 \times \frac{d_1}{\varepsilon_{si}}\right]}$$
(3.11)

$$V(2) = \frac{Q_b}{C(2)} \tag{3.12}$$

The value of Q_b changes with the increase in distance

Together, for n number of layers, capacitance will be given by

$$C(n) = \frac{1}{\left[\frac{X_{ox}}{\varepsilon_{ox}} + n \times \frac{d_1}{\varepsilon_{si}}\right]}$$
(3.13)

As $d_1 = d_2 = \dots = d_n$

$$V(n) = \frac{Q_b}{C(n)} \tag{3.14}$$

Therefore, the threshold voltage of the proposed model can be expressed as the summation of voltages across the *n* number of d_1 layers.

$$V_{th(proposed)} = \sum_{i=1}^{n} V(i)$$
(3.15)

The threshold voltage obtained from the proposed model can be compared with the standard equations of Shockley's model which is [1, 4]

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$$V_{th(\text{standard})} = V_{fb} + 2 |\phi_f| + \frac{Q_{depletion}}{C_{ox}}$$
(3.16)

Here,

$$\phi_f = V_T \ln\left(\frac{N_a}{n_i}\right) \tag{3.17}$$

$$Q_{depletion} = \sqrt{2\varepsilon_{si}N_a 2\phi_f} \tag{3.18}$$

$$C_{ox} = \frac{\mathcal{E}_{ox}}{x_{ox}} \tag{3.19}$$

Where ϕ_f is the Fermi level potential, $Q_{depletion}$ is the bulk charges present, C_{ox} is the oxide gate capacitance per unit area. The flatband voltage is considered to be ideally zero.

The threshold voltage derived from the proposed model is compared with that of the Shockley's model using the standard equations (3.15, 3.16, 3.17, 3.18) [1, 4].

3.4 Current voltage characteristics

The equation of the drain current in the non-saturated or linear region for a MOSFET is given by [4]

$$I_d = \mu_n \times C_{ox} \times \frac{W}{L} \times \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$
(3.20)

And for saturated region is given by [4]

$$I_d = \mu_n \times C_{ox} \times \frac{W}{2L} \times (V_{GS} - V_{th})^2$$
(3.21)

3.5 Model extended to ISFET device

The MOS structure has a metal region present above the gate oxide. This metal layer can be removed and replaced by a reference electrode and an electrolyte solution. Such a structure is called an insulator semiconductor structure (EIS) and is analogous to the MOS structure of MOSFET [2]. The threshold voltage of this EIS structure of ISFET device is given as [2]

$$V_{th(ISFET)} = (E_{ref} + \phi_{lj}) - (\phi_{eo} - \chi_{sol}) - \phi_{si} + \frac{|Q_{depletion}|}{C_{ox}} + 2|\phi_{f}| + \frac{(Q_{f} + Q_{m} + Q_{tt})}{C_{ox}}$$
(3.22)

$$V_{fb} = (E_{ref} + \phi_{lj}) - (\phi_{eo} - \chi_{sol}) - \phi_{si} + \frac{(Q_f + Q_m + Q_{tt})}{C_{ox}}$$
(3.23)

Where

 E_{ref} is the reference electrode potential relative to vacuum

 ϕ_{lj} is the liquid-junction potential difference between the reference solution and the electrolyte

 ϕ_{eo} is the potential drop in the electrolyte at the insulator-electrolyte interface

 χ_{sol} is the surface dipole potential of the solution

 ϕ_{si} is the work function of silicon in volts.

In the expression of threshold voltage for MOSFET as expressed in equation 3.16, the flatband term (V_{fb}) also comprise of the work function difference between the metal and the semiconductor (The trapped charges, interface charges and the fixed immobile charges are neglected in further equations). Therefore substituting equation (3.16) in equation (3.22), the threshold voltage of ISFET can be written as-

$$V_{th(ISFET)} = V_{th(MOSFET)} + E_{ref} + \phi_{lj} + \chi_{sol} - \phi_{eo} - \phi_m$$
(3.24)

The proposed MOSFET model can be extended to ISFET as stated in equation

$$V_{th(ISFET-proposed)} = V_{th(MOSFET-proposed)} + E_{ref} + \phi_{lj} + \chi_{sol} - \phi_{eo} - \phi_m \qquad (3.25)$$

Here ϕ_m is the work function of the metal relative to vacuum in volts.

3.6 Results and Discussion

The model proposed for MOSFET has been simulated using MATLAB and it has been compared with the existing Shockley model. Simulations have been carried out for different dopant concentrations ranging from 10^{13} to 10^{20} /cm³. Mirabella et al. in their work have reported high doping concentration of boron in the range of 10^{20} /cm³ [16]. Hence, simulations of the model have been carried out upto maximum possible concentration of boron doping in silicon. The threshold voltage obtained using both the model is tabulated in the table 3.1.

Table 3.1. Table for comparison of the threshold voltage of MOSET calculated by the proposed model and the standard formulae

Concent	d ₁ (m)	$W_m(m)$	n	$Q_b(Cm^{-2})$	V_{th}	Qdepletion	φ _f	$V_{th}(V)$
-ration			(number		Proposed	(C)	(V)	Standard
N _a (cm ⁻³)			of layers)		model(V)			formulae
10 ¹³	4.64×10 ⁻⁷	6.89×10 ⁻⁶	14.8	7.42×10 ⁻⁷	0.349	1.03×10 ⁻⁵	0.18	0.343
10 ¹⁴	2.15×10 ⁻⁷	2.51×10 ⁻⁶	11.6	5.99×10 ⁻⁶	0.531	3.79×10 ⁻⁵	0.24	0.478
10 ¹⁵	1×10 ⁻⁷	8.89×10 ⁻⁷	8.89	2.11×10 ⁻⁶	0.663	1.28×10 ⁻⁴	0.30	0.656
10 ¹⁶	4.64×10 ⁻⁸	3.07×10 ⁻⁷	6.6	7.74×10 ⁻⁵	0.985	5.19×10 ⁻⁴	0.36	0.975
10 ¹⁷	2.15×10 ⁻⁸	1.05×10 ⁻⁷	4.88	3.60×10 ⁻⁴	1.83	1.37×10 ⁻³	0.41	1.776
10 ¹⁸	1×10 ⁻⁸	3.55×10 ⁻⁸	3.55	1.64×10 ⁻³	4.24	6.4×10 ⁻³	0.47	4.18
10 ¹⁹	4.64×10 ⁻⁹	1.19×10 ⁻⁸	2.5	7.53×10 ⁻²	12.18	1.48×10 ⁻²	0.53	11.96
10 ²⁰	2.15×10 ⁻⁹	3.97×10 ⁻⁹	1.8	0.34×10 ⁻¹	37.62	6.89×10 ⁻²	0.59	37.58

The detailed comparison of the threshold voltage calculated by the proposed model and the standard formulae (Shockley's model) for MOSFET is illustrated in figure 3.2. The dopant concentration is made to vary from the range of 10^{13} to 10^{20} /cm³ and the corresponding threshold voltage is plotted against the respective dopant concentration. It is observed that the proposed model is in agreement with existing standard formulae. Minimum, maximum and the average error percentage between the threshold voltage calculated by proposed and existing model is 0.09%, 9.83% and 2.52% respectively.

Further, in the succeeding plot as depicted in figure 3.3, the comparison has been presented for the output characteristics of the MOSFET. The dopant concentration considered is 10^{13} /cm³ and the drain characteristics are plotted for the models with the gate voltages 2.5V, 2.7V and 3V. The plot exhibits that the current voltage characteristics obtained using the proposed model and that of standard formulae are in reasonable agreement with each other. From the output characteristics of the proposed model and existing model it was observed that error percentage:- when V_{GS} = 2.5V; the minimum error is 0%, maximum error is 0.41%, when V_{GS} = 2.7V; minimum error is 0.93%, average error is 0.40% and when V_{GS} =3V; minimum error is 0%, maximum error is 0.83% and average error is 0.49%.

Further, the model has been extended for ISFET with Ag/AgCl as the reference electrode. Here, the variation of the threshold voltage for an ISFET device (considering the MOSFET models for the dopant concentration of 10^{13} cm⁻³) is plotted as depicted in figure 3.4. Minimum, maximum and average error percentage between the threshold voltages of the ISFETs (existing and proposed model) is found to be 0.70%, 1.29% and 0.93% respectively.

In figure 3.5, the I_D versus V_{DS} (output characteristics) for the ISFET device using both the MOSFET model is illustrated. Error percentage:- for pH 4, minimum error is 0.51%, maximum is 1.0% and average is 0.715%; for pH 7, minimum error is 0.54%, maximum error is 1.07% and average is 0.755%; for pH 10, minimum error is 0.58%, maximum error is 1.14% and average error is 0.86%.

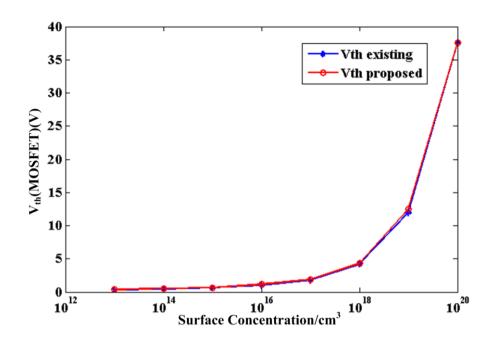


Figure 3.2. The plot showing the comparison of threshold voltage of MOSFET calculated using the proposed model and that of standard formulae for the dopant concentration that varies from 10^{13} to 10^{20} /cm³

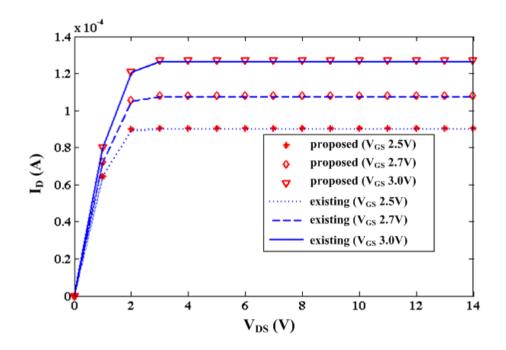


Figure 3.3. Comparison of the current voltage characteristics of the proposed model and that of existing model (standard formulae) for dopant concentration of 10¹³/cm³ at different gate to source voltage

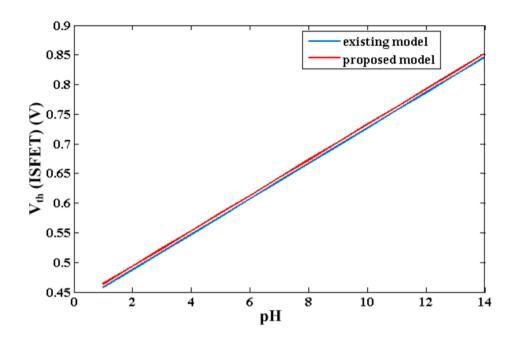


Figure 3.4. Variation of threshold voltage of ISFET device with pH values of electrolyte considering the threshold voltage of MOSFET for dopant concentration of 10^{13} /cm³

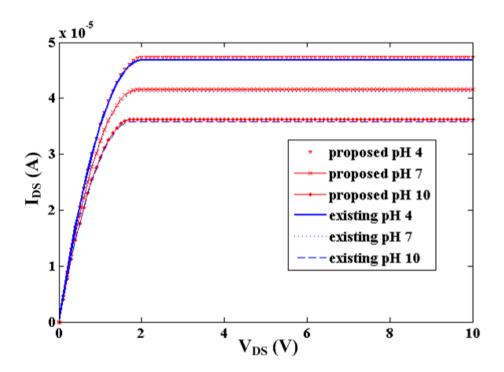


Figure 3.5. The current voltage characteristics of the ISFET device considering both the MOSFET models (proposed and existing) for three pH values of 4, 7 and 10.

Bibliography

[1] Uyemura, J.P. CMOS logic circuit design. Springer Science & Business Media, 1999.

[2] Grattarola, M. and Giuseppe, M. *Bioelectronics Handbook*, McGraw Hill, 1998.

[3] Sze, S.M. *Semiconductor Devices Physics and Technology*, John Wiley and Sons(Asia) Pte. Ltd, 2002.

[4] Neamen, D.A. Semiconductor Physics and Devices, McGraw Hill, 2007.

[5] Karlsson, P.R. and Jeppson, K.O. An efficient method for determining threshold voltage, series resistance and effective geometry of MOS transistors. *IEEE Transaction of Semiconductor Manufacturing*, 9(2):215-222, 1996.

[6] McAndrew, C. C. and Layman, P.A. MOSFET effective channel length, threshold voltage, and series resistance determination by robust optimization. *IEEE Transactions on Electron Devices*, 39(10):2298-2311, 1992.

[7] Sasaki, M., Ito, H., and Horiuchi, T. A new method to determine effective channel length, series resistance and threshold voltage. In *Microelectronic Test Structures, ICMTS 1996. Proceedings*(IEEE), pages 139-144, Mar 25, 1996.

[8] Hardillier, S., Mourrain, C., Bouzid, M.J., and Ghibaudo, G. New method for the parameter extraction in Si MOSFETs after hot carrier injection. In *Microelectronic Test Structures, ICMTS 1997.* Proceedings, pages 63-66, Mar 17, 1997.

[9] Tsuno, M., Suga, M., Tanaka, M., Shibahara, K. Miura-Mattausch, M., and Hirose, M. Physically-based threshold voltage determination for MOSFET's of all gate lengths. *IEEE Transactions on Electron Devices*, 46(7):1429-1434, 1999.

[10] Zhou, X., Lim, K.Y., and Lim, D. A simple and unambiguous definition of threshold voltage and its implications in deep-submicron MOS device modeling. *IEEE Transactions on Electron Devices*, 46(4):807-809, 1999.

[11] Jean, Y.S. and Wu, C.Y. The threshold-voltage model of MOSFET devices with localized interface charge. *IEEE Transactions on Electron devices*, 44(3):441-447, 1997.

[12] Yan, Z. X. and Deen, M. J. Physically-based method for measuring the threshold voltage of MOSFETs. *IEE Proceedings G (Circuits, Devices and Systems)*, 138(3): 351-357, Jun 1991.

[13] Lau, M. M., Chiang, C.Y., Yeow, Y.T., and Yao, Z.Q. Measurement of V_t and L_{eff} using MOSFET gate-substrate capacitance. In *Microelectronic Test Structures, ICMTS 1999 Proceedings*, pages 152-155, 1999.

[14] Lau, M.M., Chiang, C.Y., Yeow, Y.T., and Yao, Z.Q. A new method of threshold voltage extraction via MOSFET gate-to-substrate capacitance measurement. *IEEE Transactions on Electron Devices*, 48(8):1742-1744, 2001.

[15] Akers, L.A. The effect of field dependent mobility on the threshold voltage of a small geometry MOSFET. *Solid-State Electronics*, 23(2):173-175, 1980.

[16] Mirabella, S., De Salvador, D., Napolitani, E., Bruno, E., and Priolo, F. Mechanisms of boron diffusion in silicon and germanium. *Journal of Applied Physics*, 113(3):1-21, 2013.