Exploring the Reliability of LDMOS and Junctionless FETs in Harsh Environments: High-Temperature and High-Radiation Applications

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by

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5.1 Summary of Contributions

LDMOS transistors address limitations of conventional MOSFETs in high-power applications, offering high power density, breakdown voltage, and efficiency. They feature a structurally different design with a laterally diffused channel, thicker drift region, and buried drain contact. LDMOS devices are widely explored for high-power RF applications like cellular base stations and radar systems, but face challenges such as HCD and radiation effects.

Junctionless transistors provide better control over carrier concentration, lower leakage currents, and have increased scalability. Their ultra-low subthreshold swing and simplified fabrication procedure make them promising for low-power and energy-efficient electronic systems. This thesis explores the most recent developments in nano-electronic devices, with a special emphasis on DG-SiCJLT. The novel P^{+}-SiCJLT transistor topologies provide notable gains in scalability, energy economy, and performance while addressing important semiconductor technology issues. In addition to that, by combining the JLT and TFET, a new device JL-TFET, particularly aimed at low-power and high-temperature scenarios, offer enhanced gate control, resulting in improved performance parameters such as speed and power efficiency. They exhibit reduced leakage current, addressing a significant challenge associated with conventional FETs, particularly as feature sizes decrease.

For real life application knowing reliability of these devices is important. Therefore, this study investigates the reliability of LDMOS and JLTs in high temperature and in high-radiation conditions through a comprehensive approach by using TCAD simulation tools and modeling methodologies. The goal of the study is to identify the benefits, drawbacks, and opportunities for improvement in these semiconductor devices by examining device architecture, low-frequency noise performance, reliability problems, and environmental stressors.

A through simulation study on this work reveals the significant impact of TID on the analog performance of LDMOS devices. EHP generation with TID leads to V_{TH} shifts and degradation in I_{ON}/I_{OFF}. I_{output} increases, reducing R_0, while G_M and f_T show nonlinear responses. Sensitivity of $1/f$ noise to TID highlights the need for effective mitigation strategies. Proposed methods for modulating V_{TH} under TID offer avenues for improving device performance and reliability.

The proposed P^+-SiCJLT design offers enhancement mode operation and exceptional electrostatic characteristics, making it highly promising for high-power electronics. The device's tunability of V_{TH} through various parameters enhances scalability and versatility. Comparative analysis demonstrates superior performance in terms of I_{ON}/I_{OFF} and gain, positioning P^+-SiCJLT as a viable option for lower power and higher voltage applications. Furthermore, its retention of excellent characteristics at high temperatures underscores its suitability for power electronics.

The investigation into JL-TFET performance under various conditions reveals its resilience to HCI due to its junctionless nature. The minimal change in gate current I_G with temperature suggests reduced trap formation, contributing to improved device stability. However, radiation-induced effects, including increased gate leakage current and reduced channel control, lead to V_{TH} degradation, highlighting the complexity of device behavior under TID. Additionally, trapping-induced BTI further underscores the intricate interplay between HCI, radiation, and NBTI affecting JL-TFET characteristics. Temperature-dependent analyses demonstrate JL-TFET's favorable performance in terms of I_{ON} and I_{ON}/I_{OFF} up to T=400K, making it suitable for low-power applications such as memory devices. The device's simplicity in fabrication and cost-effectiveness further enhances its attractiveness for practical implementation. Conversely, p-i-n SOI-TFETs exhibit superior f_T and *GBW*, making them better suited for high-speed analog applications. The investigation into interface traps reveals their significant impact on device performance, with donor-like traps predominantly affecting the ambipolar state region and acceptor-like traps influencing transfer characteristics in the ON-state region. Overall, the study provides valuable insights into the performance and suitability of JL-TFET and p-i-n SOI-TFET devices under various operating conditions, guiding their application in diverse electronic systems.

Furthermore, this research aims to offer significant insights for electronics design and implementation in mission-critical industries like aerospace, automotive, and space exploration, in addition to furthering our understanding of semiconductor device dependability. This initiative aims to spur innovation and improve the dependability of electronic systems in critical applications by expanding our understanding of transistor technologies and their performance under demanding circumstances.

5.2 A Few Directions for Future Works

Subsequent investigations into sophisticated transistor technologies for difficult environments have the capacity to stimulate creativity, enhance the dependability of electronic systems, and facilitate revolutionary progress in several sectors.

- In order to obtain optimal performance in hostile conditions, future research can investigate hybrid transistor architectures that combine the advantages of many transistor types, such as JL-FETs, FinFETs, and nanowire FETs. Researchers can take advantage of each transistor technology's distinct properties to improve the overall performance and dependability of their devices by combining them.
- As operating at high temperatures puts transistor reliability at risk, research in the future can concentrate on creating novel thermal management strategies to efficiently disperse heat and keep devices operating in challenging conditions. Investigating cutting-edge heat sink designs, phase-change materials, or active cooling systems specifically designed for semiconductor devices may be part of this.
- The advent of quantum computing presents an opportunity to utilize cutting-edge transistor technology in quantum computing systems intended for challenging settings. Subsequent studies may examine the incorporation of resilient transistors in quantum computing frameworks designed for industries such as aerospace, automotive, and other crucial sectors.
- Future studies may examine how machine learning and AI might be combined to improve transistor performance, reliability, and design in challenging conditions. To improve transistor performance and longevity, AI algorithms can help with problem detection, adaptive control, and predictive modeling.
- It may be possible to create transistors with greater performance and dependability in harsh circumstances by looking into novel materials other than silicon, such as wide-bandgap semiconductors like silicon carbide and gallium nitride, and 2D materials like graphene and transition metal dichalcogenides. Subsequent investigations may concentrate on comprehending the characteristics and actions of these substances and using them for applications in tough environments.

- The development of adaptive transistor technologies, which can self-adjust their properties and performance in response to changing environmental conditions may be the subject of future research. Investigating self-healing materials, adaptive control circuits, or reconfigurable transistor designs made to survive severe environments' fluctuating stresses are a few possible approaches to this.

Further research should focus on designing and fabricating transistors according to particular application needs in challenging conditions. For specific applications, including deep-sea exploration, space exploration, or industrial automation under harsh conditions, researchers can improve device performance and reliability by tuning transistor parameters like gate oxide thickness, doping profiles, and channel diameters.

Publications Based on This Work

Journal [Published]:

1. **Routh, S**., Deb, D., Baruah, R.K. and Goswami, R. Impact of High-temperature and Interface Traps on Performance of a Junctionless Tunnel FET. **Silicon**. 15, 2703–2714, 2022. https://doi.org/10.1007/s12633-022-02191-8
2. Baruah, R.K., Mahajan, B.K. and **Routh, S.** A Scalable Enhancement-Mode Junctionless SiC FET with Embedded P^+ Pockets in the Oxide Layer for High-Temperature Applications. **J. Electron. Mater.** 52, 1507–1517, 2022. https://doi.org/10.1007/s11664-022-10057-3
3. **Routh, S. and** Baruah, R.K. A comprehensive analysis of LDMOS transistors for analog applications under γ-radiation. **Microelectronics Reliability**. 148, 115159, 2023. https://doi.org/10.1016/j.microrel.2023.115159

Journal [Under Review]:

1. **Routh, S.,** Deb, D. and Baruah, R.K. Exploring the Reliability of Junctionless Tunnel-FETs: Impact of HCI, TID, and NBTI Challenges. **Microsystem Technologies**, 2024.
2. **Routh, S.,** Daimari, A. and Baruah, R.K. Exploring the Impact of Radiation and Temperature on LDMOS: An Analysis for Analog Circuit Perspective. **Microelectronic Reliability**, 2024.

Conference:

1. **Routh, S.,** Deb, D., Baruah, R.K. and Goswami, R. Junctionless Tunnel FET for High-Temperature Applications from an Analog Design Perspective. In: 2022 IEEE International Conference on Nanoelectronics, Nanophotonics, Nanomaterials, Nanobioscience & Nanotechnology (**5NANO**). pp. 1–4. IEEE, Kottayam, India, 2022. doi:10.1109/5nano53044.2022.9828986
2. Khatoniar, S., **Routh, S.,** Malakar, D. and Baruah, R.K. Modelling of surface potential and threshold voltage for short channel junctionless cylindrical gate-all-around MOSFET" in IEEE International Conference of Electron Devices Society Kolkata Chapter (**EDKCON**), pp. 495-499, Kolkata, India, 2022. doi:10.1109/edkcon56221.2022.10032880