Declaration

I, **Sujay Routh**, hereby declare that the present thesis, entitled **"Exploring the Reliability of LDMOS and Junctionless FETs in Harsh Environments: High-Temperature and High-Radiation Applications"**, is the record of work done by me under the supervision of Dr. Ratul Kumar Baruah, Associate Professor, Department of Electronics and Communication Engineering, Tezpur University, Tezpur. The contents of the thesis represent my original works that have not been previously submitted for any Degree/Diploma/Certificate in any other University or Institutions of Higher Education.

This thesis is being submitted to Tezpur University for the Degree of Doctor of Philosophy in Electronics and Communication Engineering.

Place: Tezpur University, Tezpur

Date: (Sujay Routh)

TEZPURUNIVERSITY

(A Central University Established by an Act of Parliament)
Napaam, Tezpur-784028, Sonitpur, Assam, India

Certificate

This is to certify that the thesis entitled, "**Exploring the Reliability of LDMOS and Junctionless FETs in Harsh Environments: High-Temperature and High-Radiation Applications**", submitted to the School of Engineering, Tezpur University in partial fulfillment for the award of the degree of Doctor of Philosophy in Electronics and Communication Engineering is a record of research work carried out by **Mr. Sujay Routh** under my supervision and guidance.

All help received by him from various sources have been duly acknowledged.

No part of this thesis has been submitted elsewhere for award of any other degree.

16/10/2024

(*Supervisor*)

Dr. Ratul Kumar Baruah
Associate Professor
Department of ECE
School of Engineering, Tezpur University

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Certificate of the External Examiner

This is to certify that the thesis entitled **"Exploring the Reliability of LDMOS and Junctionless FETs in Harsh Environments: High-Temperature and High-Radiation Applications"** submitted by **Mr. Sujay Routh,** Department of Electronics & Communication Engineering, School of Engineering, Tezpur University in partial fulfilment for the award of the degree of Doctor of Philosophy in Electronics & Communication Engineering has been examined by us on_____ and found to be satisfactory.

The committee recommends for the award of the degree of Doctor of Philosophy.

Supervisor **External Examiner**

(Dr. Ratul Kumar Baruah) **( )**

Date:_____ **Date:_____**

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Sujay Routh

Dedicated to my

Parents.....

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Nomenclature

Symbols:

V_{TH}	Threshold Voltage
G_M	Transconductance
f_T	cut-off frequency
R_0	Output Resistance
R_{dose}	Radiation Dose
V_{DS}	Drain to Source Voltage
V_{GS}	Gate to Source Voltage
I_{DS}	Drain Current
N_{it}	Interface Trap Charges
N_{ot}	Bulk Trap Charges
V_{BD}	Breakdown Voltage
$R_{ON,sp}$	Specific ON-Resistance
q	Charge of an Electron
τ	Carrier Lifetime
ρ	Space Charge Density
m	Mass of an Electron
T	Temperature
φ_S	Surface Potential
I_{ON}	ON-State Current
I_{OFF}	OFF-State Leakage Current

I_{output}	Output Current
g_0	Number of EHP Generated Per Unit Dose
C_{GD}	Gate-to-Drain Capacitance
C_{GS}	Gate-to-Source Capacitance
C_{GG}	Total Gate Capacitance
D_{it}	density of interface traps density
D	Absorbed Radiation Dose
$\emptyset_f$	Bulk Potential
$\emptyset_{ms}$	Metal Workfunction
Q_{ox}	Oxide Charge Density
C_{ox}	Oxide Capacitance
V_{T0}	Threshold Voltage at Ambient Temperature
ϕ_{M1}	Metal 1 Work Function
ϕ_{M2}	Metal 2 Work Function
E_g	Band Gap
T_{OX}	Oxide Thickness
L_G	Gate Length
L_{CG}	Length of Control Gate
L_{ch}	Length of the Channel Region
L_{drift}	Length of Drift Region
Γ	Transmission Coefficient
g_v	the valley degeneracy factor

P_{ins}	The Probability of Electrons Moving Without Scattering
m_{ins}	The Effective Mass of The Insulator
v	The Magnitude of Electron Velocity
ΔV_{TH}	Threshold Voltage Shift
ΔL	Change in Length
σ_n	Capture Cross-Section of Electron
σ_p	Capture Cross-Section of Hole
v_{th}^{n}	Thermal Velocity of Electron
v_{th}^{p}	Thermal Velocity of Hole

Abbreviation:

D	Total Absorbed Dose
E	Electric Field
SS	Sub Threshold Slope
CG	Control Gate
FG	Fixed Gate
CB	Conduction Band
VB	Valance Band
NW	Nanowire
FD	Fully Depleted
RF	Radio Frequency
SH	Self-Heating
WF	Work Function
LS	Spacer Length

JLT	Junctionless Transistor
FET	Field-Effect Transistor
WBG	Wide Bandgap
TAT	Trap-Assisted Tunneling
SRH	Shockley-Read-Hall Recombination
RTN	Random Telegraph Noise
GBW	Gain Bandwidth Product
EHP	Electron Hole Pair
BTBT	Band-to-Band Tunneling
HTFET	Heterojunction Tunnel FET
MOSFET	Metal-Oxide-Semiconductor FET
JL-TFET	Junctionless Tunnel Field Effect Transistor
MugFETs	Multi-Gate FETs
ULSI	Ultra-Large-Scale Integration
DG-JLT	Double-Gate Junctionless Field-Effect Transistor
DG-SiCJLT	Dual-Gate Silicon Carbide Junctionless Transistor
SOA	Safe Operating Area
DTCO	Design Technology Co-Optimization
ZTC	Zero Temperature Coefficient
GAA	Gate All Around
ITRS	International Technology Roadmap for Semiconductors
HPC	High-Performance Computing
IoT	Internet of Things
SiO_2	Silicon Dioxide
HfO_2	Hafnium Dioxide

SiC	Silicon carbide
GaN	Gallium Nitride
TPU	Tensor Processing Units
VHF	Very High Frequency
UHF	Ultra-High Frequency
RESURF	Reduced Surface Field
DeMOS	Drain-extended MOS Transistor
TCAD	Technology Computer-Aided Design
BTI	Bias Temperature Instability
TDDB	Time-Dependent Dielectric Breakdown
NBTI	Negative Bias Temperature Instability
CMOS	Complementary Metal Oxide Semiconductor
EOT	Effective Oxide Thickness
GIDL	Gate-Induced Drain Leakage