Abstract

The field-effect transistor (FET) has become a key technology that has shaped electronic applications in a wide range of industries. These transistors are the building blocks of semiconductor devices used nowadays and play a crucial role in modern electronics allowing for fast digital logic and effective signal processing. Power electronics applications increase the efficiency of voltage regulators, power inverters, and switch-mode power supplies by utilizing low ON-state resistance and quick switching capabilities. In the field of wireless communication, transistors are essential components of RF amplifiers and mixers, which are essential to the smooth operations of gadgets such as communication satellites and smartphones. FET's adaptability also extends to analog circuits, where they help achieve the precision needed for uses like sensor interfaces and audio amplification.

The need for strong and durable components has increased as electronic systems are incorporated into more complicated and challenging environments, making the study of device reliability essential. Laterally-diffused-metal-oxide-semiconductor (LDMOS) and junctionless transistors (JLT) have certain qualities that make them especially appealing for use in harsh environments. LDMOS transistors are at the forefront of advancements in RF electronics, pushing gains in performance, efficiency, and downsizing as semiconductor technologies continue to provide strong prospects for improving electronic systems in challenging environments. A revolutionary development in transistor technology, the JLT offers increased control over carrier concentration, lower leakage currents, improved scalability, comparatively cost effective and and easier fabrication process. This study examines two types of JLT transistors, namely: the junctionless tunnel field-effect transistor (JL-TFET) and the double gate silicon carbide junctionless transistor (DG-SiCJLT). The JL-TFET achieves ultra-low subthreshold swing by making use of quantum tunneling events, which allows ultra-low power operation. Utilizing silicon carbide's high band gap property, the DG-SiCJLT improves electron mobility and device reliability. This transistor design achieves better control over the channel region through the use of a double-gate structure, which leads to better I_{ON}/I_{OFF} and lower leakage currents. The transistor's thermal stability is further improved by the integration of silicon carbide, which makes it a viable option for high-temperature and high-power applications.

This study investigates the analog performance of LDMOS and JLTs under the influence of total ionizing dose (TID), temperature variations, and process-induced reliability concerns. Through extensive simulation studies and calibration with fabricated devices using the Sentaurus TCAD and analytical tools, we analyze key parameters such as V_{TH}, G_M R_0, f_T, and $1/f$ noise behavior. It is observed that TID-induced electron-hole pair generation causes V_{TH} to decrease and impacts I_{ON}/I_{OFF} ratios in LDMOS, while DG-SiCJLT exhibit sensitivity to oxide thickness and substrate dimensions. Strategies to modulate V_{TH} in LDMOS include channel doping, length modulation, oxide thickness variation, and pocket-doped methodologies, all of which are discussed in detail.

Additionally, we propose a novel design of P^+-SiCJLT with enhanced electrostatics and scalability for high-power electronics, memory, and IoT applications. Our findings underscore the importance of mitigating radiation and temperature effects in this advanced electronic devices to ensure reliability and efficiency, especially in mission-critical environments such as aircraft systems and satellite communication.

Furthermore, the impact of hot carrier injection (HCI), TID, negative bias temperature instability (NBTI), and process-induced reliability on JL-TFET performance is explored. It is observed that JL-TFETs exhibit less degradation with HCI due to their junctionless nature, while radiation-induced traps in the gate dielectric significantly affect V_{TH} and transistor behavior. Through comprehensive numerical analyses, we aimed to clarify the intricate interplay between HCI, radiation, and NBTI, providing insights into JL-TFET reliability under high temperature and high radiation conditions.

This study offers valuable guidelines for optimizing the performance, reliability, and efficiency of high-power analog circuits, paving the way for the practical application of LDMOS and JLT in diverse fields ranging from automotive to medical electronics.

Keywords: *FET; JLT; JL-TFET; DG-SiCJLT; P^+-SiCJLT, LDMOS; high-temperature; low-power; 1/f noise; TID; HC; NBTI.*