CHAPTER 1
Introduction

Contents

1.1 Field Effect Transistors

1.2 Transistor Scaling

1.3 Short Channel Effects (SCEs)

1.4 Advanced Semiconductor Devices

1.5 TCAD Simulation Methodology

1.6 Reliability of Semiconductor Devices

1.7 Radiation Effect on Semiconductor Devices

1.8 Research objectives

1.9 Thesis Organization

Bibliography

1.1 Field Effect Transistors

The current technology revolution, often labeled as Industry 5.0, is demonstrated by combining the ‘Internet of Things’ with the integration of sensors in cars, smart homes, and industry boosting productively [1, 2]. Innovations in power distribution, robotics, electronics, cybersecurity, and communication are largely responsible for this shift. Transistors are essential to this revolution because they make it possible to provide, manage, and consume electrical energy efficiently. This highlights the importance of transistor reliability for the advancement of technology in future electronics (Fig. 1.1) [3].

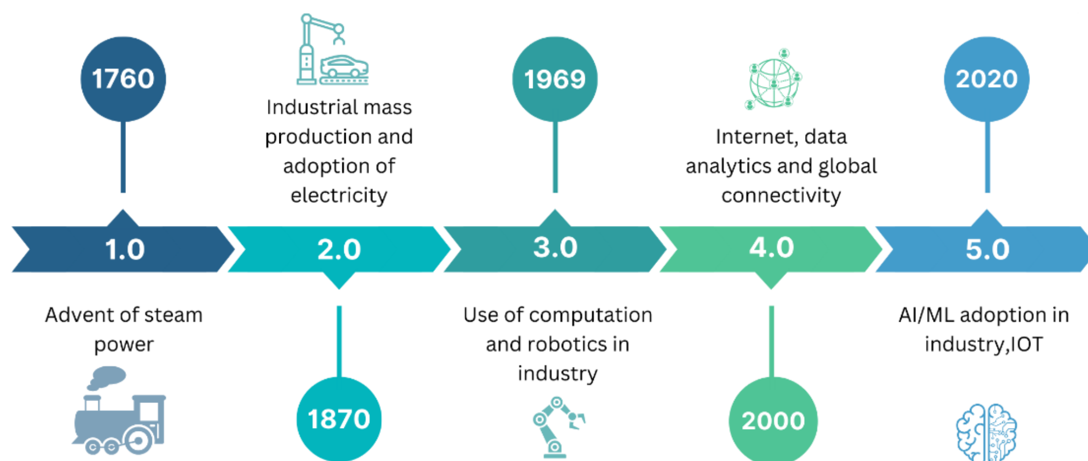


Fig. 1.1: Revolution to industry 5.0 [2].

Field Effect Transistors (FETs) are key component of this sophisticated semiconductor technology. Integrated Circuits (ICs) are designed with FETs, most especially Metal-Oxide-Semiconductor FETs (MOSFETs) [4]. Electronic devices operate better and are more efficient because of MOSFETs' special qualities, which include their great switching features, low power consumption, effective amplification, and regulation of electrical impulses [5–7]. MOSFETs are made up of a finely tuned metal gate that is isolated from the semiconductor material by a thin silicon dioxide-based insulating layer. The precise regulation of the current flow between the source and drain terminals is made possible by this design of forming a parallel plate capacitor between gate electrode and semiconductor substrate [8]. The voltage applied to the gate terminal creates an electric field that modifies the semiconductor channel's conductive characteristics. MOSFETs are essential for digital circuits as well, because of their quick ON-OFF (I_{ON}/I_{OFF}) switching speed, which increases data processing speed and

efficiency. Furthermore, these devices' adaptability in a variety of electronic applications is further enhanced by the differentiation between N-channel and P-channel MOSFETs based on the kind of predominant charge carriers in the channel i.e. n-type and p-type charge carrier respectively [9–11]. The improvement and optimization of FET designs support the never-ending quest for greater performance, reduced power consumption, and shrinking in electronic devices as semiconductor technology develops [7]. The continuous development of FETs highlights their pivotal function in molding the field of modern semiconductor technology and its influence on several sectors, ranging from computing to telecommunications and beyond [10].

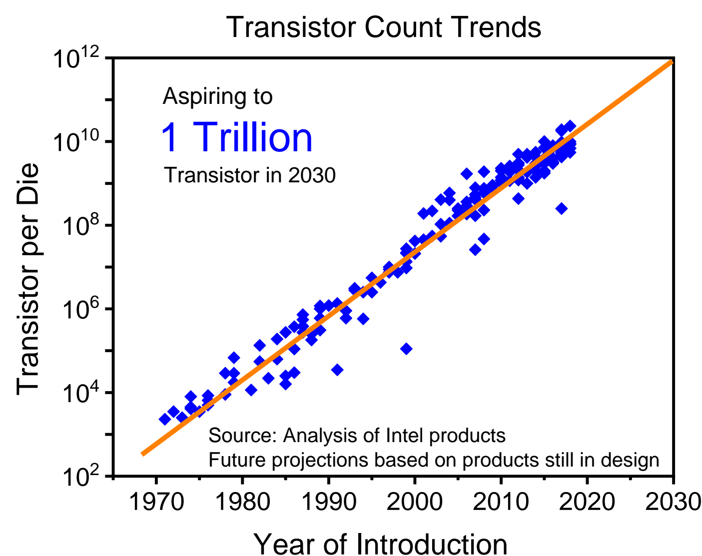


Fig. 1.2: Transistor counts doubling every two years against introduction dates according to Moore's Law.

IC technology has been continuously advanced by Moore's Law, a fundamental principle of the semiconductor industry shown in Fig. 1.2. According to this theory, transistor density doubles roughly in every two years, resulting in an exponential development in processing power [12]. Currently, the International Roadmap for Devices and Systems (IRDS) [13] and the International Technology Roadmap for Semiconductors (ITRS) [14] have established formal rules for industry cooperation that are in keeping with the objectives of Moore's Law [13]. It is becoming more and more clear that Metal-Oxide-Semiconductor (MOS) devices have limits, such as issues with heat dissipation, power consumption, and electron leakage. As technology is shrinking, unique strategies including alternate transistor topologies, new materials, and quantum computing breakthroughs are being looked for maintain semiconductor technology development beyond the traditional bounds of Moore's Law [15, 16].

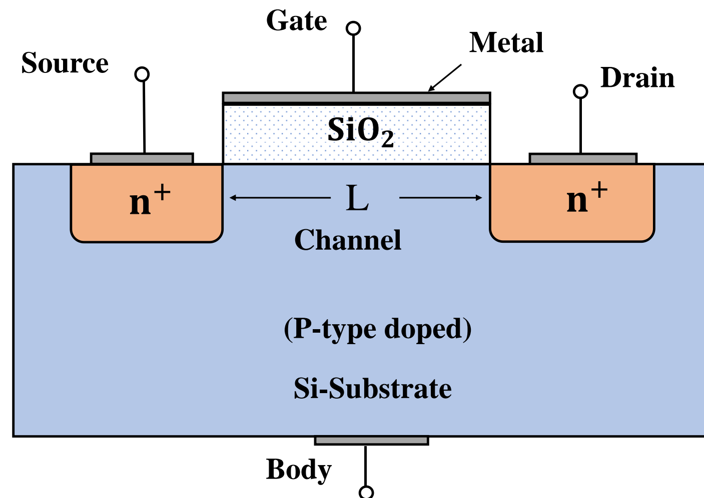


Fig. 1.3: Block diagram of an n-channel MOSFET.

The MOSFET is being continuously improved to increase packing density and computational effectiveness. The block diagram of an n-channel MOSFET shown in Fig. 1.3. Researchers and engineers have investigated many FET topologies, each intended to maximize performance in terms of size, power consumption, and speed, in order to fulfill the demands of high-density packing, higher processing speed and more memory space. Emerging technologies like FinFETs and Nanowire FETs, which go beyond conventional MOSFETs, have drawn attention due to their capacity to significantly increase transistor density and lower power consumption [17–19]. Because of its three-dimensional fin-like architecture, FinFETs offer superior control over current flow, allowing for higher packing densities and faster speeds. Furthermore, it has been shown that Tunneling FETs (TFETs) are a potential option for high-density applications. Compared to traditional FETs, TFETs can operate with low power consumption because they use quantum tunneling to transfer electrons [20, 21]. Need of high-speed computing has led to the investigation of ultra-thin bodies, buried oxide FETs and multigate transistors. By reducing the size of the transistor body, these designs aim to provide quicker switching times and faster electron mobility [17, 20].

1.2 Transistor Scaling

A further important principle that must be followed for Moore's Law to continue to hold true is Dennard scaling. This theory, named after its founder, Robert Dennard, states that power density of transistors must not decrease with transistor size, requiring proportionate decreases in voltage and current in addition to other dimensional scaling effects [22].

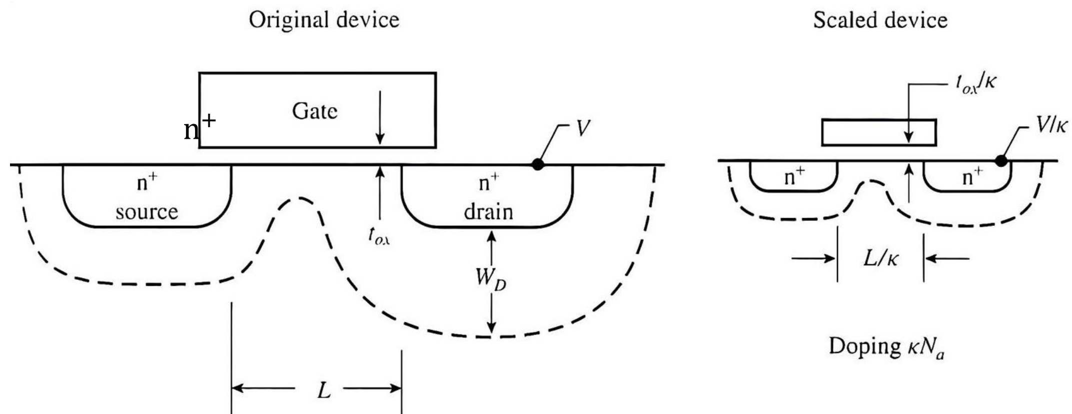


Fig. 1.4: Schematic representation of a Si MOSFET scaled by factor k [23].

Chip makers faithfully adhered to Dennard's scaling law far into the 1990s, making calculated changes to doping densities, voltages, and dielectric thicknesses that advanced the industry with each new generation of microprocessors. The development of memory modules, high-performance microprocessors, and other complex electronic systems depends on this scalability [24]. Quantum effects become more obvious as transistors get smaller in size (Fig. 1.4), which can calculate electron leakage and reduced switching with precision. At increased power densities, the problem of heat dissipation becomes more difficult, increasing the possibility of reliability problems and performance degradation [25]. The consistency of integrated circuits is impacted by differences in transistor performance brought about by manufacturing variability. Aggressive scaling is not always feasible due to rising economic costs related to sophisticated fabrication facilities. Moore's Law predicted a 20 to 30 percent annual decline in quality-adjusted manufacturing costs for electronic circuits due to shrinking transistor sizes every 2-3 years, leading to denser and cheaper chip fabrication over time [26, 27]. Signal delays and higher resistance are the outcomes of shrinking transistor sizes, which worsen problems with metal interconnects. It gets harder and harder to achieve steeper subthreshold slopes, which are essential for low-power applications [28]. Innovation is needed to overcome these obstacles, which is why the semiconductor industry is investigating new materials and structures.

1.3 Short Channel Effects (SCEs)

The reducing dimensions of MOSFETs to nano meter regime cause SCEs in MOSFET devices [4, 24, 29, 30]. The control of charge carriers gets more difficult as device lengths drop, which increases leakage currents and decreases gate control on the

channel. Comprehending these fundamental causes is essential to formulating tactics to tackle SCE and enhance MOSFET device performance in forthcoming semiconductor technologies [24]. Furthermore, when device dimensions get closer to sub-10nm scales, SCE become more pronounced, requiring creative design and fabrication methods to lessen their effects [4]. Further affecting device performance is the shortening of the channel length, which intensifies phenomena like:

1.3.1 Channel Length Modulation

In FETs where the length of the inverted channel region decreases as the drain bias increases, particularly notable at higher drain biases as shown in Fig. 1.5. This may cause the transistor's output resistance to drop, which would diminish its capacity to maintain a steady output voltage even with fluctuating drain currents [31]. The main source of this impact is the electric field that is created close to the MOSFET's drain area. This field extends into the channel and shortens the channel's useful length. Because of the decreased drain current caused by this reduction in effective channel length, the properties and performance of the device are affected [32].

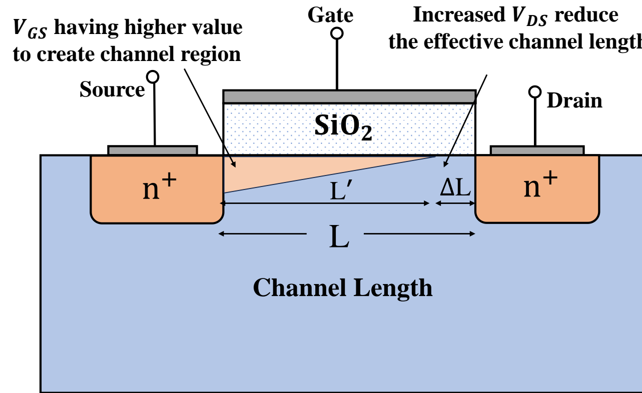


Fig. 1.5: Channel length modulation.

Reducing the length-to-width ratio lowers channel resistance, which increases current flow. At saturation, the drain current progressively rises as the drain-to-source voltage rises due to channel-length modulation. To accommodate this change , the saturation-region drain-current formula need to be modified by include the incremental channel length reduction expressed below [28]:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L-\Delta L}(V_{GS}-V_{TH})^2 \qquad (1.1)$$

If the incremental alteration is significantly smaller than the physical channel length,

the drain current in saturation can be expressed as:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2\left(1 + \frac{\Delta L}{L}\right) \quad (1.2)$$

The aforementioned expression assumes that the change in length (ΔL) is substantially smaller than the original length (L). However, this assumption becomes less valid as channel lengths decrease, particularly in modern short-channel devices for a nano-meter regime. Consequently, researchers have devised more accurate models for channel-length modulation to simulate these devices in modern contexts [33, 34].

1.3.2 Drain Induced Barrier Lowering (DIBL)

The effective barrier height between the source and drain is lowered as the channel length decreases because the drain voltage's influence spreads farther into the channel. DIBL changes V_{TH} with drain bias as the channel length decreases [28, 30]. This effect is first seen in the subthreshold region as a shift in the subthreshold current against gate bias curve. However, as the length of the curve increases, the slope decreases, suggesting that a larger gate bias adjustment is needed to achieve the same change in drain current. In very brief periods of time, it is conceivable for the gate to fail to entirely turn off the device; nevertheless, this cannot be solely attributed to a threshold change.
In practical terms, DIBL can be computed as follows [28]:

$$DIBL = -\frac{V_{TH}^{DD} - V_{TH}^{low}}{V_{DD} - V_{DD}^{low}} \quad (1.3)$$

In this calculation, DIBL is determined by subtracting the threshold voltage measured at a high drain voltage (V_{TH}^{DD}) from the threshold voltage measured at a very low drain voltage (V_{TH}^{low}), typically 0.05 V or 0.1 V. The difference is then divided by the supply voltage (V_{DD}) minus the low drain voltage (V_{DD}^{low}), which represents the linear part of the device's current-voltage characteristics. The negative sign in the formula ensures a positive DIBL value, given that the high drain threshold voltage is always smaller than the low drain threshold voltage. DIBL is typically expressed in units of mV/V.

1.3.3 Threshold Voltage Roll-off

The electric field between the channel region and the drain increases as the channel length (L_{ch}) decreases. The depletion zone close to the drain expands further

into the channel as a result of the higher electric field, shortening the effective channel length that is accessible for conduction. As a result, the V_{TH} drops since less V_{GS} is required to cause the same degree of channel inversion [35, 36].

An equation that takes into consideration the threshold voltage's dependence on L_{ch} can be used to mathematically explain the V_{TH} roll-off. The empirical expression is one model that is frequently used to explain this phenomenon [37]:

$$V_{TH} = 2\emptyset_F - \frac{Q_B}{C_{ox}} = 2\emptyset_F + \frac{qN_AW_T}{C_{ox}} \quad (1.4)$$

Where W_T is the total width of the device a function of L_{ch}, $\emptyset_F$ represent bulk potential, Q_B is fixed charge due to imperfection in silicon/oxide interface and C_{ox} represent oxide capacitance. From the equation it is clear that the V_{TH} of the device decrease with L_{ch}. Moreover, process variances like variations in oxide thickness or impurity concentrations during fabrication might result in V_{TH} roll-off. The variations affect the overall performance and dependability of the device by causing irregular transistor behavior throughout the integrated circuit.

1.3.4 Velocity Saturation

Saturation effects limit the rise in drain current with V_{GS} when carriers in the channel reach high velocities at high drain voltages. The efficiency and speed of the transistor may be impacted by this phenomenon [38]. The mobility of charge carriers also relies on the lateral electric field. As this field increases and approaches about 1 V/µm, carrier mobility starts declining. Consequently, the carrier velocity, represented by $v\ (=\ \mu E)$, reaches a saturation point at approximately $\sim 10^7$cm/s for sufficiently elevated fields along the channel. Here, $'\mu'$ denotes carrier mobility, and *'E'* signifies the low electric field [39].

As the electric field increases, the carrier velocity stops increasing because the carriers lose energy from interacting with the lattice. This interaction can include emitting phonons and photons when the carrier energy is large enough [40]. It affects the saturation current, transit time, and frequency response of these devices, ultimately imposing limits on their maximum achievable operating speed.

1.3.5 Hot Carrier Effects

High electric fields can cause carriers to gain excessive energy, which is why short channel devices are more vulnerable to hot carrier injection. The lifetime of the

device may be impacted by reliability problems including threshold voltage shift and increased leakage current [41, 42]. The degradation of MOSFET characteristics as a result of high-energy carriers' effects on the semiconductor material itself, including transconductance (G_M), threshold voltage (V_{TH}), and drain current (I_{DS}), is referred to as this effect. The silicon lattice may be harmed by hot carriers, which could lead to modifications in oxide characteristics, an increase in interface trap density, and changes in device characteristics. The longevity and dependability of MOSFETs can be greatly impacted by hot carrier degradation (HCD), which is a cumulative effect that is particularly noticeable in high-performance applications [43].

1.4 Advanced Semiconductor Devices

Modern semiconductor devices are essential for a wide range of applications, and each one needs a customized architecture to satisfy unique performance requirements such as better speed, power, space etc. as aforementioned. FinFETs are being used for high-performance computing (HPC) because of its three-dimensional fin-like structure, which increases speed and power efficiency [18]. The limitations of conventional MOSFETs are their susceptibility to overheating and insufficient ability to handle voltage and current. Power MOSFETs like LDMOS, DG-SiCJLT, get around these problems by offering higher voltage and current ratings, improved thermal performance, and lower ON-state resistance [44]. They are required for equipment that requires efficient power switching, such as power supplies, motor controls, and inverters. Their low ON-state resistance minimizes power losses, making them ideal for high-power applications [10, 45, 46]. Additionally, their fast-switching speeds enable efficient power flow management, which enhances overall system performance. Energy-efficient low-power architectures are essential to the internet of things (IoT), because they prolong the battery life of IoT sensors [9]. Memory devices have topologies designed to maximize storage density and minimize power consumption. Examples of these devices are Resistive RAM (RRAM) and 3D NAND flash memory. Silicon carbide (SiC) and gallium nitride (GaN) power devices are utilized by automotive electronics to provide increased efficiency and power density in driver-assistance systems and electric automobiles. Millimeter-wave semiconductor devices are needed for 5G communication networks to transmit data at high speeds. Tensor processing units (TPUs) and neuromorphic computing are two architectures that

artificial intelligence (AI) accelerators use to process neural networks efficiently. High-speed data transmission in data centers and telecommunications is made possible by architectures like silicon photonics, which are beneficial for optoelectronic applications [47]. High-efficiency III-V compound semiconductor solar cells are used in renewable energy technologies to harvest solar energy. High-resolution and sensitive imaging for medical diagnostics is made possible in the field of healthcare imaging by quantum dot imaging architectures and CMOS imaging sensors. TFETs use quantum tunneling to provide effective switching at low voltages, allowing for extremely low power consumption in applications like wearable technology and IOT sensors. While JLTs provide affordable options for integrated circuits and power management systems, with simplified fabrication procedures as there is no doping gradient present. Contrarily, both devices show promise in meeting the growing need for energy-efficient electronics [47–49].

1.4.1 Laterally Diffused Metal-Oxide-Semiconductor Device (LDMOS)

LDMOS transistors have dominated radio frequency (RF) power applications, especially in base stations, for more than two decades. Their superiority over conventional bipolar junction transistors (BJTs) and their persistent performance in terms of higher frequencies account for their prominence. Let's take a closer look at the elements that made LDMOS the clear winner among base station transmitters operating in the very high frequency (VHF) and ultra-high frequency (UHF) bands. The intrinsic nonlinearity of BJTs is one of its main drawbacks in high-power applications [45, 50, 51]. Due to the distortion that this nonlinearity adds to the amplified signal, communication systems may experience power loss and possible interference. Conversely, LDMOS transistors have better linearity, which enables less distortion in the signal and cleaner amplification. Improved signal quality and more effective power use are the results, both of which are essential for dependable base station operation. LDMOS transistors are not without limitation, despite their better performance as mentiones above. When compared to certain alternative technologies, such as GaN transistors, their on-resistance is typically larger which determines power losses during conduction. Nonetheless, ongoing R&D is concentrated on improving LDMOS designs to further minimize on-resistance while preserving other significant benefits [45].

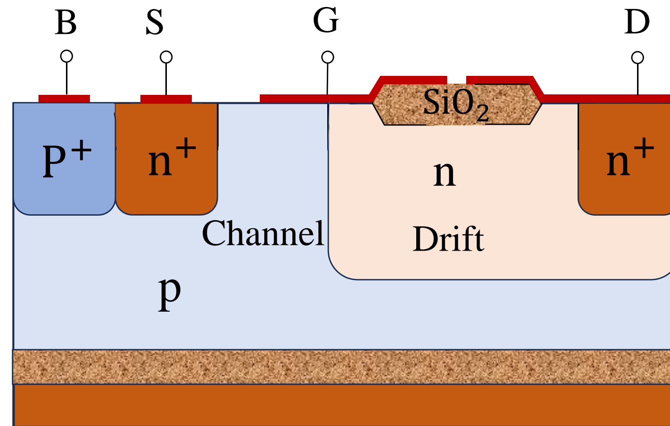


Fig. 1.6: Schematic of LDMOS.

The idea behind high-voltage MOSFETs such as LDMOS is to raise breakdown voltage by decreasing the surface electric field. This is accomplished by relaxing the distribution of space charges by extending the channel and increasing the drain diffusion area shown in Fig. 1.6. Breakdown voltage is raised without sacrificing current inversion by reducing drain diffusion doping and adding a lower doped drift zone. The reduced surface field (RESURF) effect extends the depletion layer for bulk breakdown, proposed in 1979 [52–54]. Nevertheless, instead of length and doping, increased on-resistance caused drift depth to increase. As a result, gate-to-drain overlap and shallow trench isolation were added to drain-extended MOS transistor (DeMOS) or LDMOS transistors for increased reliability [47, 55].

$$\frac{\partial^2 V}{\partial x^2} = -\frac{\partial E}{\partial x} = -\frac{q\rho}{\epsilon} \tag{1.5}$$

The link between charge (q), potential (V), electric field (E), and space charge density (ρ) is described by Poisson's equation (Eq. 1.5). To decrease the channel electric field, the channel length is first increased. Next, expanding the drain diffusion area contributes to the breakdown voltage increase by dispersing space charge. Reducing drain diffusion doping helps to relax space charge even more, albeit at the cost of current and inversion characteristics. In order to overcome this, the depletion layer is made to extend beyond the boundaries of a one-dimensional lateral diode by introducing a less doped "drift" zone between the channel and drain. This maximizes breakdown voltage while preserving current flow by facilitating bulk breakdown as opposed to junction breakdown.

1.4.2 Double Gate Silicon Carbide JLT (DG-SiCJLT)

Junctionless transistors (JLTs) using silicon carbide (SiC) as substrate material is a potential semiconductor technology since they perform better than traditional silicon-based devices in terms of power handling capabilities efficiency and superior performance in high-temperature environments [56]. By avoiding the need for extra transfer stages and growing SiC epitaxially directly on the substrate, the direct growth technique improves device scalability and lowers manufacturing costs. Additionally, this approach makes it easier to regulate the interface characteristics and material quality, which enhances device dependability and performance [57].

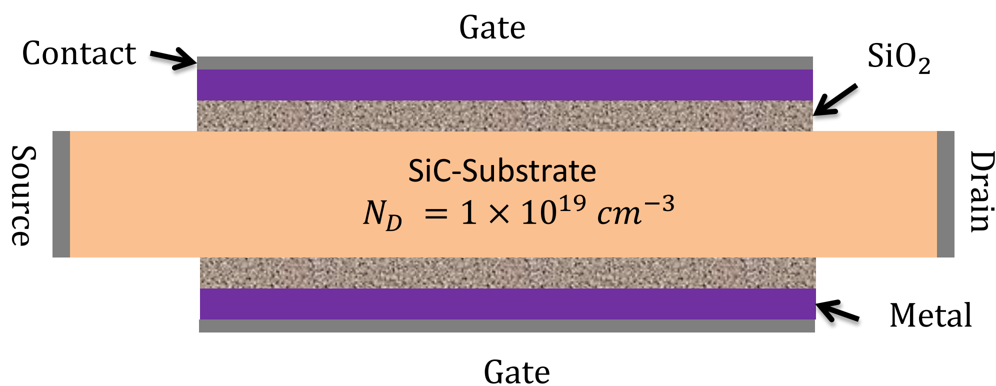


Fig. 1.7: Cross sectional view of a DG-SiCJLT.

Field-effect transistor theory governs how the DG-SiCJLT functions. By producing an electric field and adjusting conductivity in the SiC channel between the source and drain, the dual gate terminal regulates current flow as shown in Fig. 1.7. SiC can operate at high temperatures and voltages due to its wide bandgap, and fast switching speeds are made possible by its high electron mobility [56, 58]. Because of these characteristics, SiC FETs have lower switching losses than silicon-based counterparts, which makes them preferable for high-frequency and high-power applications. Critical factors for assessing SiC JLTs are performance metrics like transconductance, ON-state resistance, and threshold voltage. Recent developments have shown notable gains in these parameters, indicating that DG-SiCJLT have the potential to surpass current semiconductor technology [59]. In addition, one of the main factors influencing DG-SiCJLT adoption across a range of industries is their scalability. It is possible to create lightweight, compact electronic systems with improved performance thanks to the fabrication of smaller, more efficient devices.

1.4.3 Junctionless Tunnel Field Effect Transistor (JL-TFET)

Transistors, the backbone of contemporary electronics, are relentlessly shrinking, but their physical limits are being reached at nano meter regime. Novel transistor architectures are being investigated by researchers in their pursuit of ever-smaller and more efficient devices, the TFET is one such intriguing contender [60]. A TFET operates by leveraging quantum tunneling through a narrow barrier, allowing for low-power switching with reduced leakage current compared to conventional FETs (Fig. 1,8).

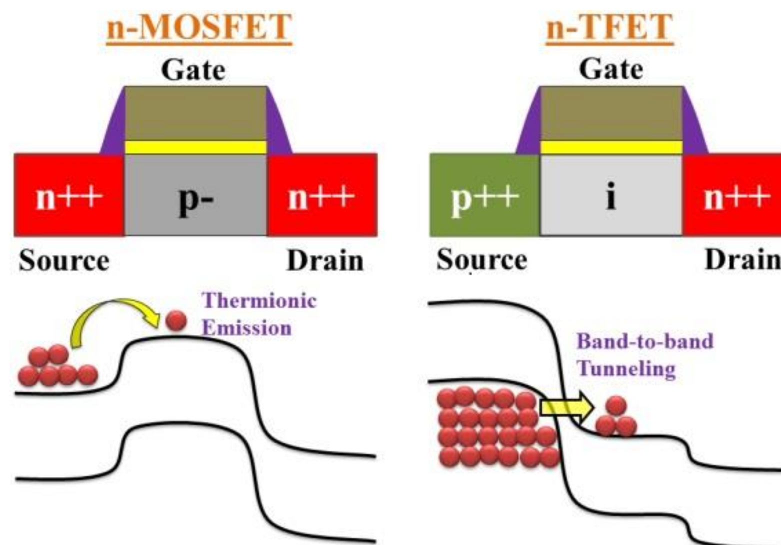


Fig 1.8: Comparison between conventional MOSFET and TFET [61].

Another promising device similar to the TFET is JL-TFET shown in Fig. 1.9(a), lack traditional PN junctions, relying on a thin silicon layer for quantum tunneling, enabling efficient electron transport and low power consumption, promising advancements in nanoscale electronics [48, 62]. Because of their distinctive design, JL-TFET have a lot of potential benefits such as less complicated, junctionless architecture offers the possibility of reduced power usage and simpler manufacture which makes them an interesting subject for future electronics research. They have steeper subthreshold swing and therefore has better scalability and lower leakage current. The band diagram in a JL-TFET illustrates the energy levels of electrons and holes, showing the tunneling process across the bandgap to enable low-power switching by leveraging quantum mechanics shown in Fig 1.9(b). Because of the JL-TFET's special structure, employ two gates to decouple the tunneling process from the transistor operation, namely fixed gate and control gate [62].

Fixed Gate: Unlike the control gate, the fixed gate maintains a constant voltage. This gate plays a supporting role, shaping the electric field within the channel and influencing how the control gate modulates the tunnel width. By adjusting the fixed gate voltage, researchers can fine-tune the JL-TFET's characteristics.

Control Gate: The control gate functions when a voltage is applied to it. Strong positive voltage enlarges the tunnel, making it easier for electrons to flow through (high current). In contrast, a negative voltage causes the tunnel to constrict, which makes it more difficult for electrons to pass through low current. Current flow is controlled by this tunnel width control.

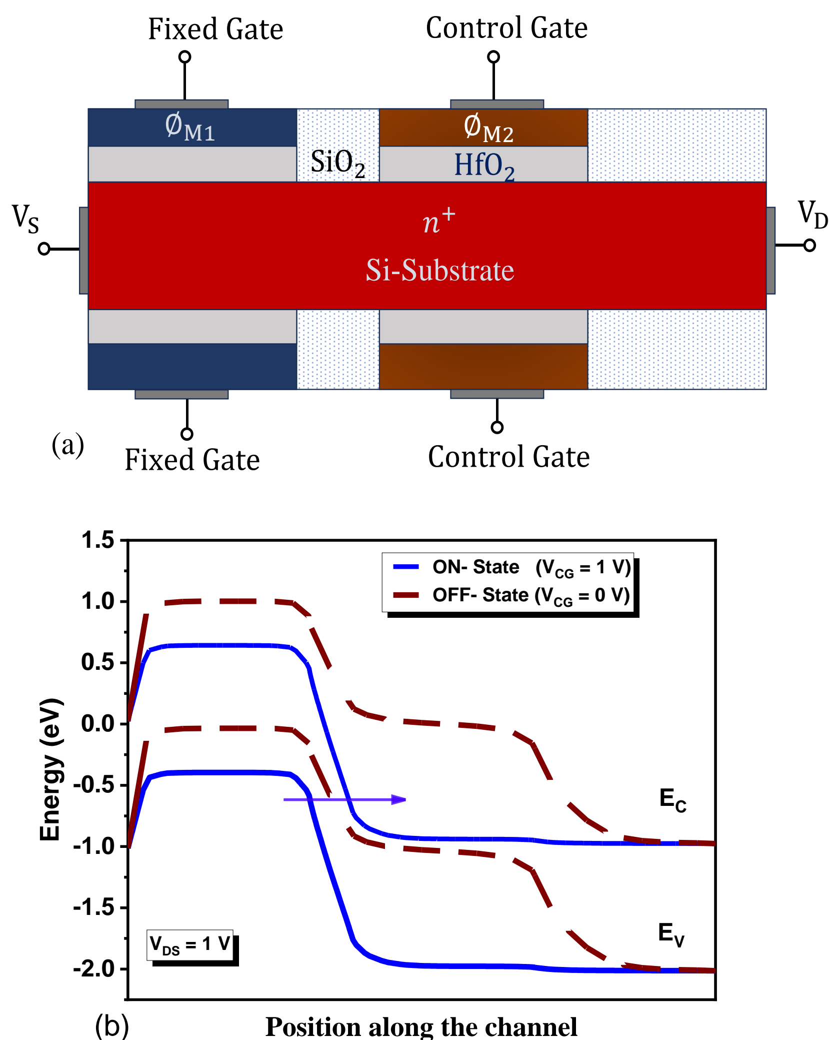


Fig 1.9: (a) Cross section view of n- channel JL-TFET (b) Band diagram of JL-TFET [62].

1.5 TCAD Simulation Methodology

Advanced simulation approaches are necessary to study the nano-electronic devices due to the ongoing push towards downsizing and increased performance. One essential technique for simulating and optimizing the behavior of these devices at the nanoscale is Technology Computer-Aided Design (TCAD). It makes easier to analyze performance data, electrical properties, and device behavior under varied operating circumstances. Nano-electronic device design, optimization, and analysis are made possible using TCAD simulation. TCAD helps engineers and researchers to investigate the complex behavior of devices at the nanoscale, spurring innovation and improvement in semiconductor technology [63]. It does this by utilizing computational modeling and

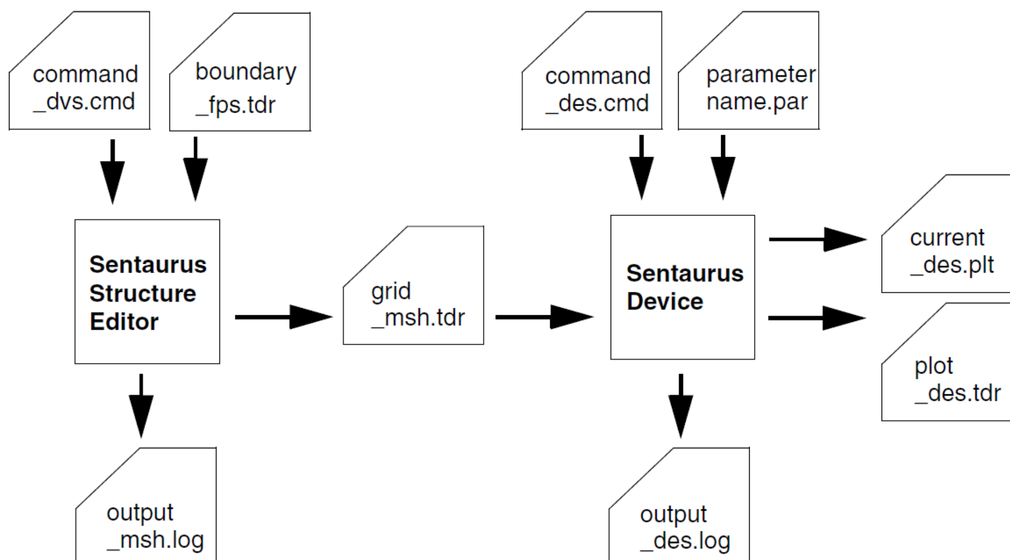


Fig. 1.10: Device simulation tool flow using Sentaurus TCAD [64].

numerical simulation approaches. In the era of nano-electronics, greater improvements in device performance, reliability, and manufacturability are promised by ongoing research and development in the TCAD methodology.

Device geometry definition, material property specification, mesh creation, physics modeling, and simulation output analysis are some of the phases that are included in TCAD shown in Fig. 1.10 explained below [64].

- Determining the device's geometric structure is the initial stage in the TCAD simulation process. This entails defining characteristics such electrode designs, doping profiles, layer thicknesses, and device dimensions. To accurately simulate the electrical activity of the device and capture its physical attributes, precise geometry

characterization is essential.

- TCAD needs specific material property data after the device geometry has been defined. This covers variables including bandgap energies, doping concentrations, dielectric constants, carrier mobility, and carrier lifespan. The performance of devices is greatly influenced by material properties, which necessitate precise modeling in order to produce trustworthy simulation results.
- Mesh generation involves dividing the device geometry into discrete elements or nodes to facilitate numerical analysis. Depending on the requirements of the simulation and the device construction, many meshing techniques are used, including adaptive, unstructured, and structured meshing. A fine mesh resolution is necessary to accurately record device activity in areas of high carrier concentration or rapid material property changes and to know the voltage and current at those nodes.
- The foundation of TCAD simulation is physics modeling, which involves the numerical solution of mathematical equations describing the physics of semiconductor devices. Models for carrier transport, electrostatics, thermal effects, quantum effects, and device-material interactions are included in this. Sophisticated algorithms and solvers are employed by TCAD tools to model the intricate physical phenomena that dictate the functioning of devices.
- TCAD uses a variety of simulation methods such as finite element analysis to examine various facets of device behavior. These comprise statistical variability analysis using Monte Carlo simulation, small-signal analysis for linear behavior, transient analysis for dynamic response, and DC analysis for steady-state characteristics. Every method provides information on particular device characteristics and performance indicators.
- To guarantee the quality and dependability of TCAD models, calibration and validation are essential. This entails validating the consistency and predictive power of the TCAD tool by contrasting simulation findings with experimental data or well-established analytical models. To increase simulation accuracy and fine-tune model parameters, iterative refinement might be necessary.
- Numerous nano-electronic devices, such as MOSFETs, FinFETs, nanowire transistors, memristors, photodetectors, and quantum devices, find extensive use in TCAD simulation. It gives device designers the flexibility to experiment with

various design configurations, maximize performance, forecast behavior under various operating scenarios, and evaluate yield and reliability before actual fabrication of the device.

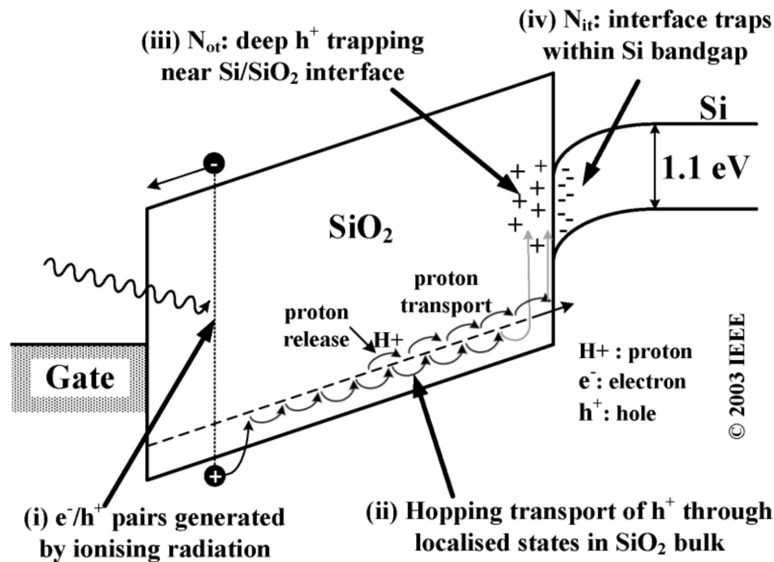
1.6 Reliability of Semiconductor Devices

Constant technological progress has led to the development of advanced semiconductor devices, which present a number of reliability issues due to their complex design and decreasing sizes. These include process differences, temperature effects, hot carrier injection (HCI), negative bias temperature instability (NBTI), gate oxide integrity, bias temperature instability (BTI), and time-dependent dielectric breakdown (TDDB) [55, 65, 66]. HCI, in which carriers acquire enough energy to be injected into a transistor's gate oxide, is one significant reliability risk. Over time, this process may cause the transistor's properties to gradually deteriorate, which could affect its functionality. NBTI, which predominantly affects PMOS transistors, is another problem. When a transistor is exposed to high temperatures and negative bias stress, its threshold voltage decreases, leading to NBTI [67]. The transistor's performance may be impacted by this deterioration, which may ultimately result in failure. Another issue that affects semiconductor device durability is radiation exposure, especially in high-radiation locations like space or close to nuclear reactors. Electron-hole pairs can form as a result of ionizing radiation, which can enhance leakage currents and cause charge accumulation in insulating layers. Elevated temperatures have the potential to hasten the processes that lead to semiconductor device deterioration. High temperatures encourage diffusion processes, which enhance dopant migration and cause structural faults in the device [55]. This may worsen problems like electromigration, NBTI, and HCI, which may ultimately affect the dependability of the device.

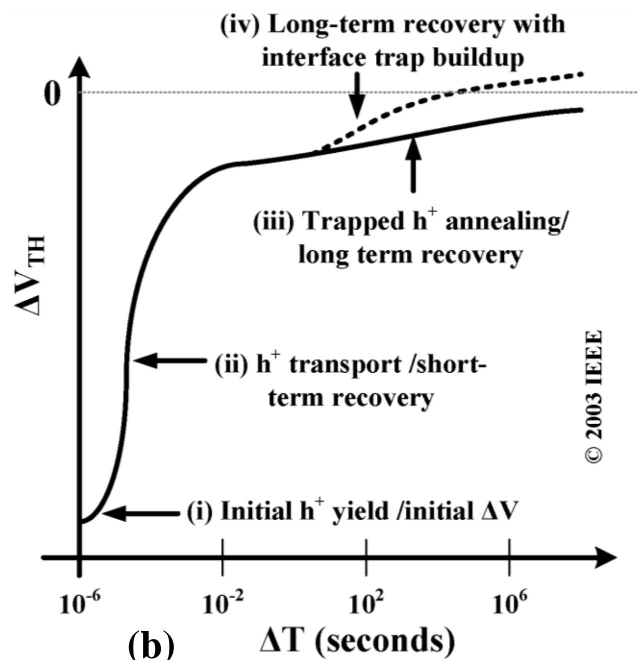
Because there is a considerable risk to the longevity and functionality of the device from each of these issues, a comprehensive strategy including material improvements, creative device architectures, advanced fabrication techniques, and exacting testing protocols is required. It is essential to address these reliability issues if advanced semiconductor technologies are to remain successful and reliable. In order to maintain the dependability requirements required by contemporary semiconductor applications, it is essential to identify and mitigate these difficulties through ongoing research and development initiatives.

1.7 Radiation Effect on Semiconductor Devices

Ionizing radiation doses that semiconductor devices accumulate over time are referred to as total ionizing dose (TID) effects. Electron-hole pairs can be produced by ionization processes involving ionizing radiation, such as gamma rays, X-rays, or energetic particles interacting with semiconductor material [68].



(a)



(b)

Fig. 1.11: (a) Energy band diagram of a MOSFET with positive gate bias represent how ionizing radiation affects carrier generation, transport, and trapping. (b) Changes in an n-channel MOSFET (nMOS) threshold voltage after radiation exposure [69, 71].

Its electrical characteristics may be impacted by the buildup of these produced charges inside the gadget. In semiconductors, the following are some important TID effects:

- **Threshold voltage shift:** Metal-oxide-semiconductor (MOS) transistors may experience a shift in their threshold voltage as a result of ionizing radiation. This change in control and performance of the transistor is caused by the creation of interface traps at the semiconductor-oxide interface [69, 70].

- **Increased leakage current:** Additional current channels may be created by radiation-induced traps in the oxide or bulk semiconductor, which would raise the leakage currents within the apparatus. This may result in a decrease in the semiconductor device's overall performance and dependability, particularly in low-power applications [70, 72].

- **MOS capacitor degradation:** Defects in the insulating oxide layer of MOS capacitors due to ionizing radiation can alter capacitance and interface states as shown in Fig. 1.11. Integrated circuit performance and stability are impacted by this degradation, especially for those circuits that depend on exact capacitor properties [73].
- **Change in electrical parameters:** Radiation exposure can affect a semiconductor device's mobility, carrier lifetimes, and dopant concentrations, among other electrical properties. Changes in these parameters can have an impact on the functionality and performance of the device, as well as its circuitry [74].
- **Long-term damage:** When semiconductor devices are used in radiation-intensive situations, TID effects can build up over time and cause long-term damage. Degradation may show up as changes in electrical characteristics, a greater vulnerability to radiation-related malfunctions, and a shorter lifespan for the equipment [75].

1.8 Research objectives

The proposed research work aims to explore the reliability of LDMOS and junctionless FETs in harsh environments for high-temperature and high-radiation applications which will be achieved by the following objectives,

- Investigate the LDMOS transistors, in terms of device performance, noise analysis, circuit performance, and high-temperature performance under radiation conditions.

- To design a scalable, enhancement mode double gate junctionless silicon carbide FET with embedded P^+ pockets in the oxide layer for high-temperature applications.
- Investigate the operational performance and reliability of JL-TFETs in harsh environments, especially under high-temperature and radiation conditions.

1.9 Thesis Organization

Chapter 1 gives a thorough explanation of the motivations behind the study, its particular objectives, and the constraints that it will work under. It also provides a well-organized overview of the thesis's structure, assisting the reader in navigating the ensuing chapters and parts.

Chapter 2 evaluate the performance of LDMOS transistors, analysis entails examining device characteristics such as breakdown voltage, on-resistance, and transconductance. Noise analysis techniques are used to comprehend and reduce noise sources like flicker noise or low frequency $(1/f)$ noise. In order to determine sensitivity to ionizing radiation effects and ensure the suitability for radiation-sensitive applications, radiation performance using calibration methodology with experimental dataset simulated under radiation circumstances. Metrics including gain, efficiency, linearity, and stability are assessed for evaluating circuit performance in circuit simulations through calibration with experiments.

Chapter 3 investigates the effects of oxide layer characteristics and P^+ pocket integration on the behavior and functionality of DG-SiCJLT in challenging environments. Furthermore, optimizing gate geometry and doping profiles for scalability in enhancement mode operation is carried out. To guarantee intended performance, simulation studies evaluate device properties such as transconductance, ON-OFF current ratio, and threshold voltage. Thermal simulations are used to assess the dependability and stability at high temperatures. Studies on process variability look into production tolerances and how they affect yield and device performance.

Chapter 4 examined the operational performance of JL-TFETs through simulations and calibration methodology with particular attention paid to important factors including

current-voltage characteristics and subthreshold swing at different temperatures. Accelerated aging tests and high-temperature cycling studies are used in reliability evaluations to analyze the stability of devices over time. Radiation testing evaluates the effect on the performance and dependability of the JL-TFET in radiation-prone situations, including exposure to ionizing radiation sources. Examining trap-assisted tunneling processes under challenging circumstances sheds light on possible dependability problems. To further comprehend the device's thermal stability, thermal simulations look into the temperature distribution inside it. Furthermore, examination of oxide layer characteristics and material compatibility guarantees the JL-TFET's dependability in harsh environmental circumstances.

Chapter 5 summarizes the thesis and assesses the research's contributions in conclusion. In addition, it suggests topics for more research and broadens the scope of the existing study by examining possible directions for future research.

Bibliography

[1] Adel, A. Future of industry 5.0 in society: human-centric solutions, challenges and prospective research areas. Journal of Cloud Computing. 11, 40, 2022. https://doi.org/10.1186/s13677-022-00314-5

[2] Leng, J., Sha, W., Wang, B., Zheng, P., Zhuang, C., Liu, Q., Wuest, T., Mourtzis, D. and Wang, L. Industry 5.0: Prospect and retrospect. Journal of Manufacturing Systems. 65, 279–295, 2022. https://doi.org/10.1016/j.jmsy.2022.09.017

[3] Nexus Admistra Integra: Industry 5.0: the new revolution, https://nexusintegra.io/industry-5-0-the-new-revolution/, 2020.

[4] Brews, J.R., Fichtner, W., Nicollian, E.H. and Sze, S.M. Generalized guide for MOSFET miniaturization. IEEE Electron Device Lett. 1, 2–4, 1980. https://doi.org/10.1109/EDL.1980.25205

[5] Enz, C.C., Krummenacher, F. and Vittoz, E.A. An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. Analog Integr Circ Sig Process. 8, 83–114, 1995. https://doi.org/10.1007/BF01239381

[6] Arora, N. and Wien, S.-V. MOSFET Models for VLSI Circuit Simulation: Theory and Practice. New York: Springer, 1993.

[7] Omura, Y., Mallik, A., Matsuo, N. MOS Devices for Low-Voltage and Low-Energy Applications. Singapore Wiley, 2016.

[8] Yang, P., and Chatterjee, P. K. SPICE Modeling for Small Geometry MOSFET Circuits. in IEEE Transactions on Computer-Aided Design of Integrated Circuits

and Systems, vol. 1, no. 4, pp. 169-182, October 1982, doi: 10.1109/TCAD.1982.1270008.

[9] Lorenz, L. and Mitlehner, H. Key power semiconductor device concepts for the next decade. Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344). 1, 564–569, 2002. https://doi.org/10.1109/IAS.2002.1044141

[10] Wang, H., Wang, F. and Zhang, J. Power Semiconductor Device Figure of Merit for High-Power-Density Converter Design Applications. IEEE Trans. Electron Devices. 55, 466–470, 2008. https://doi.org/10.1109/TED.2007.910573

[11] Yu Yuan, X., Oswald, N. and Mellor, P. Superjunction mosfets in voltage-source three-level converters: Experimental investigation of dynamic behavior and switching losses', IEEE Transactions on Power Electronics, 30(12), pp. 6495–6501, 2015. doi:10.1109/tpel.2015.2434877.

[12] Moore, G.E. Cramming More Components Onto Integrated Circuits. Proceedings of the IEEE. 86, 82–85, 1998. https://doi.org/10.1109/JPROC.1998.658762

[13] IEEE International roadmap for devices and systems (IRDS), https://irds.ieee.org/

[14] Hoefflinger, B. ITRS: The International Technology Roadmap for Semiconductors. Presented at the , Berlin, Heidelberg, 2011.

[15] Sesnic, S.S. and Craig, G.R. Thermal effects in JFET and MOSFET devices at cryogenic temperatures. IEEE Transactions on Electron Devices. 19, 933–942, 1972. https://doi.org/10.1109/T-ED.1972.17522

[16] Shin, S.H., Wahab, M.A., Ahn, W., Ziabari, A., Maize, K., Shakouri, A. and Alam, Muhammad.A. Fundamental trade-off between short-channel control and hot carrier degradation in an extremely-thin silicon-on-insulator (ETSOI) technology. In: 2015 IEEE International Electron Devices Meeting (IEDM). p. 20.3.1-20.3.4, 2015.

[17] Chenming Hu, Bokor, J., Tsu-Jae King, Anderson, E., Kuo, C., Asano, K., Takeuchi, H., Kedzierski, J., Wen-Chin Lee and Hisamoto, D. FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. IEEE Trans. Electron Devices. 47, 2320–2325, 2000. https://doi.org/10.1109/16.887014

[18] Colinge, J.-P. ed: FinFETs and Other Multi-Gate Transistors. Springer US, Boston, MA, 2008.

[19] Das, R., Rajalekshmi, T. and James, A. FinFET to GAA MBCFET: A Review and Insights. IEEE Access. PP, 1–1, 2024. https://doi.org/10.1109/ACCESS.2024.3384428

[20] Cho, M., Roussel, P., Kaczer, B., Degraeve, R., Franco, J., Aoulaiche, M., Chiarella, T., Kauerauf, T., Horiguchi, N. and Groeseneken, G. Channel Hot Carrier Degradation Mechanism in Long/Short Channel n-FinFETs. IEEE Transactions on Electron Devices. 60, 4002–4007, 2013. https://doi.org/10.1109/TED.2013.2285245

[21] Ionescu, A.M. and Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. Nature. 479, 329–337, 2011. https://doi.org/10.1038/nature10679

[22] Dennard, R.H., Gaensslen, F.H., Yu, H.-N., Rideout, V.L., Bassous, E. and

LeBlanc, A.R. Design of ion-implanted MOSFET's with very small physical dimensions. IEEE Journal of Solid-State Circuits. 9, 256–268, 1974. https://doi.org/10.1109/JSSC.1974.1050511

[23] Dhar, S., Pattanaik, M. and Poolla, R. Viability of Low Temperature Deep and Ultra Deep Submicron Scaled Bulk nMOSFETs on Ultra Low Power Applications. Journal of Electron Devices. 11, 567–575, 2011.

[24] Masuda, H., Nakai, M. and Kubo, M. Characteristics and limitation of scaled-down MOSFET's due to two-dimensional field effect. IEEE Trans. Electron Devices. 26, 980–986, 1979. https://doi.org/10.1109/T-ED.1979.19529

[25] Frank, D.J. Power-constrained CMOS scaling limits. IBM Journal of Research and Development. 46, 235–244, 2002. https://doi.org/10.1147/rd.462.0235

[26] Hook, T.B. Power and Technology Scaling into the 5 nm Node with Stacked Nanosheets. Joule. 2, 1–4, 2018. https://doi.org/10.1016/j.joule.2017.10.014

[27] Flamm, K. Measuring Moore's Law: Evidence from Price, Cost, and Quality Indexes, https://www.nber.org/papers/w24553, 2018.

[28] Taur, Y. and Ning, T.H. Fundamentals of Modern VLSI Devices, United Kingdom: Cambridge University Press,2022.

[29] Chaudhry, A. and Kumar, M.J. Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. IEEE Transactions on Device and Materials Reliability. 4, 99–109, 2004. https://doi.org/10.1109/TDMR.2004.824359

[30] Frank, D.J., Dennard, R.H., Nowak, E., Solomon, P.M., Taur, Y. and Wong, H.-S.P. Device scaling limits of Si MOSFETs and their application dependencies. Proceedings of the IEEE. 89, 259–288, 2001. https://doi.org/10.1109/5.915374

[31] Hiroki, A., Yamate, A. and Yamada, M. An analytical MOSFET model including gate voltage dependence of channel length modulation parameter for 20nm CMOS. In: 2008 International Conference on Electrical and Computer Engineering. pp. 139–143, 2008.

[32] Zabeli, M., Caka, N., Limani, M. and Kabashi, Q. Impact of MOSFET's Structure Parameters on its Overall Performance Depending to the Mode Operation. International Journal of Circuits, Systems and Signal Processing. 10, 2016.

[33] Nariai, Y. and Hiroki, A. Gate voltage dependence of channel length modulation for 14 nm FinFETs. In: 2016 IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK). pp. 1–2, 2016.

[34] Afzal, B., Ebrahimi, B., Afzali-Kusha, A. and Pedram, M. An accurate analytical I–V model for sub-90-nm MOSFETs and its application to read static noise margin modeling. J. Zhejiang Univ. - Sci. C. 13, 58–70, 2012. https://doi.org/10.1631/jzus.C1100090

[35] Jung, H. Threshold Voltage Roll-off by Structural Parameters for Sub-10 nm Asymmetric Double Gate MOSFET. TELKOMNIKA (Telecommunication Computing Electronics and Control). 16, 2444–2450, 2018. https://doi.org/10.12928/telkomnika.v16i5.10248

[36] Goel, E., Kumar, S., Rawat, G., Kumar, M., Dubey, S. and Jit, S. Two Dimensional Model for Threshold Voltage Roll-Off of Short Channel High-k Gate-Stack

Double-Gate (DG) MOSFETs. In: Jain, V.K. and Verma, A. (eds.) Physics of Semiconductor Devices. pp. 193–196. Springer International Publishing, Cham, 2014.

[37] Shih, C.-H., Chen, Y.-M. and Lien, C. An analytical threshold voltage roll-off equation for MOSFET by using effective-doping model. Solid-State Electronics. 49, 808–812, 2005. https://doi.org/10.1016/j.sse.2005.01.021

[38] Hwang, S., Im, H., Song, M., Ishida, K., Hiramoto, T. and Sakurai, T. Velocity Saturation Effects in a Short Channel Si-MOSFET and itsSmall Signal Characteristics. Journal of The Korean Physical Society - J KOREAN PHYS SOC. 55, 2009. https://doi.org/10.3938/jkps.55.581

[39] Baum, G. and Beneking, H. Drift velocity saturation in MOS transistors. IEEE Transactions on Electron Devices. 17, 481–482, 1970. https://doi.org/10.1109/T-ED.1970.17014

[40] Taylor, G.W. Velocity-saturated characteristics of short-channel MOSFETs. AT&T Bell Laboratories Technical Journal. 63, 1325–1404, 1984. https://doi.org/10.1002/j.1538-7305.1984.tb00039.x

[41] Takeda, E. Hot-carrier effects in submicrometre MOS VLSIs. IEE Proceedings: Solid-State Electron Devices. 131, 153–162, 1984.

[42] Chen, K.-L., Saller, S.A., Groves, I.A. and Scott, D.B. Reliability Effects on MOS Transistors Due to Hot-Carrier Injection. IEEE Journal of Solid-State Circuits. 20, 306–313, 1985. https://doi.org/10.1109/JSSC.1985.1052307

[43] Aur, S. Low voltage hot carrier effects and stress methodology. In: 1995 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers. pp. 277–280, 1995.

[44] Kim, N. S., Lee, H. G., Cui, Z.Y. And Kim, K. W. Electrical Characteristics of CMOS Circuit Due to Channel Region Parameters in LDMOSFET. Transactions on Electrical and Electronic Materials. 7, 99–102, 2006. https://doi.org/10.4313/TEEM.2006.7.3.099

[45] Theeuwen, S.J.C.H. and Qureshi, J.H. LDMOS Technology for RF Power Amplifiers. IEEE Trans. Microwave Theory Techn. 60, 1755–1763, 2012. https://doi.org/10.1109/TMTT.2012.2193141

[46] Wang, Z., Shi, X., Tolbert, L.M., Wang, F., Liang, Z., Costinett, D. and Blalock, B.J. A high temperature silicon carbide mosfet power module with integrated silicon-on-insulator-based gate drive. IEEE Transactions on Power Electronics. 30, 1432–1445, 2015. https://doi.org/10.1109/TPEL.2014.2321174

[47] Burdeaux, D.C. and Burger, W.R. Intrinsic reliability of RF power LDMOS FETs. In: 2011 International Reliability Physics Symposium. p. 5A.2.1-5A.2.9. IEEE, Monterey, CA, USA, 2011.

[48] Reddy, I.V.V. and Tripathi, S.L. Enhanced Performance Double-gate Junction-less Tunnel Field Effect Transistor for Bio-Sensing Application. Solid State Electronics Letters. 3, 19–26, 2021. https://doi.org/10.1016/j.ssel.2021.12.005

[49] Baruah, R.K., Mahajan, B.K., Chen, Y.-P. and Paily, R.P. A Junctionless Silicon Carbide Transistor for Harsh Environment Applications. J. Electron. Mater. 50, 5682–5690, 2021. https://doi.org/10.1007/s11664-021-09087-0

[50] Rijs, F. and Theeuwen, S.J.C.H. Efficiency improvement of LDMOS transistors for base stations: Towards the theoretical limit, 2007.

[51] Li, Y., Zhu, S., Wu, J., Hong, G. and Xu, Z. Research for radiation-hardened high-voltage SOI LDMOS. J. Semicond. 40, 052401, 2019. https://doi.org/10.1088/1674-4926/40/5/052401

[52] Xiarong, Hu., Zhang, Bo., Luo, Xi., Yao, G., Chen, Xi. and Li, Z.: A new high voltage SOI LDMOS with triple RESURF structure. J. Semicond. 32, 074006 (2011). https://doi.org/10.1088/1674-4926/32/7/074006

[53] Appels, J.A. and Vaes, H.M.J. High voltage thin layer devices (RESURF devices). 1979 International Electron Devices Meeting. 238–241, 1979. https://doi.org/10.1109/IEDM.1979.189589

[54] Charitat, G., Nezar, A. and Rossel, P. High voltage RESURF LDMOS for smart power integrated circuits. Revue de Physique Appliquée. 24, 993, 1989. https://doi.org/10.1051/rphysap:019890024010099300

[55] Belaïd, M.A., Ketata, K., Mourgues, K., Gares, M., Masmoudi, M. and Marcon, J. Reliability study of power RF LDMOS device under thermal stress. Microelectronics Journal. 38, 164–170, 2007. https://doi.org/10.1016/j.mejo.2006.08.004

[56] Casady, J.B. and Johnson, R.W. Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review. Solid-State Electronics. 39, 1409–1422, 1996. https://doi.org/10.1016/0038-1101(96)00045-7

[57] M'Sirdi, M. K., Baghaz, E., Frifita, K., Naamane, A. and Boussak, M Simulation Model of a SIC Power MOSFET - Variables Estimation and Control of a Power Source. Proceedings of the 14th International Conference on Informatics in Control, Automation and Robotics, 2017. https://doi.org/10.5220/0006460806370643.

[58] Mudholkar, M. and Mantooth, H.A. Characterization and Modeling of 4H-SiC Lateral MOSFETs for Integrated Circuit Design. IEEE Transactions on Electron Devices. 60, 1923–1930, 2013. https://doi.org/10.1109/TED.2013.2258287

[59] Singh, J. and Kumar, M.J. A Planar Junctionless FET Using SiC With Reduced Impact of Interface Traps: Proposal and Analysis. IEEE Transactions on Electron Devices. 64, 4430–4434, 2017. https://doi.org/10.1109/TED.2017.2752227

[60] Suzuki, E., Ishii, K., Kanemaru, S., Maeda, T., Tsutsumi, T., Sekigawa, T., Nagai, K. and Hiroshima, H. Highly suppressed short-channel effects in ultrathin SOI n-MOSFETs. IEEE Transactions on Electron Devices. 47, 354–359, 2000. https://doi.org/10.1109/16.822280

[61] Tunnel FET, https://masumnawaz.wordpress.com/emerging-nano-devices/, 2015.

[62] Ghosh, B. and Akram, M.W. Junctionless Tunnel Field Effect Transistor. IEEE Electron Device Letters. 34, 584–586, 2013. https://doi.org/10.1109/LED.2013.2253752

[63] SentaurusTM, Device User Guide, Version R-2020.09, September 2020. Mountain View, CA, Available online: https://www.synopsys.com, 2020. (Accessed 15 March 2023).

[64] Sentaurus Device User: Sentaurus TCAD Version R-2020.09-SP1.

[65] Mahapatra, S., Parihar, N.: A review of NBTI mechanisms and models. Microelectronics Reliability. 81, 127–135, 2018. https://doi.org/10.1016/j.microrel.2017.12.027

[66] Suh Song, Y., Yeong Kim, K., Young Yoon, T., Jung Kang, S., Kim, G., Kim, S. and Hyun Kim, J. Reliability improvement of self-heating effect, hot-carrier injection, and on-current variation by electrical/thermal co-design. Solid-State Electronics. 197, 108436, 2022. https://doi.org/10.1016/j.sse.2022.108436

[67] Huard, V., Denais, M. and Parthasarathy, C. NBTI degradation: From physical mechanisms to modelling. Microelectronics Reliability. 46, 1–23, 2006. https://doi.org/10.1016/j.microrel.2005.02.001

[68] Aishwarya, K. and Lakshmi, B. Radiation study of TFET and JLFET-based devices and circuits: a comprehensive review on the device structure and sensitivity. Radiation Effects and Defects in Solids. 178, 229–257, 2023. https://doi.org/10.1080/10420150.2022.2133708

[69] Fleetwood, D.M. Radiation Effects in a Post-Moore World. IEEE Trans. Nucl. Sci. 68, 509–545, 2021. https://doi.org/10.1109/TNS.2021.3053424

[70] Lho, Y.H. and Kim, K.Y. Radiation Effects on the Power MOSFET for Space Applications. ETRI J. 27, 449–452, 2005. https://doi.org/10.4218/etrij.05.0205.0031

[71] Karmakar, A., Wang, J., Prinzie, J., De Smedt, V. and Leroux, P. A Review of Semiconductor Based Ionising Radiation Sensors Used in Harsh Radiation Environments and Their Applications. Radiation. 1, 194–217, 2021. https://doi.org/10.3390/radiation1030018

[72] Kim, W., Han, J., Tcho, W., Park, J., Yu, J., Choi, Y. Triboelectric nanogenerator for a repairable transistor with self-powered electro-thermal annealing,Nano Energy,Volume 76, 2020, 105000, ISSN 2211-2855, https://doi.org/10.1016/j.nanoen.2020.105000.

[73] Schwank, J.R., Winokur, P.S., Sexton, F.W., Fleetwood, D.M., Perry, J.H., Dressendorfer, P.V., Sanders, D.T. and Turpin, D.C.: Radiation-Induced Interface-State Generation in MOS Devices. IEEE Trans. Nucl. Sci. 33, 1177–1184, 1986. https://doi.org/10.1109/TNS.1986.4334575

[74] Sujatha, R., Damle, R., Khan, A.R. and Ravindra, M. Study of the effect of gamma radiation on MOSFET for space applications. Indian Journal of Pure and Applied Physics. 56, 587–590, 2018

[75] Onnasch, D. and Reimerdes, H.P. Radiation effects in n-channel MOSFETS. Solid-State Electronics. 17, 663–666, 1974. https://doi.org/10.1016/0038-1101(74)90088-4