CHAPTER 2

Reliability Assessment and Circuit Applications of LDMOS Transistor in Harsh Environments

Contents

2.1 Introduction

LDMOS transistors emerged around two decades ago as replacements for conventional MOSFETs in RF power applications. Today, LDMOS transistor has become the industry standard across various applications, ranging from base stations, broadcast, frequency modulation (FM), very high frequency (VHF), ultra-high frequency (UHF), and radar, to newer domains such as microwave cooking and RF lighting. This widespread adoption is attributed to the substantial advancements in RF performance achieved over time [1–4]. High switching speeds, lower ON-resistance, and compatibility with integrated circuit technologies are just a few of the benefits that MOSFETs have to offer. However, in some high-power RF applications, their limited power handling capacity and vulnerability to self-heating effects may be drawbacks. The frequency range has been extended to include worldwide inter-operability for microwave access (WiMAX) and wide-band radar frequencies, ranging from 1 MHz to 10 GHz. From a few watts to several thousand watts, LDMOS transistor operates over a broad power spectrum. Efficiency enhancement is a major motivator, particularly for base stations, where Doherty amplifiers and DPD are used in current systems to boost efficiency [5, 6]. Because of its high gain, efficiency, and affordability, LDMOS transistor is a good fit for these types of systems.

MOSFETs have been a staple in electronics for few decades, finding use in nearly every imaginable application. However, in scenarios requiring high power, traditional MOSFETs encounter limitations such as elevated ON-resistance, restricted maximum voltage ratings and current densities, compromised performance under high temperatures, relatively high gate voltage (V_{GS}) requirements for full activation, and the presence of parasitic capacitances. LDMOS transistor overcome these issues and has high power density and linearity, high breakdown voltage, efficiency, and offers higher gain, etc [1]. High-voltage devices are mostly used for switching and rectifying, and in order to do these tasks, two important requirements must be met - (a) There shouldn't be any electrical contact between the terminals when the device is in the open position, prohibiting current flow. (b) When the device is closed, current should pass through it without being lost. To achieve these advantages, an LDMOS transisor has to be structurally different from a conventional MOSFET by the fact that the former has a laterally diffused channel, a thicker drain drift region, a buried drain contact, a thicker

gate oxide (T_{OX}), and a larger layout [7–10]. The thick and highly-doped drift region in LDMOS transistor can withstand high electric field and therefore, the device can work at high voltages without breakdown. Also, higher doping concentration reduces the resistance of the device, which results in lower power dissipation and higher efficiency [10]. Moreover, the lateral diffusion regions benefit from spreading of the electric field and help reduce breakdowns [11].

In summary, the amalgamation of a highly-doped drift region and a lateral diffusion region marks LDMOS devices well-suited for high-power and high-efficiency RF amplification such as cellular base stations, broadcasting, radar systems, industrial and automobile applications, microwave ovens, etc. Depending on power handling capability, breakdown voltage, frequency range, etc. there have been different types of LDMOS transistor reported till now according to their specific operation, such as Low-Noise LDMOS, Enhancement Mode LDMOS, High-Frequency LDMOS, Low drain doping LDMOS etc. [7-11].

2.2 Laterally Diffused Metal-Oxide-Semiconductor (LDMOS) Device Structure and Operation

The LDMOS transistor consists of two distinct regions: the channel and the drift region. The structure includes an N-type substrate layer with a P-type doped region formed within it. Near the P-base, there's a drift region with N-type doped, which extends from channel towards the drain. On either side of the gate, heavily doped N+ source and drain regions are situated shown in Fig. 2.1. This design facilitates efficient control of current flow between the source and drain terminals by the gate voltage, with the drift region enabling high-voltage operation and reducing on-resistance. Short channels offer benefits such as achieving high transconductance, ensuring good high-frequency performance, and maintaining linearity by operating in velocity saturation. The drift region, extending from the channel's drain end to the drain contact, serves to handle applied voltage and safeguard the channel from high voltage. Finding the greatest possible balance between two important factors is critical to the design of RF-LDMOS devices: breakdown voltage (V_{BD}) and ON-resistance (R_{ON}). Maintaining their optimum value is necessary to maximize the RF-LDMOS device's performance. The ON-resistance tends to decrease when the breakdown voltage is increased, and vice

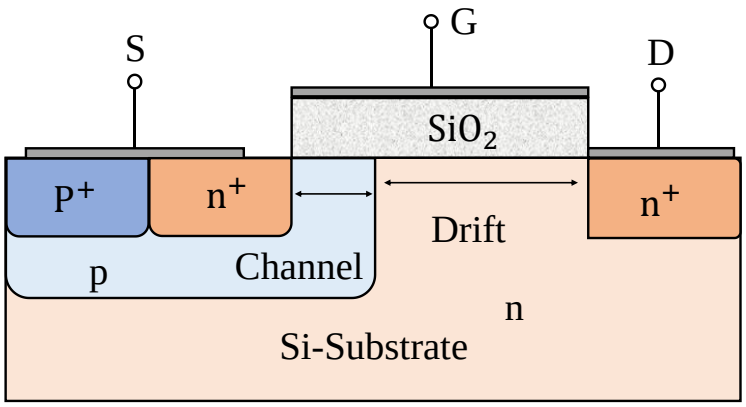

Fig. 2.1: Basic structure of the n-channel LDMOS.

versa [12]. There is a correlation in an idealized device between the parallel-plane breakdown voltage and the specific ON-resistance ($R_{ON,sp}$) [13].

$$R_{ON,sp} = \frac{4V_{BD}^2}{\varepsilon_s \mu E_C^3} \tag{2.1}$$

In the given equation, ε_s represents the dielectric constant of the material, μ stands for the mobility, and E_c denotes the critical electric field of the material. The specific on-resistance, denoted as $R_{on,sp}$, is the on-resistance normalized to the area of the device.

It is common practice to include a low-doped drift (LDD) zone between the gate and drain in order to improve V_{BD} and decrease feedback capacitance (C_f). By dispersing the electric field and lowering the probability of breakdown, the LDD zone contributes to an increase in V_{BD}. It also helps lower C_f, which by minimizing parasitic capacitance effects, can enhance high-frequency performance [8].

On the other hand, R_{ON}, frequently increases as the LDD region is introduced. RF performance may be seriously harmed by this increase in R_{ON}, especially in terms of operating frequency and power efficiency. Greater R_{ON} values may restrict the device's capacity to process high-frequency signals effectively, which may affect the cut-off frequency and overall radio frequency performance of the device.

2.3 Reliability concern of LDMOS Transistor

Because of the high operating power and frequencies of these applications, a substantial amount of heat is generated, which may concern the performance as well as the reliability of the device [14]. In addition, for applications such as radar applications, or similar industrial applications, the device has to face radiation. In this thesis effect of

gamma radiation (electromagnetic radiation that has a high energy and shorter wavelength) effect on device performance is explored. Radiation may cause ionization to form electron-hole pairs (EHP) and change the V_{TH} of the device and therefore, creating reliability concerns [15, 16]. To reduce these effects, several mitigation strategies, such as device layout optimization, radiation-hardened device design, and circuit-level design strategies, have been proposed [17–19]. Many works have been reported on the radiation study of LDMOS and other transistors. Lei *et al*. reported that high temperature degrades the device performance under the total-ionizing dose (TID) effect of an LDMOS; furthermore, the transient response is affected by dose rate and radiation time [20].

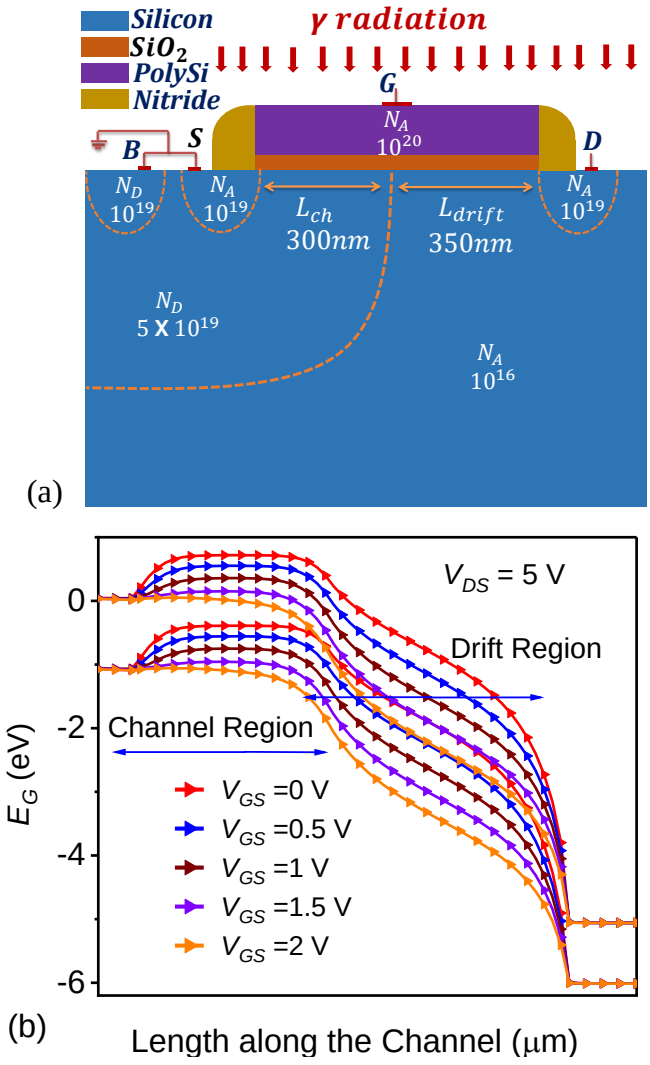

Fig. 2.2: (a) Schematic diagram of the LDMOS [27]. (b) Band diagram (pre-radiation) along the channel at $V_{DS} = 5V$, $T_{OX} =$ 20 nm, $L_{ch} =$ 300 nm and $L_{drift} =$ 350 nm.

The n-type LDMOS degrades at a slower rate than the p-type under TID radiation; in addition, TID degrades the parasitic capacitances coupling thereby resulting in lower switching losses [21]. However, $1/f$ noise was shown to be more significant for pMOS devices than for an nMOS device under moisture exposure [22]. Dubey et al., demonstrated that TID is more prominent for higher doping concentrations [23]. They also reported that a junctionless transistor is lesser prone to radiation effects [24]. It is also demonstrated that the effect of radiation is worse with scaling the devices [25]. It is claimed with a simulation that multigate transistors are lesser prone to TID radiation [26]. Mahajan et al demonstrated that HCD and TID are strongly correlated in an LDMOS. Unlike normalcy, TID can actually increase the overall hot carrier degradation (HCD)-limited lifetime for an LDMOS transistor [27]. They also explained based on experimental results that, HCD in an LDMOS is structurally and functionally different fundamentally; and an analogous universal scaling cannot apply. Using a two MOS model of an LDMOS, they derived a universal model for HCD of an LDMOS [28]. It is also reported that the changes in oxide and interface-trap charge with irradiation temperature affect the response of these devices more significantly than border traps [29]. Temperature fluctuations cause thermal effects, which have a substantial influence on semiconductor performance and can result in deterioration and reliability problems [11]. Because of their improved linearity, frequency characteristics, and thermal stability, LDMOS transistors, which are evolved from silicon MOSFETs are perfect for complicated modulations found in mobile phone standards. They boost power density, efficiency, and power gain in base stations by optimizing power consumption, thermal management, and efficiency [1, 14, 15]. The device's efficiency is increased by the double-diffused structure's reduction of ON-resistance. The super-junction construction lowers switching losses and increases the device's overall effectiveness in addition to better high voltage and high-power application favorites [27]. Despite these advantages, one of the critical issues of a laterally diffused MOSFET (LDMOS) is it has hot carrier degradation (HCD) at higher voltages and power [28].

Fabricating an n^+ region with $N_D = 1 \times 10^{19}$ cm^{-3} in an n^+-region/ well of $N_D = 5 \times 10^{19}$ cm^{-3} is technically challenging. The doping process can be controlled through techniques like ion implantation or diffusion to achieve different doping concentrations within the same region. The lower-doped region would exhibit a slightly

reduced carrier concentration, which could be useful for tuning device characteristics such as reducing the series resistance while maintaining adequate contact properties. This approach allows for precise tailoring of the electrical properties in specific regions of the device [60].

The gate material used is typically polysilicon or a metal gate with a work function carefully chosen to align with the desired threshold voltage. The simulation also takes into account Fermi-Dirac statistics for carrier distribution and Schottky contact models to simulate the gate work function behavior accurately, which is essential for high-performance transistor operation. For this structure, a work function that matches the mid-gap of silicon or slightly lower (around 4.6-4.8 eV) is used to balance the threshold voltage and achieve optimal device performance under high-temperature and high-radiation environments [27].

The contact metal used on the gate terminal is usually a low-resistance material like aluminum or tungsten to ensure good electrical conductivity and compatibility with the gate material, minimizing contact resistance and ensuring reliable operation. Aluminum is a good heat conductor with a thermal conductivity of 237 W/m K, while tungsten has a thermal conductivity of 173 W/m K. [61]

In this work, we have done extensive simulation studies for analog performance parameters such as V_{TH}, G_M, f_T, R_0, etc for a LDMOS device under R_{dose}. The device is also studied for $1/f$ noise under radiation. The device is calibrated with a fabricated LDMOS that offers lower hot carrier degradation (HCD) under gamma radiation.

2.4 Calibration of LDMOS Transistor with experimental data and Simulation Setup

The schematic diagram of the LDMOS transistor is shown in Fig. 2.2(a). The performance of LDMOS transistors, more especially under radiation, is dependent on operating conditions including the electric field and reliability issues, such as oxide thickness. The band diagram with different gate voltages at $V_{DS} = 5$ V is shown in Fig. 2.2(b). The calibration of the simulation framework with the fabricated device is performed to validate the models used for simulation, for any process variations, optimizing performance and reliability, ensuring that it accurately reflects the real device behavior. The **maximum % error** between simulation and measured data in Fig. 2.3 is approximately 5-**14%** as calculated from the experimental and simulated results.

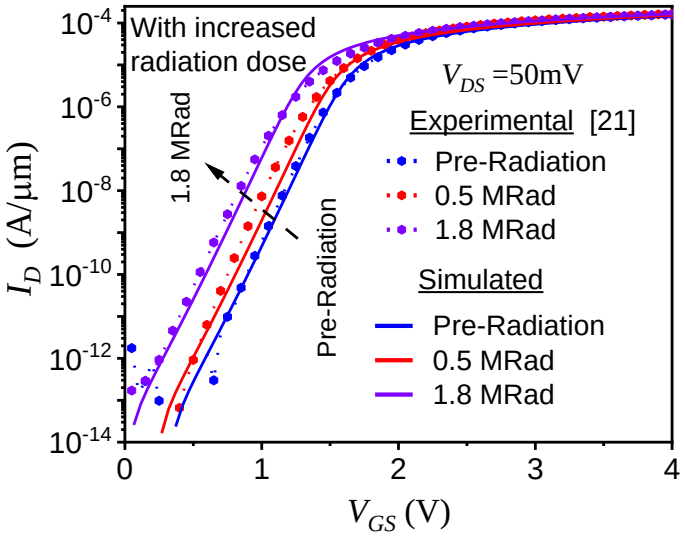

Fig. 2.3: Calibration without and with radiation (0.5MRad and 1.8MRad) for $T_{OX} =$ 20 nm, $L_{ch} =$ 300 nm and $L_{drift} =$ 350 nm and $V_{DS} =$ 50mV [27].

We have considered gamma radiation for this study with the TCAD simulator (version R-2020.09-SP1) [30]. The device is calibrated with the dimension of oxide thickness ($T_{OX} = 20$nm), channel length ($L_{ch} = 300$ nm) and drift length ($L_{drift} = 300$ nm) at an operating dc voltage of ($V_{GS} = 0 - 5$ V) and ($V_{DS} = 50$ mV) with the experimental work of Mahajan et al [27].

The simulation test structure in Fig. 2.2 was created using a finely-tuned mesh/grid to ensure accurate representation of device features, with grid statistics optimized for convergence and precision.

Total Nodes: 5000

Total Elements: 9000 (e.g., triangles in 2D)

Min Element Size: 1 nm (near junctions)

Max Element Size: 10 nm (in bulk regions)

Doping concentrations in different regions were selected based on established device design principles and targeted electrical characteristics, ensuring optimal performance under high-temperature and high-radiation conditions. A shorter channel

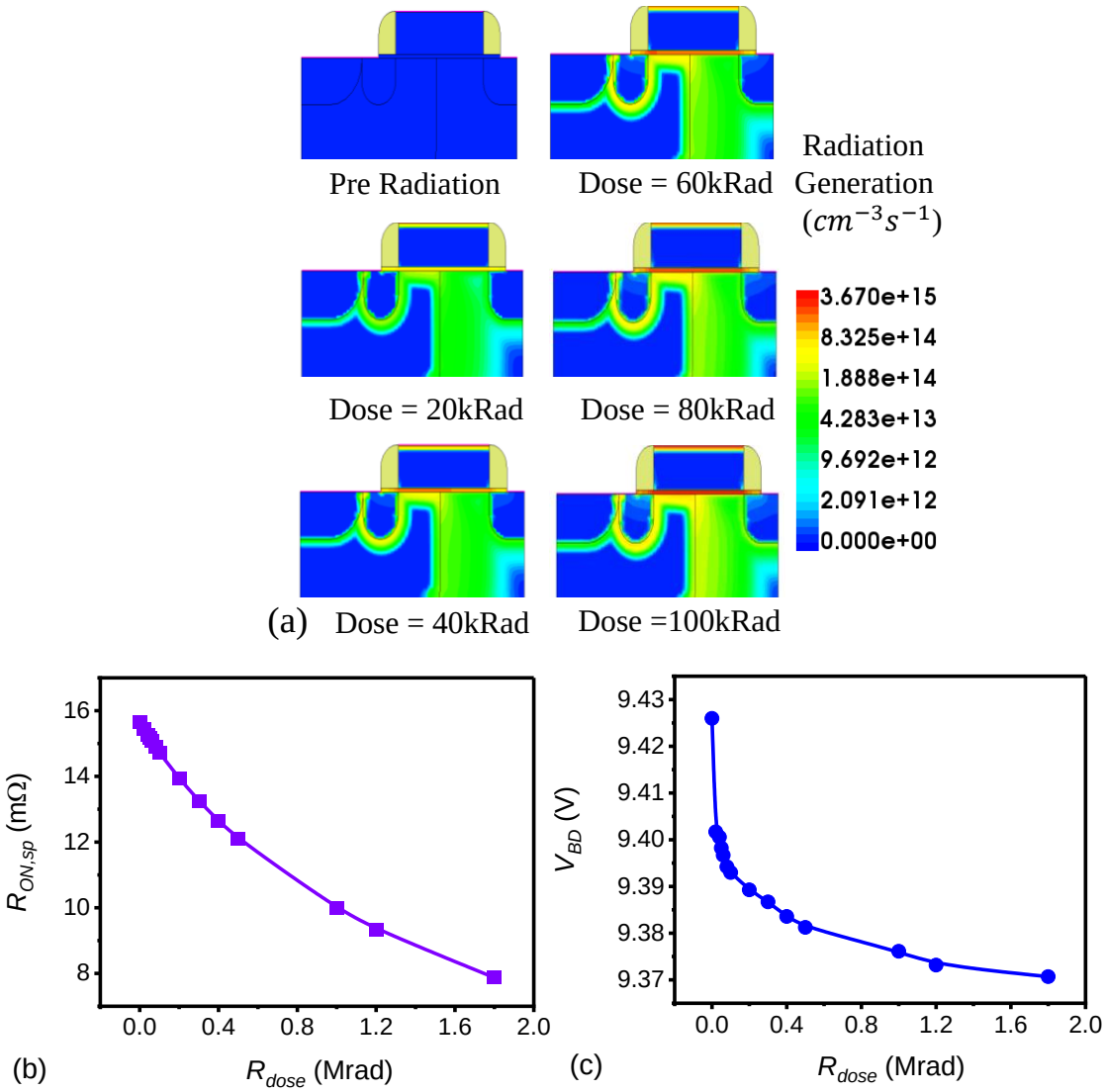

Fig. 2.4: (a) Electron-hole pair (EHP) generation profile (b) Specific ON resistance ($R_{ON,sp}$) at $V_{DS} = 2V$ (c) Breakdown voltage (V_{BD}) with D. $T_{OX} = 20$ nm, $L_{ch} = 300$ nm and $L_{drift} = 350$ nm.

length improves trans conductance and switching speed, but could lead to lower breakdown voltage. The drift region length is extended to handle higher voltages and reduce electric field concentration, improving breakdown voltage while increasing ON-resistance.

Furthermore, the simulations are also calibrated with experimental results at pre-radiation and with the radiation doses (R_{dose}). While calibrating, dose-dependent Interface traps (N_{it}) and bulk trapped (N_{ot}) charges were considered using equations expressed as [38]:

$$\mathrm{N_{ot}} = (1 - \mathrm{a_{ot}})\mathrm{G_{TID}}\mathrm{t} \tag{2.2}$$

$$N_{it} = (1 - a_{it})a_{it}D^{b_{it}} \quad (2.3)$$

Where, a_{it} (cm-2·rad-1) and b_{it} are the fitting coefficients, which values, as calculated in [36], G_{TID} = Total EHP generation rate due to γ radiation, D = R_{Dose} (rad).

The transfer characteristic of the LDMOS transistor and its semi-log plot at $V_{DS} = 50$ mV shows a good match with experimental results both without radiation and with R_{dose} of 0.5MRad and 1.8MRad, plotted in Fig. 2.3. Silicon substrate with total thickness of 1$\boldsymbol{\mu}$m was used as the semiconductor material and SiO_2 was used as a gate oxide material $T_{OX} = 20$nm. Fig. 2.4(a) represents the EHP generation profile with R_{dose}, which can have an impact on the specific ON-resistance ($R_{ON,sp}$) of LDMOS devices. The EHP generation with R_{Dose} is extracted using the below relation [30].

$$G_{max} = g_0 \frac{dR}{dt}\left(\frac{|E|+E_0}{|E|+E_1}\right)^m \quad (2.4)$$

Here g_0 is the number of EHP generated per unit dose in unit volume. dR/dt is radiation dose rate (rad/s), $Y(\vec{E})$ is the fractional yield function. For SiO_2 material, the value of g_0 is 7.88×10^{12} $\text{rad}^{-1}\text{cm}^{-3}$, $E_0 = 0.1$ V/cm, a term to ensure convergence; $E_1 = 0.55$ MV/cm and m = 0.7 for γ irradiation. $R_{ON,sp}$ of LDMOS transistor decrease with R_{dose} due to the creation of EHP within the device caused by ionizing radiation which is shown in Fig. 2.4(b). $R_{ON,sp}$ is extracted as V_{DS}/I_{DS} from output characteristics of the device at $V_{GS} = 2$V, where I_{DS} here is the drain current at which current starts saturating in the I_{DS}-V_{DS} characteristic. In particular, the formation of EHP can raise the number of trapped charges in the gate oxide layer, which can then increase leakage current and reduce gate oxide integrity, both of which can lower on-resistance. Radiation exposure has the potential to influence an LDMOS device's breakdown voltage (V_{BD}), the relationship between V_{BD} and R_{dose} is intricate and dependent on several variables such as T_{OX}, channel and drift doping concentration, temperature, mobility, material properties, device geometry, etc [31].

The breakdown voltage (V_{BD}) is the drain voltage at which I_{DS} increases rapidly in the I_{DS}-V_{DS} characteristics at $V_{GS} = 0$V. As shown in Fig. 2.4(c), with an increase in the R_{dose}, V_{BD} decreases marginally. Without radiation, the relationship between $R_{ON,sp}$ and $V_{BD}$was given by Baliga Figure of merit ($V_{BD}^2/R_{ON,sp}$), according to which, $R_{ON\,sp}$ increases with V_{BD} [32]. As $R_{ON,sp}$, and V_{BD} are extracted from transfer and output characteristics that are calibrated with experimental device at room temperature, these

values are expected to represent near close values for real devices.

The drift-diffusion transport model with Fermi statistics is used for solving the physics of the device. Shockley-Read-Hall (SRH) recombination is taken into account, which explains how carriers recombine by being trapped and released at flaws in the semiconductor crystal lattice. In order to imitate carrier mobility in semiconductors, the IALMob model is used. The carriers are distributed within the same band according to the model's presumption that intra-valley scattering limits mobility. The effective mass of the carrier and the scattering time are two variables in the IALMob model that can be computed theoretically or determined through experimental observations. Finally, the "Old Slot-boom" model is used for bandgap narrowing. All simulations are performed at a room temperature of 300 K. Hot carrier degradation (HCD) model is used to explore the defects and to adjust impurity scattering [30]. The HCD model's ability to anticipate the device's lifetime and dependability under different operating situations is one of the key benefits of employing it in LDMOS transistor [28, 29]. Using the same simulation setup, various DC and small-signal AC simulations were performed.

The IALMob model considers both inversion and accumulation layer mobility model. For small values of electric field, the acoustic phonon and surface roughness components of IALMob make an insignificant contribution to the total mobility. This mobility model is already included with doping dependency of the device layer. In the simplest form, the mobility (μ) of a charge carrier in a material can be expressed as [33]:

$$\mu = q * \tau / m \tag{2.5}$$

where: $\mu \rightarrow$ mobility of the carrier, $q \rightarrow$ charge of the carrier, $\tau \rightarrow$ scattering time of the carrier, $m \rightarrow$ effective mass of the carrier. The scattering time represents the average time between carrier scattering events, while the effective mass characterizes the carrier's behavior in response to external forces. These equations not capture all the complexities of carrier transport in different materials and conditions. More sophisticated models equations exist to describe mobility in specific systems in Sentaurus TCAD numerically [30]. In this technique the scattered wave is treated as the sum of spherical waves whose phase shift with respect to the incident wave has changed due to the scattering process. Compared to the Born approximation, phase shift analysis is a more accurate technique, albeit computationally more expensive as well [34]. The

ratio of repulsive to attractive scattering cross section (G(P)) is the same as the ratio of majority to minority mobilities. Klaassen has modeled this ratio using a seventh-order spline function

$$\frac{\mu_{maj}}{\mu_{min}} = G(P) = 1 - \frac{s_1}{\left[s_2 + \left(\frac{m_0}{m}\frac{T}{300}\right)^{s_4} P\right]^{s_3}} + \frac{s_5}{\left[\left(\frac{m_0}{m}\frac{T}{300}\right)^{s_7} P\right]^{s_6}} \tag{2.6}$$

Parameter P depends on carrier concentration and temperature as

$$P = \frac{1.36\times10^{20}}{n}\left(\frac{m_0}{m}\frac{T}{300}\right)^2 \tag{2.7}$$

$m_0 \rightarrow$ free electron mass, and $T \rightarrow$ temperature of the electron gas. Therefore, mobility

due to minority impurity scattering may be represented with majority impurity scattering mobility as

$$\mu_{coul}^{minority} = \frac{\mu_{coul}^{majority}}{G(P)} \tag{2.8}$$

2.5 Parametric Investigation of LDMOS Transistor at High Temperature and High Radiation Environment

2.5.1 N_{it}, N_{ot} and V_{TH} shift with TID

The transfer characteristics of the device are shown in Fig. 2.5(a) at a drain voltage $V_{DS} = 1V$, oxide thickness, $T_{OX} = 20nm$, channel length, $L_{ch} = 300\ nm$, channel drift length, $L_{drift} = 300\ nm$. With an increase in the radiation dose, OFF-state current (I_{OFF}) increases, while ON-state current (I_{ON}) remains same making I_{ON}/I_{OFF} to be decreased with radiation dose. The The surface potential (φ_S) of the device along with channel length for different R_{dose} are plotted in Fig. 2.5(b). As expected, φ_S which increases with R_{dose}, because of e-h pair generation (EHP) and accumulation at the interface and bulk oxide region. The V_{TH} of the device with R_{dose} at a V_{DS} of 1V is shown in Fig. 2.5(c) for a R_{dose} till 1.8MRad. The V_{TH} is measured using the constant current method at a constant drain current $I_D = 1\times10^{-7}$ A/μm from the transfer

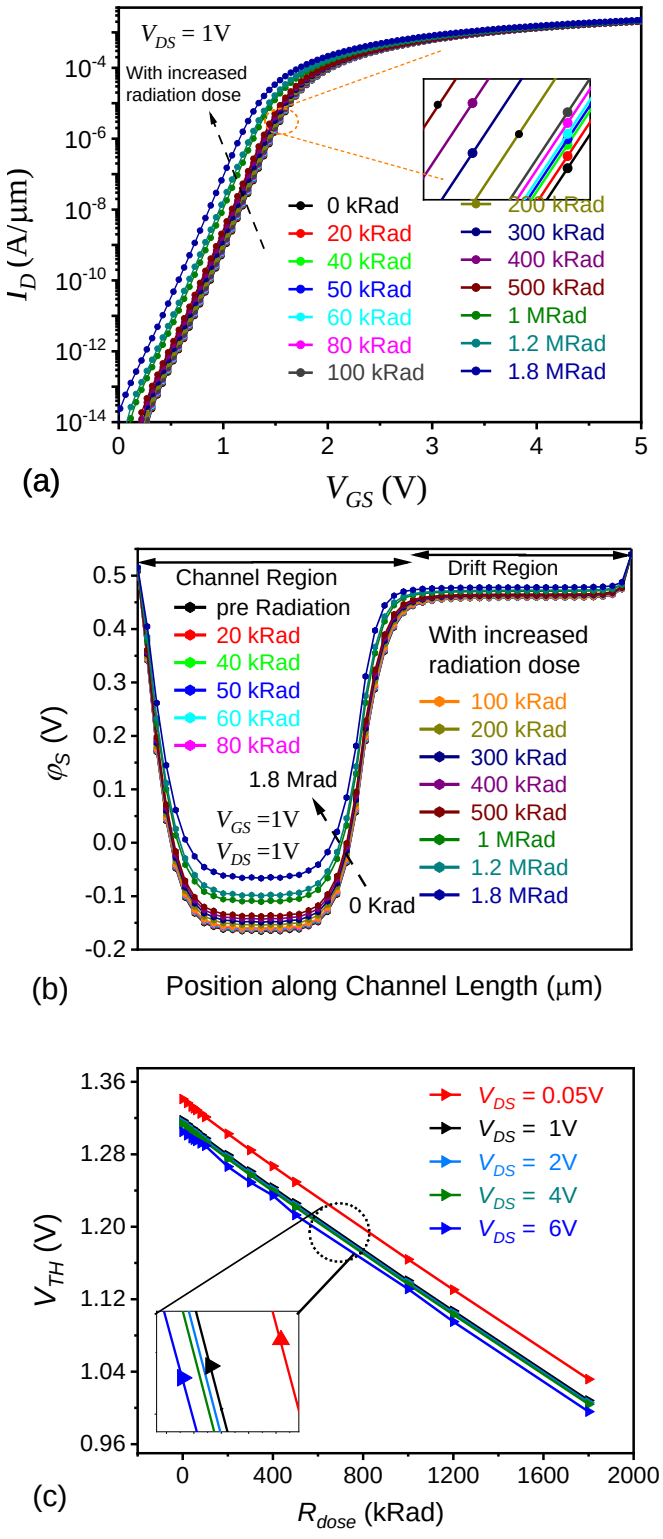

Fig. 2.5: (a) Transfer characteristics at $V_{DS} = 1\text{V}$ (b) Surface potential (φ_S) at $V_{GS} = 1\text{V}, V_{DS} = 1\text{V}$ (c) threshold voltage (V_{TH}) and with radiation dose (R_{dose}) at $T_{OX} = 20$ nm, $L_{ch} = 300$ nm and $L_{drift} = 350$ nm and $V_{DS} = 0.05\text{V}, 1\text{V}, 2\text{V}, 4\text{V}$ and 6 V.

characteristics at V_{DS} = 1V, the value of V_{GS} is taken as the threshold voltage of the device. At this current level, the device's operation is in a range where short-channel

effects, velocity saturation, and other non-ideal phenomena are minimized. This allows for a more accurate determination of the threshold voltage, as these effects can skew results at higher currents [28]. With an increase in the R_{dose}, V_{TH} decreases, indicating that the oxide is thick, and the trapped charges cannot escape through tunneling, even with an increase in the electric field [35–37]. Therefore, accumulated N_{it} and N_{ot} determine the V_{TH} shift. With increased R_{dose}, for an n-type LDMOS, where N_{bulk} is significantly higher than N_{it}, shifts the V_{TH}. We have measured the N_{it} and N_{ot} generated with R_{dose} for different input V_{GS} from the simulator, shown in Fig. 2.6(a) and Fig. 2.6(b) respectively. With a R_{dose} increase of 500krad, there is a V_{TH}shift of ~0.1V, which is not negligible. Any change in V_{TH} is not recommended for practical use. However, for a radiation dose of more than 500krad, that corresponds to V_{TH} shift of ~0.1V, may have adverse effect on device performance [38]**.** The device also does not show drastic ON-resistance (R_{ON}) change.

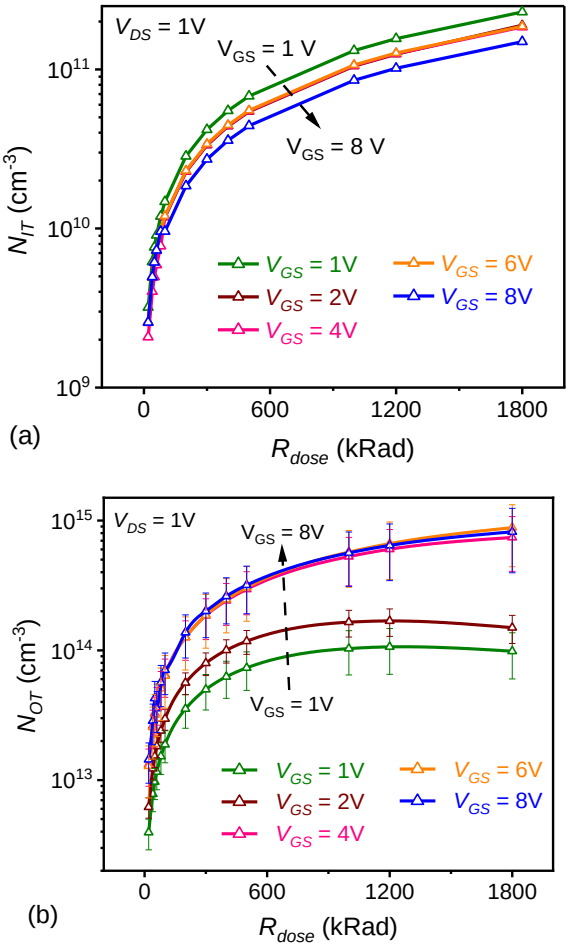

Fig. 2.6: (a) Interface trap charges and (b) bulk trap charges with radiation dose (R_{dose}) at T_{OX} = 20 nm, L_{ch} = 300 nm and L_{drift} = 350 nm and V_{DS} = 1 V.

The bigger shifts in R_{ON} indicate more mobility degradation at the drift region caused by more N_{it} generation with increased radiation. Increased R_{ON} signifies more (I^2R) loss that will accelerate self-heating effects (SHE), and eventually may lead to hot carriers' injection (HCI) effects [10]. As aforementioned, ionizing radiation causes more EHP generation in an LDMOS transistor, leading to trapped charge growth. In other words, we can say, the effective V_{GS} is decreased as a result of the trapped charge by a reduction in the E across the oxide layer. The total generation rate due to radiation is expressed as [39]

$$G_r = g_0 \frac{dR}{dt} Y(\vec{E}) \tag{2.9}$$

Here g_0 is the number of EHP generated per unit dose in unit volume. dR/dt is R_{dose} rate (rad/s), $Y(\vec{E})$ is the fractional yield function. For SiO_2 material the value of g_0 is $= 7.88 \times 10^{12}$ $\text{rad}^{-1}\text{cm}^{-3}$. The probability for generated carriers to escape recombination is given by fractional yield function, $Y(\vec{E})$ [36].

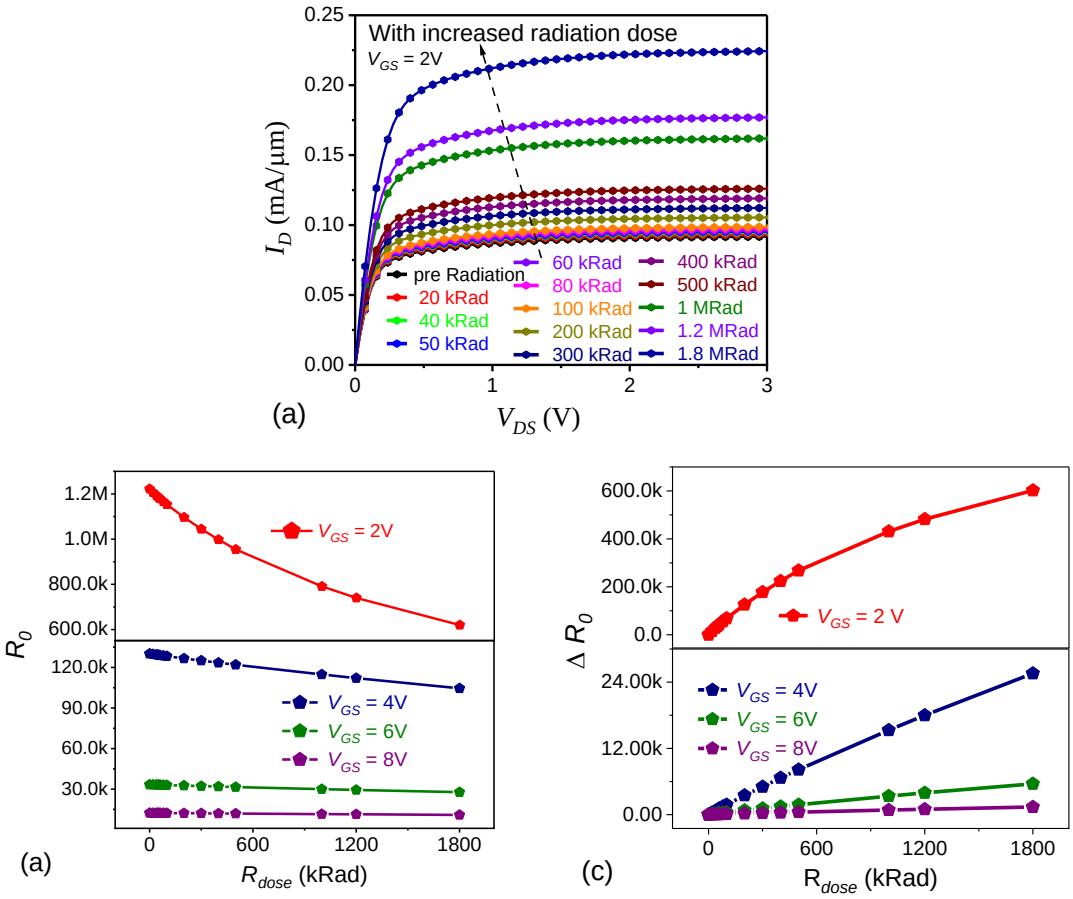

Fig. 2.7: (a) Output characteristics (b) output resistance and (c) change in output resistance with TID at T_{OX} = 20 nm, L_{ch} = 300 nm and L_{drift} = 350 nm and V_{DS} = 1 V.

$$Y(\vec{E}) = \left(\frac{|E|+E_0}{|E|+E_1}\right)^m \quad (2.10)$$

Where, $E_0 = 0.1\ \mathrm{V/cm}$, a term to ensure convergence; $E_1 = 0.55\ \mathrm{MV/cm}$ and $m = 0.7$ for γ irradiation.

R_{dose}, therefore, enhances the interface traps accumulated at the oxide-semiconductor (SiO_2/Silicon) interface. These trapped charges may trap or release charge carriers, which modulates the device V_{TH} and hence gate-channel capacitance [31]. Depending on the type and placement of the traps, the development of N_{it} and N_{ot} can change V_{TH} of the transistor [35]. An empirical formula that connects V_{TH} shift to the R_{dose} and other factors like the N_{ot} and N_{it} can be used to model V_{TH} with R_{dose} for LDMOS [36]. Using calibration methodology, we have analyzed other important circuit design parameter effects with total R_{dose} like G_M, f_T, R_0, C_{GS} and C_{GD}, etc. N_{ot} and N_{it} gate-channel capacitance and the V_{TH} is calibrated for the simulations in the radiation study. N_{it} can be calculated by integrating $D_{it}(E)$ through the band-gap:

$$N_{it} = \int_{E_1}^{E_2} D_{it}(E)dE \quad (2.11)$$

$D_{it}(E)$ is the density of N_{it} per unit of energy. E_1 and E_2 depend on the substrate doping density and the carrier capture cross-section, among other parameters. Assuming an energy level model describing the electrical behavior of the trap D_{it} can be described by an acceptor level of 0.3 eV from the valence band ($E_v + 0.3$ eV) and a donor level of 0.8 eV ($E_c + 0.8$ eV).

We have also incorporated the mathematical models for the calibration of N_{it} and N_{ot} given in equation below based on experimental data, in our TCAD simulator. This gives more near-practical changes in N_{it} and N_{ot} and hence device behavior changes with TID. V_{TH} can be expressed as a function of N_{ot} and N_{it} and can be extracted from equations 2.2 and 2.3.

2.5.2 Output resistance (R_0) shift with TID

The output current of the LDMOS with radiation is shown in Fig. 2.7(a) at $V_{GS} = 2$V. As expected, the output current increases with radiation dose as the electron-hole pair (EHP) generation is increased. The output resistance affects the performance of a device in both linear and switching applications. R_0 affects the performance of a device in both linear and switching applications. R_0 is primarily determined by the channel resistance

and the parasitic resistance associated with the device's layout. Radiation may increase the channel resistance of an LDMOS transistor by introducing additional trapped charge in the gate oxide, which reduces the device's conductivity. This increase in channel resistance leads to a decrease in R_0. Also, parasitic resistances associated with radiation may add up to R_0. The value of R_0 decreases with an increase in V_{GS} for the same reason as shown in Fig. 2.7(b). For shorter channel length, due to the channel length modulation (CLM) phenomenon, I_{DS} increase with drain bias and hence R_0 reduces. As the channel length in this study is 300nm, the effect of CLM will not be high. The change in resistance with R_{dose} is shown in Fig. 2.7(c).

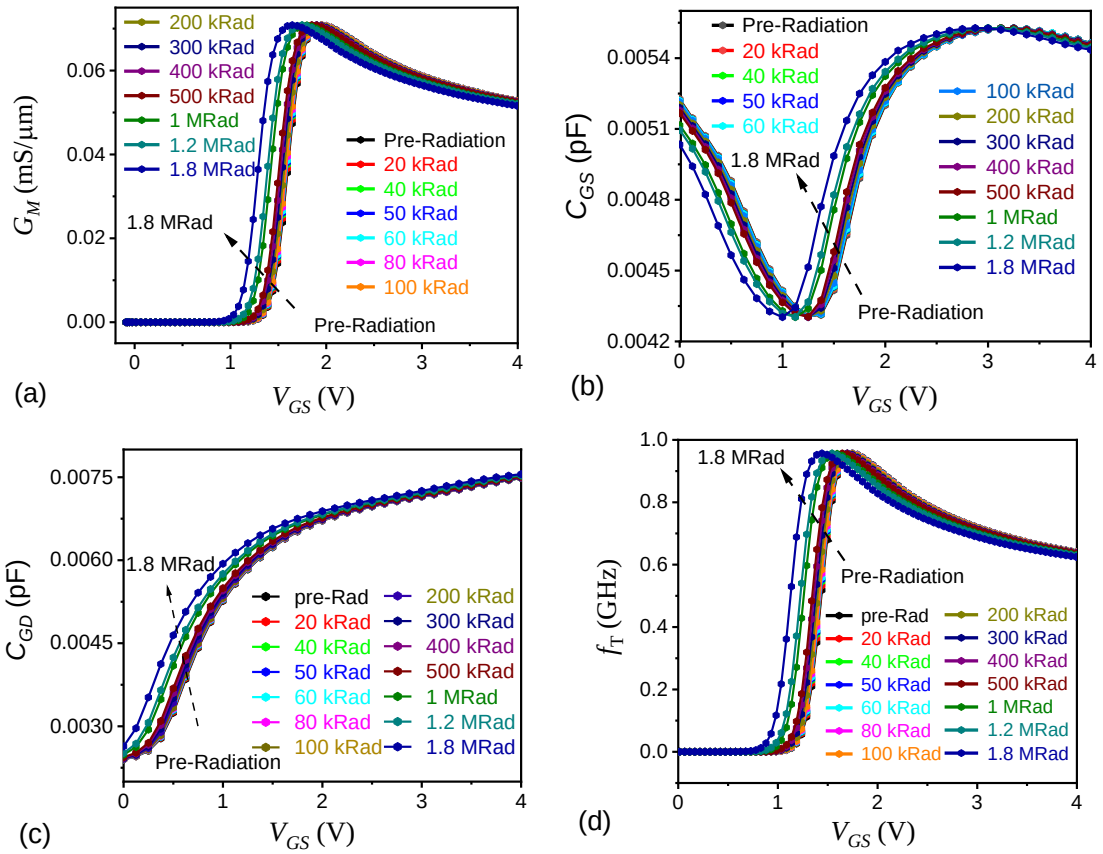

Fig. 2.8: (a) Transconductance, G_M (b) gate to source capacitance, C_{GS} (c) gate to drain capacitance, C_{GD} and (d) unity gain cut-off-frequency, f_T with TID for $T_{OX} = 20$ nm, $L_{ch} = 300$ nm, $L_{drift} = 350$ nm, $V_{DS} = 1$ V and input frequency, $f_i = 1$MHz.

2.5.3 Unity gain cut-off frequency (f_T) shift with TID

LDMOS has applicability in high-power applications, such as RF power amplifiers, switching power supplies, motor drives, etc. The LDMOS structure is designed to reduce the on-resistance of the device and improve its thermal performance,

enabling it to handle high power levels without overheating. Enhancement-mode LDMOS devices are commonly used in high-power RF amplifier applications, while depletion-mode LDMOS devices are used in power-switching applications. The technology required to convert a depletion mode device into an enhancement mode is critical and costly [32, 40–42]. The important parameter for RF studies is G_M, C_{GS}, C_{DS} and f_T. G_M affects the gain, frequency response, stability, and R_0 of the circuit. A transistor with a higher G_M value will have a higher gain and be able to control a large amount of current with a small change in input voltage. The G_M of the device is shown in Fig. 2.8(a). It increases with V_{GS} till saturation, after which it starts decreasing slightly, the reasons for which are as follows. With an increase in the V_{GS}, the channel resistance decreases with the increase in the free carrier's density and therefore current and hence increases until it attains a saturated value.

For a fixed V_{DS}, I_{DS} and hence G_M increases, with an increase R_{dose} as aforementioned. Moreover, as V_{DS} increases after saturation at a particular value of V_{GS}, the R_{DS} also increases with an increased V_{DS}voltage, which eventually reduces the G_M. C_{GS} and C_{GD} (parasitic capacitances) perform low-pass filters to reduce the switching speed. They also tend to increase the switching losses, thus restraining the maximum operation frequency [43]. C_{GS} may affect the input impedance of the MOSFET, which decorates the stability and performance in circuits using these devices as an amplifier or switching devices. As shown in Fig. 2.8(b), with V_{GS} increase C_{GS} first decreases and then increases. C_{GS} has mainly two components, oxide capacitance (C_{ox}), and depletion capacitance (C_{dep}). At lower V_{GS}, C_{dep} is larger due to the thick depletion of carriers. With an increase in V_{GS}, depletion width diminishes to a value such that C_{dep} is lowest, and does not affect on C_{GS}. Thereafter, C_{ox} dominates the C_{GS}, and increases with V_{GS}. With an increase in V_{GS}, C_{GD} increases, due to increased free mobile carriers in the channel (Fig. 2.8(c)). The f_T of the device (shown in Fig. 2.8(d)) signifies the frequency at which the gain of a circuit, such as an amplifier or filter, decreases to unity or 0 db. In other words, at this frequency, the circuit passes the signal unchanged rather than amplifying it. f_T can be expressed as $G_m/2\pi(C_{GS} + C_{GD})$. Therefore, higher value of G_M and lower values of C_{GS} and C_{GD} enhance the f_T for the aforementioned reasons. The accuracy of the simulations at higher voltages and temperatures is supported by validated physical models within the TCAD tool, which accurately predict device behavior over a broad range of conditions. While these models were calibrated at lower

values, their extension to high-voltage and high-temperature conditions is based on well-established physical principles. Future experimental validation is recommended to further ensure the accuracy of these high-condition simulations.

2.5.4 High-Temperature Performance of LDMOS Transistor at Radiation Environment

With the proposed Temperature and radiation exposure have a major impact on the transfer characteristics of a LDMOS transistor. Elevated carrier mobility improves conductivity at higher temperatures, which may result in changed V_{TH} behavior [44–47]. On the other hand, complications arise when one is exposed to a radiation dose (given 1MRad). Defects in the semiconductor material caused by radiation-induced electron-hole pairs result in changes in V_{TH}, an increase in leakage currents because of oxide charges and interface traps, and a decrease in G_M. Complex alterations in the transistor's

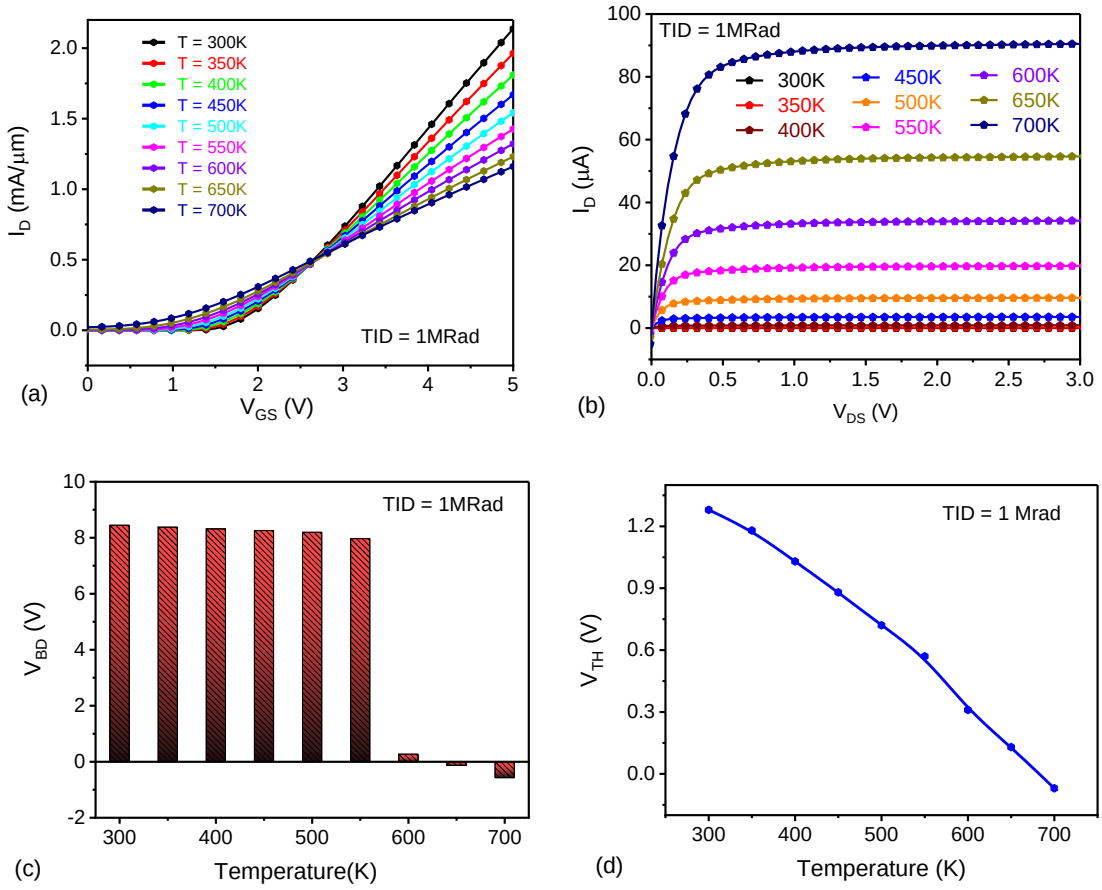

Fig. 2.9: (a) Transfer characteristics (b) f_T (c) V_{BD} (d) V_{TH} of LDMOS with Temperature at Radiation dose 1MRad.

transfer characteristics are the outcome of these combined actions, which are impacted by the particular device design and semiconductor characteristics. Comprehending these

fundamental principles is imperative in the development of radiation-resistant and stable-performing LDMOS transistors, which are vital for use in extreme radiation-filled settings such as space. Fig. 2.9(a) and 2.9(b), illustrates the transfer and output characteristics of the devices at temperature from 300K to 700K. Our work is significantly enhanced by the inclusion of a model that appropriately accounts for temperature changes caused by radiation exposure. The other significant factors like V_{BD} and V_{TH} affected by temperature deterioration are skilfully depicted in Fig. 2.9(c) and 2.9(d), especially at a TID of 1 Mrad. This thorough analysis greatly improves our understanding of how radiation stress affects LDMOS behavior. These insights provide a greater understanding of the functionality and stability of LDMOS devices in harsh settings, which is crucial for evaluating their performance.

Transistor conduction begins when the V_{TH} forms the inversion channel between the drain and source. It is defined by the peak of the acceptor impurity concentration, N_{max}, which is usually located in the LDMOS device's conduction channel. Comprehending this crucial characteristic is vital for enhancing device functionality and creating effective electrical circuit designs. N_{max} controls V_{TH} in LDMOS transistors, which affects how the device behaves and functions as a whole. The correlation between V_{TH} and N_{max} is essential for describing the behavior of LDMOS and creating durable semiconductor devices which is expressed as [48, 49]:

$$V_{TH}(T) = \emptyset_{ms} + 2\emptyset_f + \frac{\sqrt{2 \in q N_{max}(x)(2\emptyset_f)}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \tag{2.12}$$

The primary source of temperature dependency in equation (2.12) arises from the Fermi potential, expressed as:

$$\emptyset_f = \frac{kT}{q} ln\left(\frac{N(x)}{n_i(T)}\right) \tag{2.13}$$

The V_{TH}, is an electrical characteristic influenced by temperature. In these equations, ϕ_f represents the Fermi potential, ϕ_{ms} denotes the difference in work function between the metal and the semiconductor, ε is the dielectric constant of silicon, kT/q is the thermal voltage, and n_i stands for the intrinsic carrier concentration. The temperature dependency of n_i (intrinsic carrier concentration) is described as:

$$n_i(T) = 3.87 \times 10^{16} T^{3/2} e^{-E_g/2kT} \quad (2.14)$$

The trend of the temperature-dependent fluctuation of the DMOS V_{TH} can be obtained by combining equations (2.12) to (2.14) and taking their derivative.

$$\frac{dV_{TH}}{dT} = \left[\frac{\emptyset_f}{T} - \frac{K}{q}\left(\frac{E_g}{2KT} + \frac{3}{2}\right)\right]\left(2 + \frac{\sqrt{2 \in q N_{max} 2\emptyset_f}}{2\emptyset_f C_{ox}}\right) \quad (2.15)$$

Fig. 2.9(d) illustrates the relationship between the V_{TH} and the technological and physical factors of LDMOS. It shows that V_{TH} decreases with rising temperature. This change can be expressed using the following expression, shows a linear link with temperature:

$$V_{TH}(T) = V_{T0} + (V_{tT} T_j) \quad (2.16)$$

The equation coefficient is represented by $V_{TH}(T)$, the junction temperature is shown by T_j, the ambient temperature is represented by T_0, and the V_{TH} at this ambient temperature is indicated by V_{T0}. A typical n-channel LDMOS device's observed V_{TH} is shown in Figure 1.9(d) for a temperature range of 300K to 700K. As the temperature increases, the V_{TH} exhibits a linear progression, but it lowers. Temperature tends to increase total gate capacitance, since greater temperatures induce charge carriers in semiconductor material to become more mobile, which raises capacitance. The semiconductor characteristics are also impacted by exposure to 1 MRad radiation, which adds to the overall rise in C_{GG} shown in Fig. 2.10(a). The transistor's performance and speed of switching are affected by this rise in capacitance, which influences circuit design and reliability evaluation in radiation-prone locations.

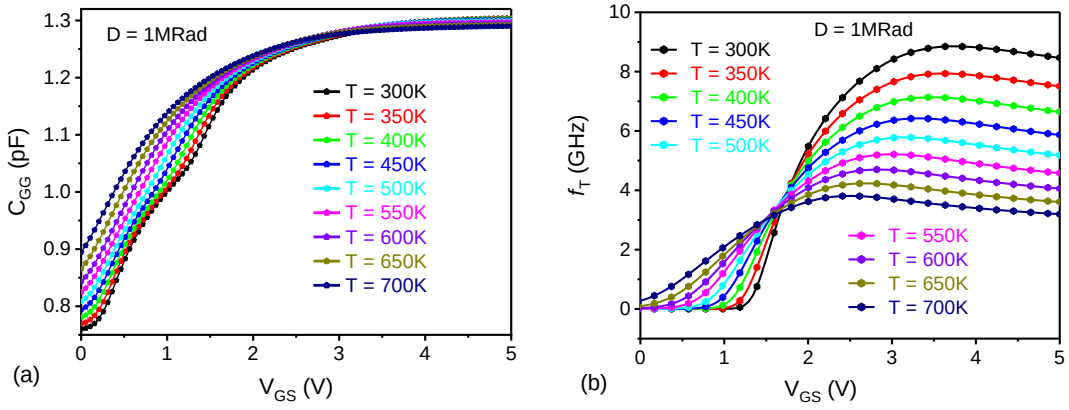

Fig. 2.10: (a) Total Gate Capacitance (C_{GG}) (b) f_T at $V_{DS} = 1\text{V}, \text{D} = 1\text{MRad}$ with temperature.

However, a transistor's f_T, which represents its high-frequency performance, tends to diminish in response to radiation and temperature. The f_T is calculated from the G_M and C_{GG} of the device from the relation $f_T = G_M/2\pi C_{GG}$. Radiation-induced flaws in the semiconductor material led to a drop in transistor performance in G_M, with temperature which is derived from transfer characteristics. Furthermore, carrier mobility falls with temperature, which lowers the transistors f_T even more as shown in Fig. 2.10(b). The transistor's capacity to handle high-frequency signals efficiently is impacted by this drop in f_T, which is significant in several applications.

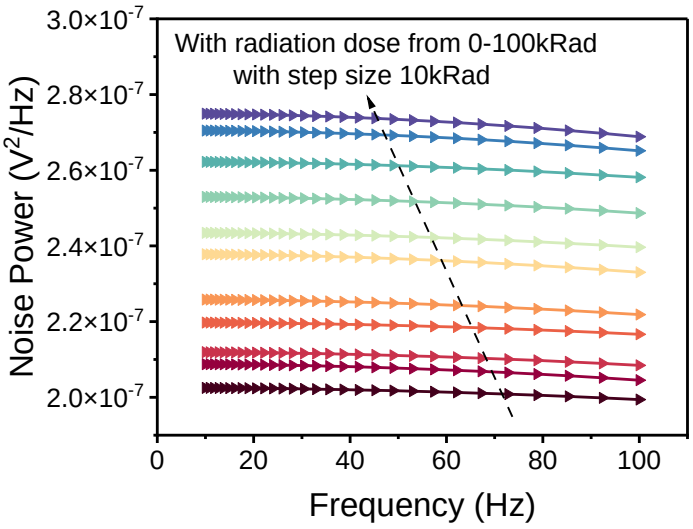

Fig. 2.11: Low-frequency noise density with TID at $T_{OX} = 20$ nm, $L_{ch} = 300$ nm and $L_{drift} = 350$ nm and $V_{GS} = V_{DS} = 1$ V.

2.6 Low-Frequency Noise ($1/f$) Calculation of LDMOD Transistor with Total Ionizing Dose (TID)

With the proposed in electronic devices, often noise originates from a variety of sources, including thermal noise, shot noise, flicker noise, etc. varying on devices and operating conditions. Shielding, filtering, noise-reducing components, etc., are some of the commonly used techniques to reduce noise. When the MOSFET is exposed to radiation, several noise events are encountered such as single event upsets (SEUs), single event latch-up (SEL), Total ionizing dose (TID) effects, Single event burnout (SEB), etc. [41], which may temporarily or permanently damage the device, depending on how it is exposed to radiation. In this work, the LDMOS is exposed to gamma radiation and we have studied the total ionizing dose (TID) effects for understanding the reliability, performance, and radiation tolerance of the device. With radiation, charges are trapped at the interface of the oxide and silicon surface, which may increase the $1/f$

noise, whose spectral density is inversely proportional to the frequency of the signal. At lower frequencies, the fluctuations happen slowly, and the noise power is concentrated at lower frequencies, resulting in a higher level of noise power at each frequency, therefore, flicker noise is very relevant to this device under radiation. The low frequency (LF) noise power behaviour with R_{dose} from 0-100kRad is shown in Fig. 2.11.

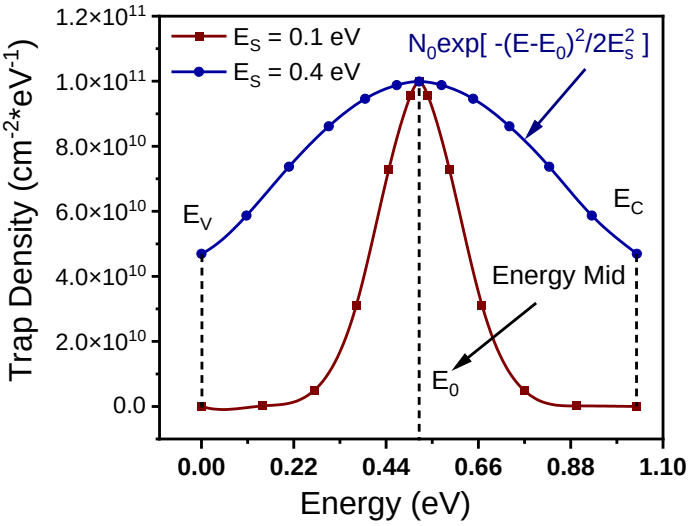

Fig. 2.12: Gaussian distribution of traps in the oxide/semiconductor interface.

Noise power indicates the total amount of power contained in the noise signal in an electronic system. For better circuit performances, the lower noise power is desirable. With an increase in R_{dose}, the noise power increases. This is because, radiation-induced charge carriers can add to the existing carriers and increase the fluctuation rate of the noise, subsequently increasing the flicker noise power. The $1/f$ noise in an LDMOS in presence of radiation may be represented as follows [50]:

$$S(f) = \frac{K}{f^{\gamma}} \frac{V_{DS}^2}{(V_{GS}-V_{TH})^2} \tag{2.17}$$

Where, $S(f)$ is the power spectral density of the noise, f is the frequency, and γ is a parameter that describes the noise spectrum. K is the device-dependent noise level which can be calculated by device dimensions, elementary charge, and trap charges [51]. Also, as expected, the noise power decreases with increased frequency. At a lower frequency, the slow random variations in the resistances by trapping or releasing of electrons arise over a longer period and therefore, the noise power is more. Also, at higher frequencies, the parasitic capacitances may be dominant, weakening

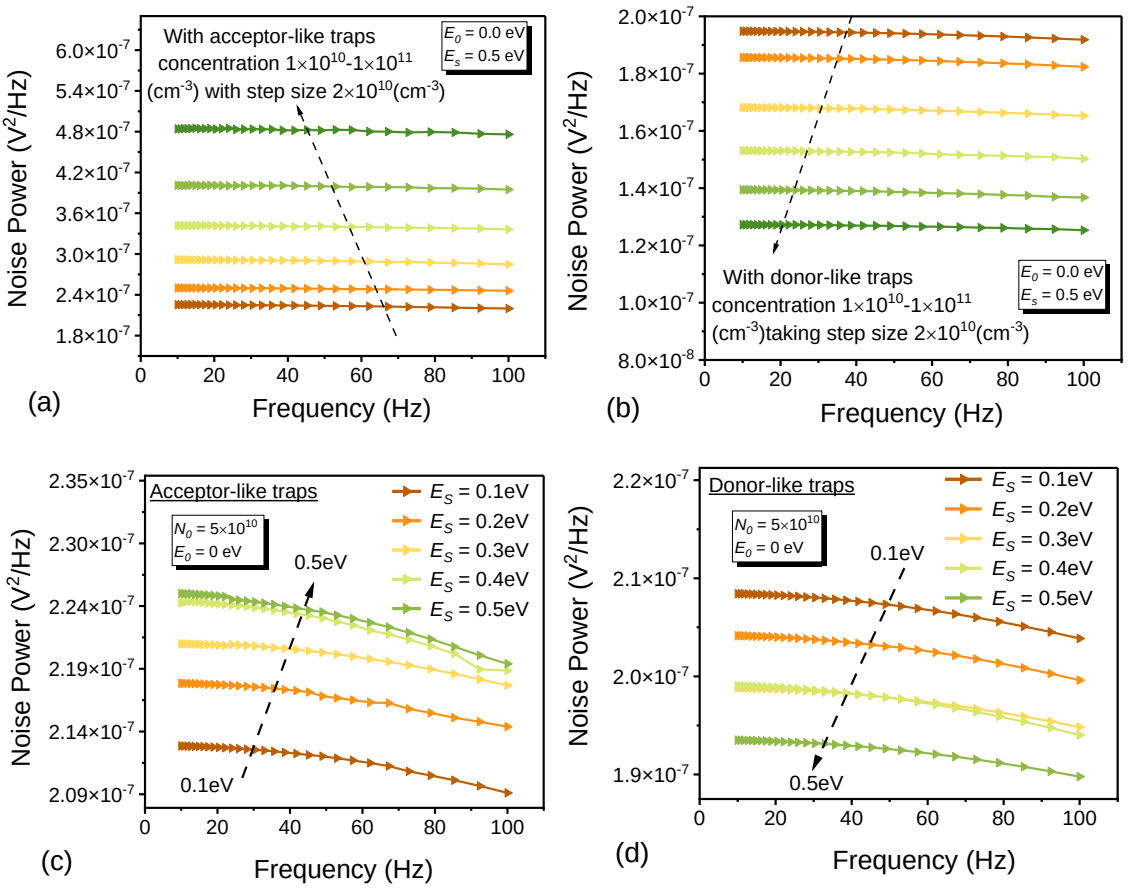

Fig. 2.13: Low-frequency noise with (a) acceptor-like trapping concentration (b) donor-like trapping concentration and with "energy sig" at the interface of oxide/channel region for (c) acceptor-like trap (d) donor-like trap at $T_{OX} = 20$ nm, $L_{ch} = 300$ nm and $L_{drift} = 350$ nm and $V_{GS} = V_{DS} = 1$ V.

high-frequency noise components. In conclusion, as a result of radiation exposure, atoms move around in the crystal lattice, resulting in displacement damage. This leads to structural flaws and traps in the device influences the LF noise to negatively impact its electrical performance of the LDMOS [52]. Fig. 2.12 shows the variation of noise power with a width of the Gaussian potential, E_S. The width of the Gaussian potential function defines the properties of the traps and hence the flicker noise power. A wider Gaussian potential function corresponds to a larger spread of energy levels. This implies that there are more traps with energy levels closer to the device's Fermi level, which eventually, leads to more EHP being generated and hence increased current fluctuations. Therefore, acceptor-like flicker noise power increases with E_S for a fixed value of energy mid (E_0).The acceptor-like traps at the interface, increase the number of defects in the semiconductor and therefore, the noise power is increased as shown in Fig. 2.13(a).

In addition, acceptor-like traps enhance the depletion of carriers in the channel region, which increases resistance and eventually increases the flicker noise power. Also, acceptor-like traps may temper the carrier mobility which may fluctuate the voltages and current of the device, eventually increasing the noise power. However, the distribution and concentration of traps, for a given material and operating condition, will take an important role in the determination of noise power. Similarly, the noise power dependence on donor-like traps as shown in Fig. 2.13(b) can be explained. The impact of traps on device performance is often described by the Gaussian potential fluctuation model, with the assumption that the trap energy levels are spread according to a Gaussian probability distribution function with a certain width [53]. The LDMOS is mostly affected by trapping concentration at the Si/SiO_2 interface under R_{dose}.

The noise power with frequency for both acceptor and donor-like traps at the interface of oxide/silicon with 'concentration' is shown in Fig. 2.13(a) and Fig. 2.13(b) and with 'energy sig' in Fig. 2.13(c) and Fig. 2.13(d) respectively. 'Energy sig' (E_S) refer to parameters that specify the shape of the trap potential in the context of a Gaussian-like trap which represents how quickly the potential energy grows as one moves out from the trap's center as shown in Fig. 2.12. The probability of finding a trap with energy level E within an energy range ΔE, around E_S is given by the following relation [50]

$$P(E) = \frac{1}{E_S\sqrt{2\pi}} e^{\frac{(E-E_0)^2}{2E_S^2}} \tag{2.18}$$

"Energy mid" (E_0), defines the position at the center of the trap potential with minimum potential energy. Therefore, E_0 is the value in the x-axis that corresponds to the maximum amplitude of the Gaussian potential function (Fig. 2.12). With an increase in the values of E_S, the probability of finding a trap decreases. Therefore, obviously, E_S manipulate the low-frequency noise power as well. The low-frequency noise power spectral density, $S(f)$ change with the distribution of traps is given by Hooge's empirical relation [39].

$$S(f) = 2q^2 N_0 W f \left(\frac{1}{1+2\pi f\tau^{\alpha}}\right) \tag{2.19}$$

Where, N_0 is trap density, W - device area, q-electronic charge, τ- carrier lifetime, α-parameter that describes the behavior of the noise at low frequencies, and f- frequency.

In equation (2.19), the term ($1 \,/\, 1 + 2\pi f\tau^{\alpha} \cong 1$) at low-frequency. Even though, the relationship between the probability of finding a trap and noise power may depend on many factors [40]. N_{it} may create additional energy states within the bandgap, which can further affect the conductivity of the device [54]. In conclusion, the low-frequency noise power in an LDMOS can be studied by the Gaussian distribution of N_{it}. E_0 and E_S maybe modulated a bit to keep the noise power at a desired value under radiation.

In conclusion, acceptor-like traps are uncharged when unoccupied, and they carry the charge of one electron when fully occupied [55]. With an increase in acceptor-like traps concentration, the noise power increases as effective mobile charges increases with trap occupancy near the channel region and the device becomes noisier. Donor-like traps are uncharged when unoccupied, and they carry the charge of one hole when fully occupied and therefore, effective conduction charges decrease for n-channel LDMOS, resulting in a decrease in the noise power. With the majority of the traps gathered tightly around a mean energy value, a smaller "Energy Sig" value indicates a narrower dispersion of trap energy levels. In contrast, a higher "Energy Sig" value denotes a wider distribution with more evenly distributed trap energy levels. Because it describes the variability or range of trap energy levels within the device, the Energy Sig parameter is important. It has an impact on phenomena connected to traps, including charge capture/release operations, trap occupancy etc. Different trap properties, such as carrier transport, threshold voltage shifts, or leakage currents, may affects on device performance explored by changing the "Energy Sig" parameter.

2.7 Threshold Voltage Modulation in The Presence of TID

When designing LDMOS devices, especially for power amplifier applications, threshold voltage modulation is a crucial factor to take into account. From the above discussions, it is clear that there is a V_{TH} change with TID. While working in a TID environment, may require maintaining a particular V_{TH}. A properly modulated threshold voltage can help increase the device's linearity, gain, and efficiency. Here are some techniques to modulate the V_{TH}.

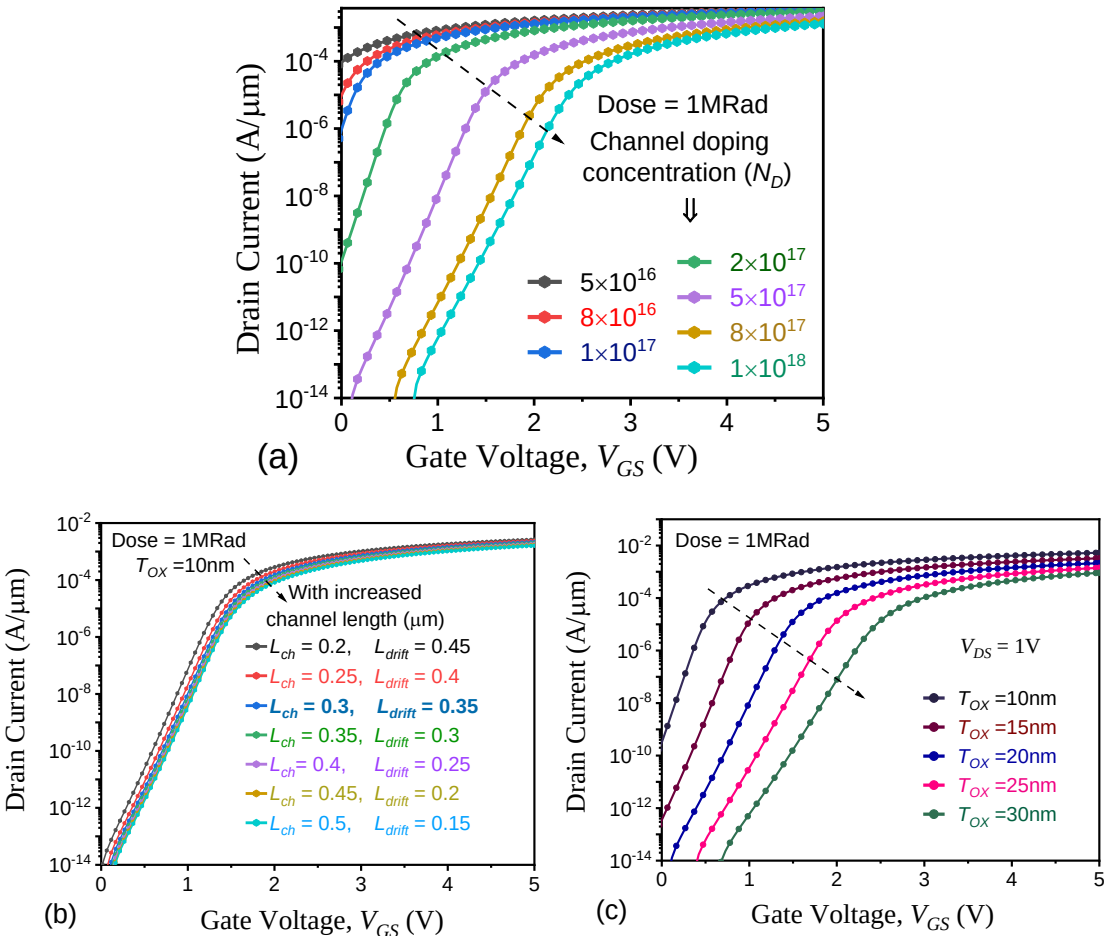

Fig. 2.14: Transfer characteristics at 1Mrad of radiation dose (a) with channel doping concentration at $T_{OX} = 20$ nm, $L_{ch} = 300$ nm and $L_{drift} = 350$ nm (b) with channel length and drift length at $T_{OX} = 20$ nm (c) with oxide thickness at $T_{OX} = 20$ nm, $L_{ch} = 300$ nm, $L_{drift} = 350$ nm and $V_{DS} = 1$ V.

2.7.1 With Channel Doping Concentration

As shown in Fig. 2.14(a), the threshold voltage (V_{TH}) increases with an increase in the channel doping concentration (N_D). A higher N_D leads to a stronger electric field in the channel, causing a larger depletion region. This increase in depletion width requires a higher gate voltage to invert the channel, thereby raising V_{TH}.

Additionally, with TID radiation exposure, more fixed charges are generated in the oxide region. These fixed charges shift the band alignment, further increasing V_{TH}. The combined effect of higher N_D and TID-induced oxide charges results in a significant rise in threshold voltage, which is critical to understanding the device's behavior under radiation and high doping conditions.

2.7.2 With Channel/Drift Length Variation

It is also possible to tune the threshold voltage by changing the length of the channel region and drift region as shown in Fig. 2.14(b). V_{TH} is lesser for an LDMOS with $L_{ch} > L_{drift}$ than an LDMOS with $L_{ch} < L_{drift}$ with TID. When a high voltage is applied across the LDMOS, the electric field in the drift region increases. To prevent this, the drift length is kept longer which increases the depletion and therefore V_{TH} increases. Therefore, V_{TH} can be modulated with a change in the values of L_{ch} and L_{drift} under TID.

2.7.3 With Oxide Thickness Variation

The threshold voltage can also be modulated by the T_{ox} with TID. A thinner oxide offers a higher capacitance per unit area and oxide charge resulting in a lower value of V_{TH} as $V_{TH} \propto C_{ox}^{-1}$ as shown in Fig. 2.14(c). Therefore, to maintain the V_{TH} at a fixed value, T_{ox} may be adjusted slightly during fabrication. TID creates positive charges in the gate oxide, which may increase the V_{TH}. As higher T_{ox} has a higher density of traps, the possibility of an increase in V_{TH} also increases with an increase in oxide thickness.

2.7.4 Inserting a P^+pocket in The Channel Region

Inserting a P^+pocket (Fig. 2.15(a)) in the channel region can change the V_{TH}. In an LDMOS, a pocket is used to reduce the higher electric fields and hence advance the breakdown voltage of the LDMOS. The length and doping concentration of the pocket modulate the V_{TH}. With an increase in the value of pocket length, V_{TH} increases as shown in Fig. 2.15(b). It can be interpreted as follows. With increased pocket length, the electric field reduces; in other words, gate controllability increases, and a higher gate voltage is required to turn on the LDMOS. For a similar reason, with an increase in the pocket doping concentration, the V_{TH} increases as shown in Fig. 2.15(c). Which describe, with increased pocket length, the electric field near the channel is reduced, which stabilizes the channel and increases gate controllability. However, this also means that the threshold voltage (V_{TH}) is higher because the channel formation is more controlled and requires a higher gate voltage to overcome the stabilized electric field and turn on the device. This doesn't contradict the improved gate controllability but reflects the need for a higher voltage to achieve channel inversion.

2.8 Analog Circuit Performance of LDMOS Transistor

Typically, two LDMOS transistors connected in series form a complementary metal-oxide-semiconductor (CMOS) configuration in an inverter circuit that uses LDMOS transistors shown in Fig. 2.16(a). Two LDMOS transistors are used; one is a pull-up and

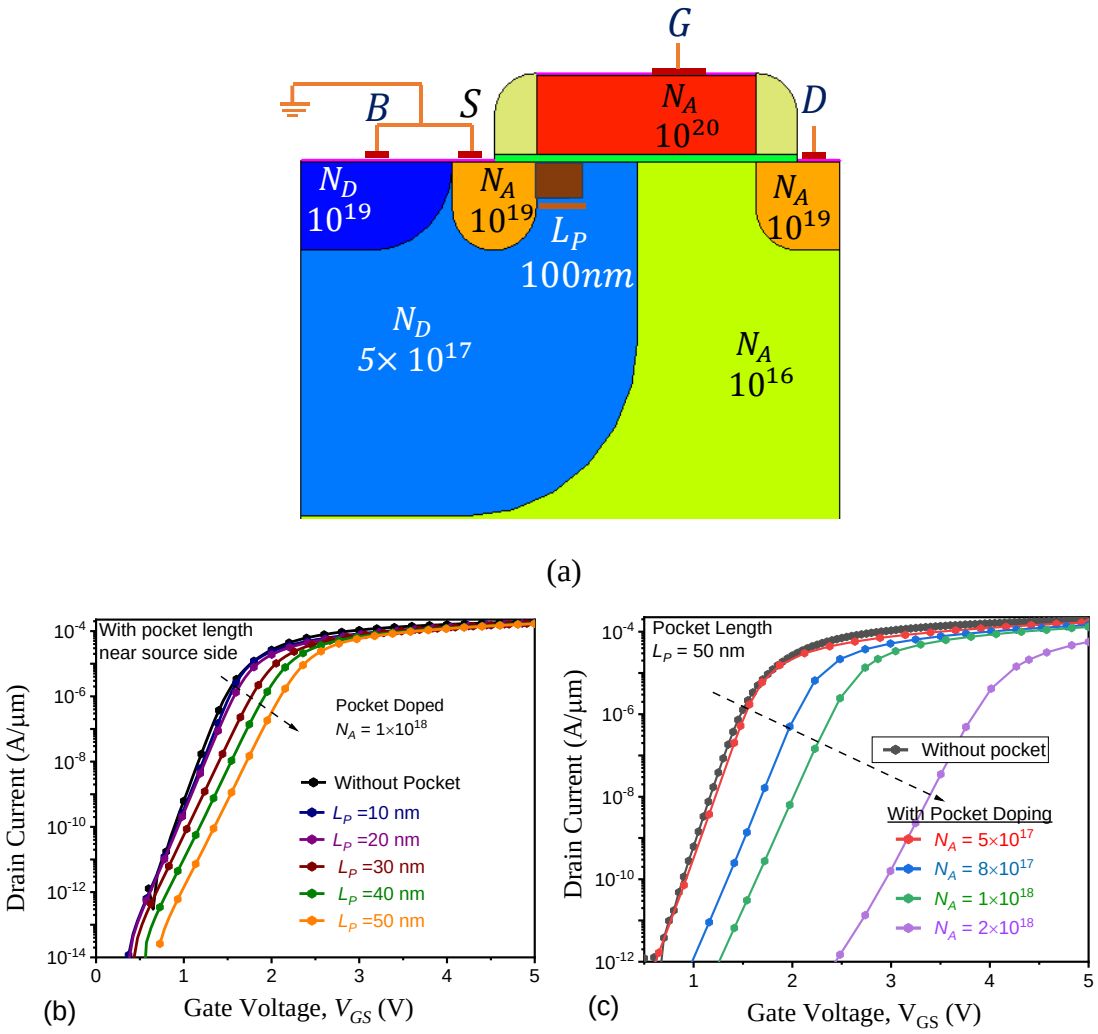

Fig. 2.15: (a) Schematic of LDMOS with the P^+ pocket region, (b) transfer characteristics with different pocket lengths, and (c) transfer characteristics with pocket doping concentration inside the channel near the source at $T_{OX} = 20$ nm, $L_{ch} = 300$nm, $L_{drift} = 350$ nm, $V_{DS} = 50$ mV and radiation dose = 1Mrad.

the other a pull-down device. Whereas the pull-down transistor is linked between the output node and ground, the pull-up transistor is connected between the output node and the supply voltage (V_{dd}). Both transistors' gate terminals receive the input signal [56–58]. The pull-down transistor pulls the output node to ground when the input signal is low and the pull-up transistor is off. Alternately, the pull-down and pull-up transistors pull the output node to V_{dd} and on, respectively, when the input signal is high.

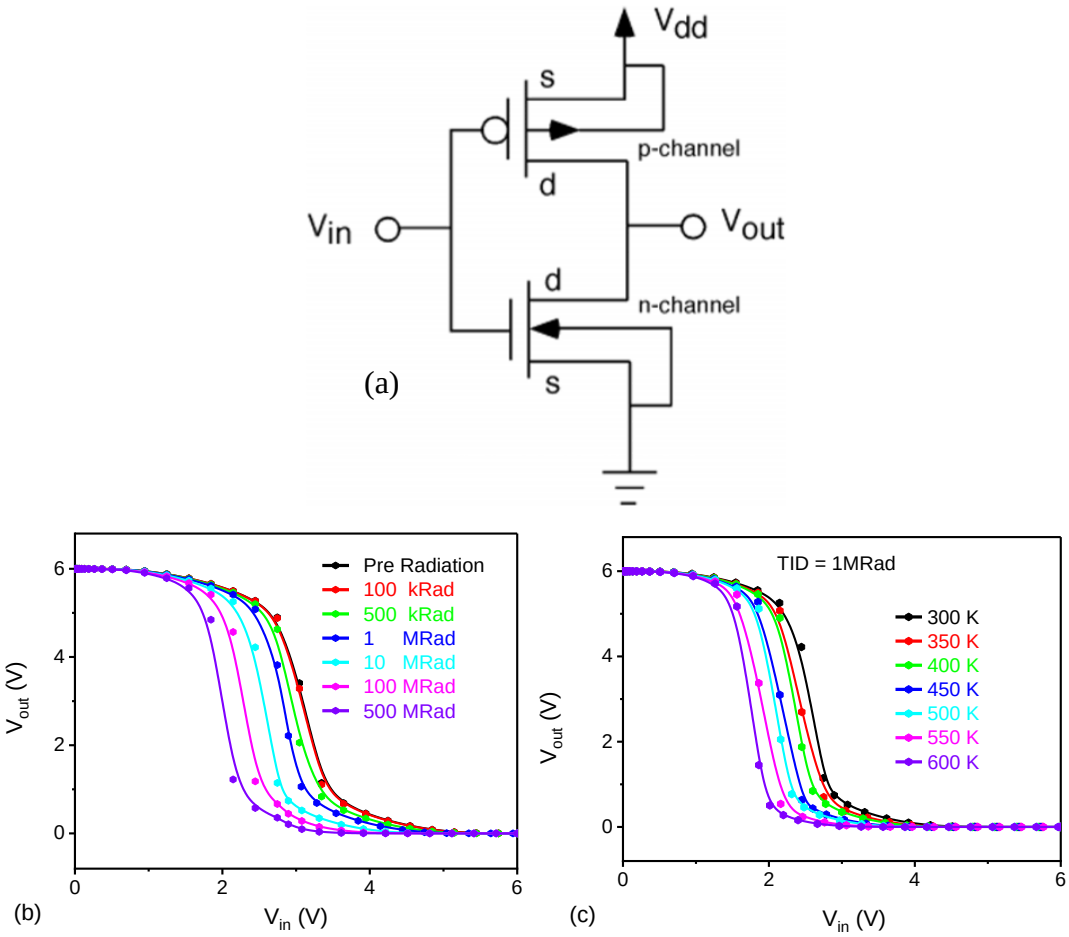

Fig. 2.16: (a) Circuit diagram of CMOS inverter using LDMOS (b) Voltage transfer characteristics with TID and (c) Voltage transfer characteristics with temperature.

Radiation exposure causes changes in the voltage transfer characteristics of an inverter circuit using LDMOS transistors because of influences on the transistor's V_{TH} and leakage currents. Exposure to radiation causes flaws in LDMOS transistors, which alter the V_{TH} and increase leakage currents. As a result, OFF-state current of the COMS increases more with radiation, changes are made to the transfer characteristics, which explain the connection between the inverter circuit's voltage transfer characteristics shown in Fig. 2.16 (b). In particular, the transition zone between the high and low output voltage states is influenced by the V_{TH} shift, which also has an impact on the transistors switching behavior. Increased leakage currents also contribute to variations in output voltage levels, which have an impact on the inverter circuit's overall performance. CMOS devices are susceptible to considerable temperature variations in their characteristics. Many important CMOS transistor characteristics, including carrier

mobility and V_{TH} vary with temperature. These differences change in transistor properties, which would impact the dependability and efficiency of the circuit. Furthermore, changes in temperature effects on the integrity of gate oxide layers, which in turn can compromise the dependability of CMOS devices shown in Fig. 2.16(c). Elevated temperatures have the potential to hasten the formation of defects in the gate oxide, hence increasing leakage currents and eventually causing device failure at higher temperature.

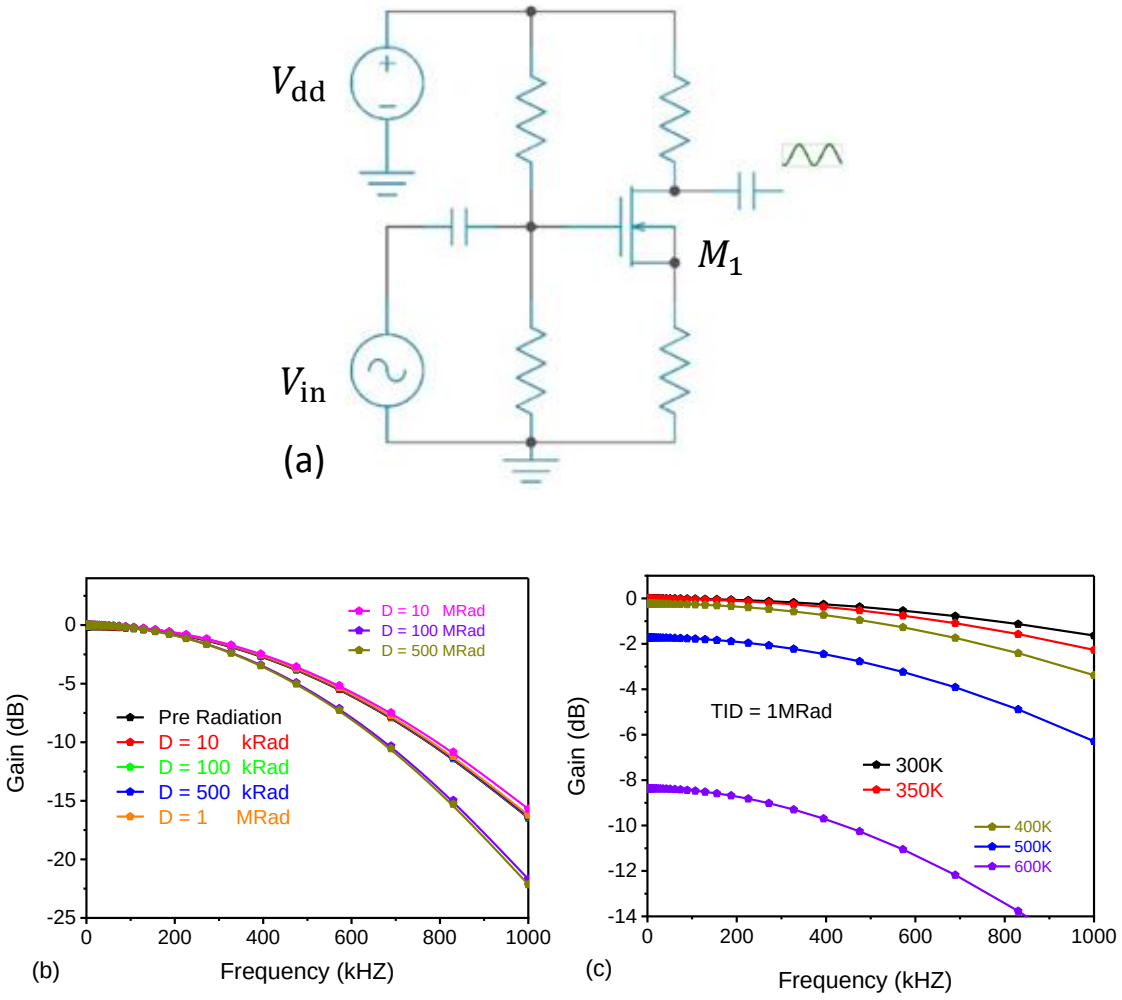

Fig. 2.17: (a) Circuit diagram of single-stage amplifier using LDMOS (b) Output characteristics with TID (c) Output characteristics with temperature.

By applying an input signal to the gate terminal of the LDMOS transistor, which modifies the drain current flowing through the transistor dependent on the input voltage, a single-stage amplifier circuit is created shown in Fig. 2.17(a). Next, the load resistor linked between the supply voltage and the drain terminal is used to determine the output

voltage across it. The circuit amplifies the input signal by suitably biasing the LDMOS transistor, yielding a gain that is dictated by the load resistor and the G_M of the transistor.

A gain vs. frequency plot for a single-stage amplifier with an LDMOS transistor usually shows that the gain drops with increasing input signal frequency. A number of variables contribute to this decrease in gain, such as parasitic capacitances in the transistor and surrounding circuitry and intrinsic transistor features like its unity-gain bandwidth (f_T) [59]. Because the transistor is operating in its linear area at low frequencies, the gain is comparatively constant and high. But as the frequency increases, the gain decreases as the effects of parasitic capacitances become more noticeable shown in Fig. 2.17. The gain eventually reaches a point when it abruptly decreases, signifying the amplifier's top bandwidth limit. It is common to refer to this point as f_T.

2.9 Summary

We have extensively done a simulation study to understand the analog performance of the device such as V_{TH}, G_M, R_0, f_T and $1/f$ noise performance with TID after calibration with a fabricated device. EHP generation increases with TID, which shifts the V_{TH} towards lower value and degrades I_{ON}/I_{OFF}. I_{output} increases with TID and correspondingly R_0 decreases. G_M and f_T increase (up to V_{GS} of ~2V) and decrease respectively. As expected, the $1/f$ noise power density is sensitive to TID. The noise power can be adjusted by energy-mid and energy-sig parameters. We have discussed, a few methods to modulate the V_{TH} of the LDMOS under TID namely channel doping concentration, channel length modulation, oxide thickness variation, and pocket-doped methodology.

Our research indicates that the combined effects of radiation and temperature greatly worsen LDMOS circuit deterioration, highlighting the need for improved resilience in electronic devices that are subjected to harsh environmental conditions. By utilizing sophisticated circuit simulation techniques along with actual data, we have been able to offer important insights into how much performance declines under different conditions. The voltage transfer characteristics of an inverter circuit are impacted by radiation exposure because it modifies the properties of LDMOS transistors, shifting V_{TH} and boosting leakage currents. Variations in temperature within CMOS devices also impact important transistor properties, which in turn impact circuit efficiency and dependability. The amplifier maintains a high and relatively constant

gain when operating in its linear range at lower frequencies. However, as the frequency increases, parasitic capacitance effects become more noticeable, causing a gradual decrease in gain until it reaches a cut-off frequency, where the gain abruptly drops, designating the amplifier's bandwidth limit. We advise the use of efficient mitigation strategies to overcome these issues and improve the dependability of LDMOS circuits in radiation-intensive and hot environments. These include using radiation-hardened design techniques and implementing strict temperature control strategies. Engineers and designers working on mission-critical applications, like aircraft systems and satellite communication, can increase the robustness and lifespan of electronic devices using LDMOS analog circuits by implementing these techniques. This research advances our understanding of the complex interactions between temperature, radiation, and circuit performance, which will help design durable and effective electronic devices that can resist a variety of harsh environmental conditions. In general, experts looking to optimize LDMOS circuits for improved performance and dependability in practical applications will find this study to be a useful resource. Comprehensive validation across multiple devices, including circuit-level evaluations, is necessary before making such a recommendation for industrial adoption. However, we performed circuit analysis, including inverter and boost converter simulations, using n-LDMOS and p-LDMOS devices to further validate the technology's potential at the circuit level.

The study executed here will help circuit designers for setting a guideline for the optimization of performances, reliability, and efficiency for high power and breakdown applications under TID and noise environment. This is in addition that the explored LDMOS offers better HCD behavior as was experimentally verified by Mahajan et al, [27, 28] which is a kind of a downside in many reported LDMOS devices. The breakdown voltage of the LDMOS transistor here is ~9-15 V. These types of LDMOS are applicable for medium voltage applications such as in vehicles, drones, and medical applications.

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