CHAPTER 3

Double Gate Junctionless FET with SiC substrate

Contents

3.1. Introduction

As heralded by the IEEE International Roadmap for Devices and Systems (IRDS), the low-power semiconductor industry continuously strives to increase performance by packing more and more transistors in a single chip [1]. On the other hand, the high-power or power electronics industry aims toward higher power capacity for their chips. However, Silicon still holds the significant market share for high-voltage and low-power transistors. This is because of its excellent interface quality with SiO_2, low-cost substrate, mature processing technology, and decades of research and development. In the low-power electronics market, the dimension of the traditional transistors approached physical limits (in terms of gate control, output current, capacitance, power/performance ratio, etc.) as they were scaled down, and performance and reliability suffered. The industry has since moved to non-planar fully depleted (FD) multi-gate MOSFETs (MugFETs) such as FinFETs, for sub 20 nm ultra-large-scale integration (ULSI) applications, allowing dimensional scaling and higher reliability, thus manufacturing integrated circuits with higher packing density and better performance [2, 3]. Although such a transistor has great performance metrics, it has abrupt source and drain junctions, which poses fabrication complexities in doping profiles, thus preventing further scaling down, or intricate integration with other CMOS technologies. Junctionless transistors (JLT), on the other hand, have homogeneous and uniform doping profiles. Combining this advantage along with many others (better short channel control, negative bias thermal instability, lesser random telegraph-noise and $1/f$ noise, low thermal budgets, etc.) depicts the potential of JLTs as a better fit for memory applications, IoT technology, etc. than FD MOSFETs [4–7]. Despite these advantages, a JLT isn't commercialized yet for daily life applications, because of relatively intricate fabrication techniques (e.g., ~5-10 nm substrate thickness with uniform, high doping) and some electrical performance constraints (e.g., inferior transconductance compared to IM MOSFETs). However, if tremendous performance advantages can be forecasted, these fabrication-related challenges and low drain current can be met over time, just like in the case of FinFETs.

The double-gate junctionless field-effect transistor (DG-JLT) on silicon carbide (SiC) substrate is a promising development in semiconductor technology for its superior performance and scalability over traditional transistors. SiC substrates offer a number of benefits, such as increased electron mobility and thermal conductivity, which improve

device dependability and efficiency [8, 9]. The transistor's double gate design provides exact electrostatic control over the channel, resulting in improved transistor properties like a high ON-OFF current ratio and a low leakage current.

3.2 Why Junctionless FET?

In 2010, researchers at the Tyndall National Institute, led by Dr. Jean-Pierre Colinge and his team, made a significant breakthrough in semiconductor technology by developing Junctionless Transistors (JLTs) [4]. Unlike in conventional transistor, JLT has no PN junction in source-channel-drain path. This invention represented a break from the conventional method of designing transistors, which relied on doping concentrations (source-channel and channel-drain) within the semiconductor material. Schematic of an n-channel nanowire transistor shown in Fig. 3.1, this seemingly straightforward change produced a device that outperformed conventional MOSFETs in several important ways.

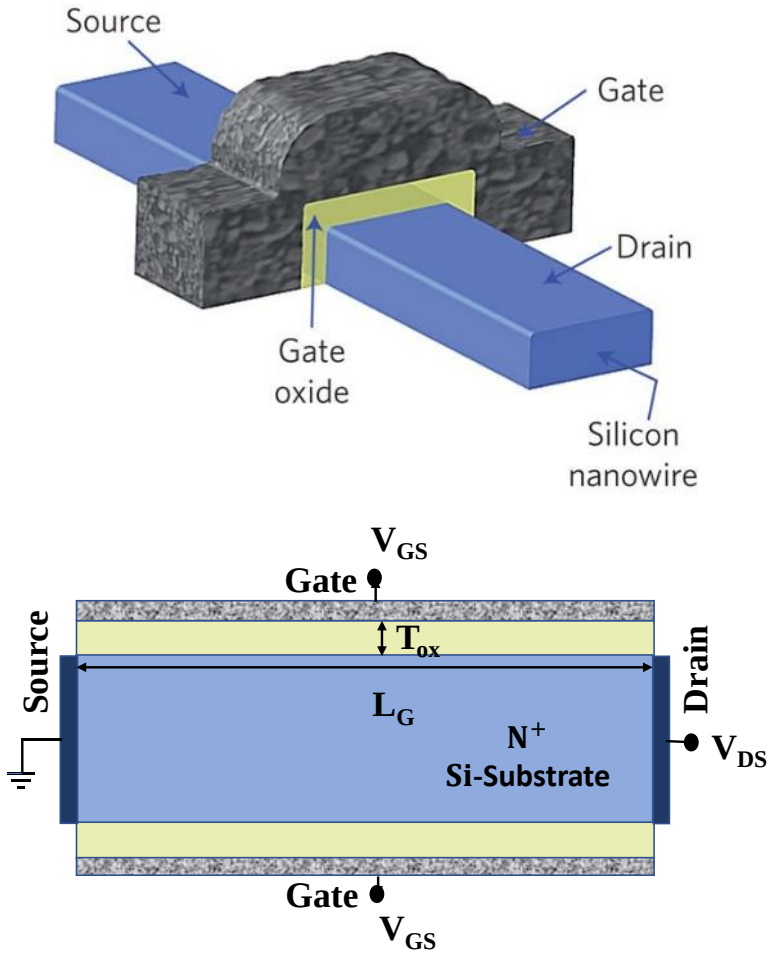

Fig. 3.1: Schematic of an n-channel nanowire transistor [4].

There are numerous important advantages to JLTs not having a PN junction. Firstly, JLTs are more scalable than MOSFETs. The adverse impacts of short-channel effects on MOSFETs cause leakage current problems and performance deterioration as device dimensions decrease. Alternatively, due to the absence of the PN junction and the associated depletion zone in JLTs, they inherently exhibit reduced susceptibility to these effects [10]. This makes it possible to keep shrinking JLTs to some extent and therefore push the limits of miniaturization.

Secondly, the fabrication process is streamlined due to the uniform doping in JLTs (see Fig. 3.2). Unlike MOSFETs, where the creation of PN junctions necessitates precise control over doping concentrations and involves high-temperature diffusion or implantation stages, JLTs achieve PN junction functionality without these requirements. This may result in comparatively cheaper production costs in addition to reducing the complexity of fabrication.

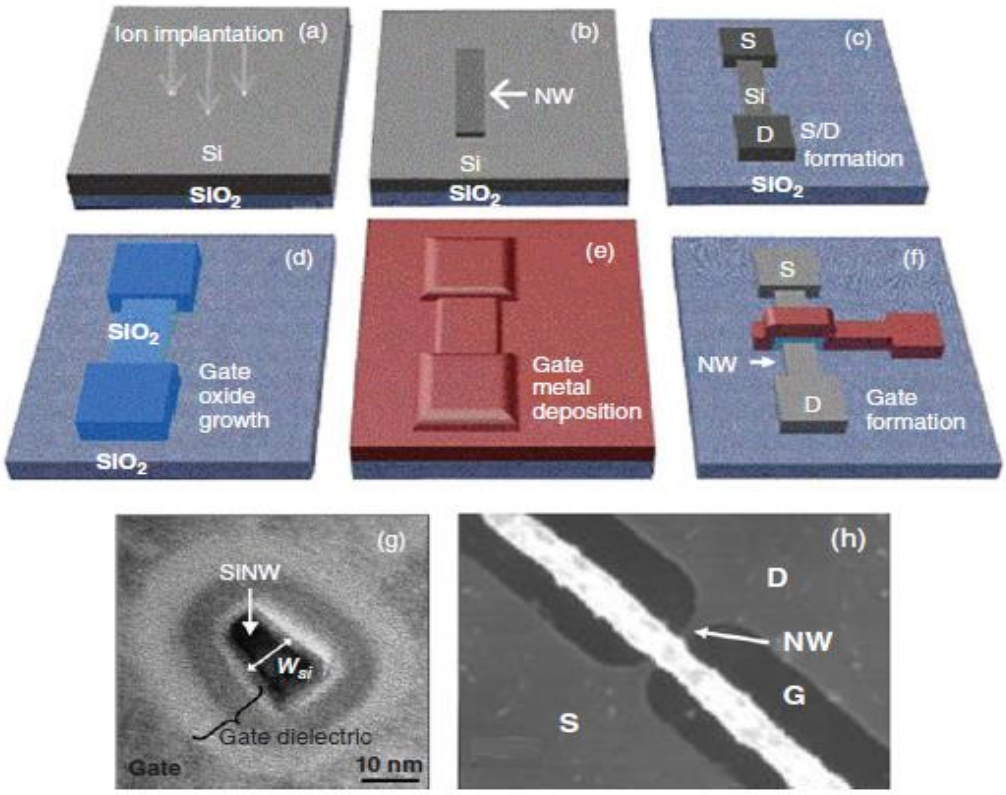

Fig. 3.2: Illustrated Procedure for Fabricating NWJLFETs [11]: (a) ion implantation of SOI film, (b) Defining the nanowire channel, (c) Forming contact pads for the source and drain, (d) Growing or depositing the gate oxide layer, (e) Deposition of the gate metal, (f) Defining the gate electrode [12], (g) Examining the fabricated NWJLFET through a cross-sectional TEM image [13], and (h) Observing the fabricated nanowire metal-oxide-semiconductor field-effect transistor (NWMOSFET) through a bird's-eye SEM image [14].

Thirdly, JLTs have the ability to enhance the functionality of devices. In contrast to MOSFETs, JLTs exhibit volume inversion. Their capability for better I_{ON}/I_{OFF} ratio and lower leakage current makes JLT a better device for lower power application.

In addition, JLTs outperform MOSFETs in terms of resistance to hot carrier effects. Electrons with high energy can break free from their channels and infiltrate the gate oxide, causing damage to the device. This phenomenon is known as hot carriers. JLTs' homogeneous doping profile reduces the production of hot carriers and lesser surface scattering, increasing the longevity and dependability of the device.

3.3 Silicon Carbide (SiC) as Substrate for High-Power Applications

The limitations of Silicon, especially its narrow bandgap, reduced heat conductivity, and decreased electron mobility, limit its usefulness in high-frequency and high-power applications. In contrast, SiC has a much wider bandgap (around 3.2 eV for 4H-SiC), which allows devices to withstand much higher voltages before breaking down [7]. This results in a significant increase in SiC-based DG-JLTs' breakdown voltage, which makes them suitable for use in power electronics applications such as electric car converters and switch-mode power supplies. SiC, as opposed to Si, also has better heat conductivity. Because of their improved capacity to dissipate heat effectively, DG-JLTs can withstand higher power densities without experiencing performance degradation [15]. This is especially useful in high-power switching applications where a considerable amount of heat generation is unavoidable. In terms of electron mobility, SiC performs better than Si, even after controlling temperature and breakdown voltage. A Dual-Gate Silicon Carbide Junctionless Transistor (DG-SiCJLT) channel experiences faster current flow due to SiC's increased electron mobility. Improved device performance results in reduced signal distortion and faster switching rates in high-frequency applications such as microwave circuits and radio frequency (RF) amplifiers [16].

Another strong benefit of SiC is its chemical stability [17]. SiC is extremely resilient in adverse environments, in contrast to Si, which degrades at high temperatures [18]. Because of this feature, DG-SiCJLTs are ideally suited for demanding applications in the aerospace and military industries, where equipment must perform dependably in harsh environments [19].

3.4 DG-SiCJLT: A Symbiosis of Material Excellence and Device Innovation

A DG-JLT's channel experiences faster current flow due to SiC's increased electron mobility. The DG-SiCJLTs' promise is further highlighted by the DG design. A narrow, evenly doped channel section is positioned between two gate electrodes in the core construction of a DG-JLT.

Metals and high-k dielectrics are two examples of the materials that can be used to create these gates. By creating an electric field, applying a voltage to the gates modifies the conductivity of the channel. While a negative voltage builds up charges at the channel surface, increasing current flow, a positive voltage on the gates depletes the channel and decreases current flow [20]. Furthermore, by reducing the impact of short-channel effects, the double-gate design allows DG-SiCJLTs to be scaled up even further for even higher density integration. Numerous benefits arise from the novel DG-JLT architecture in conjunction with the superior material quality of SiC. First of all, DG-SiCJLTs are perfect for high-power switching applications because of their extraordinarily high breakdown voltage. Second, effective heat dissipation is made possible by their greater thermal conductivity, which is essential for high-power density operation. Thirdly, enhanced performance in high-frequency applications and quicker switching speeds are a result of SiC's high electron mobility. Fourth, SiC's chemical stability guarantees dependable performance even in challenging conditions. Ultimately, the DG architecture minimizes short-channel effects, provides steeper subthreshold swing, and allows for better control over current flow, opening the door to further downsizing [21].

3.5 Literature Review on DG-SiCJLT

In recent years, besides Silicon, wide bandgap (WBG) semiconductors, namely, gallium nitride (GaN), (E_g~3.4 eV), silicon carbide (SiC) (E_g~3.3 eV) and $\beta - Ga_2O_3$ (E_g~ 4.5-5.3 eV) have received the limelight because of their high breakdown, high-frequency operation, etc. [18, 22, 23]. SiC exhibits a higher figure-of-merit (FOM) value, w.r.t. Silicon in the common metrics (Baliga FOM, Johnson FOM, Keyes FOM, Huang HCAFOM, Shenai et al., etc.[8, 9, 15, 16]. Although these FOM show that SiC could be a viable choice for power electronics switches, one should be careful about using the FOMs. It can be easily seen that each FOM is designed for a specific application such as high power, high voltage, or high temperature.

Unfortunately, different materials (e.g., Si, GaN, SiC) and devices (e.g., VDMOS, LDMOS, HEMT) are affected differently due to their dimensions, operating conditions, defects, etc. Therefore, an analytical framework for material-device-circuit-system simulations based on early-stage products is needed to assess performance. Mahajan et al. [24] reported an analytical model of an intrinsic Safe Operating Area (SOA) for the selection of a WBG semiconductor that accounts for the self-heating (SH) effect, substrate geometry, basic device parameters (mobility, thermal conductivity, critical electric field, etc.) and trap-induced degradation for applications in a modern power electronics application, that is more reliable than the traditionally used material specific FOMs. The higher the SOA, the higher the performance of a power electronics switch. Based on the analytical framework, the authors show that SiC has a higher SOA, compared to Silicon. In addition, SiC device fabrication technology is quite mature. Among all polymorphs of SiC, transistors with 4H-SiC have better potential in high-power electronics because of their high carrier mobility (μ) (500/50 cm^2/Vs-s for electron/hole, low ON-resistance, faster-switching capability, higher thermal conductivity, etc. [7, 18, 22]. In addition, 4H-SiC (referred to as SiC, hereafter) has high mechanical strength (Young's modulus of ~400-450 GPa), which makes SiC suitable for high-T, high-power electronics and harsh environmental conditions [25]. Therefore, we have chosen SiC for our analysis, in this paper. Several devices/electronics based on SiC are under development, which requires metallization, interfacing, and co-integration with oxide & other materials for SiC devices for the mass commercial market [26].

SiC-based JLT suppresses the impact of interface traps, thus avoiding the need for a counter doping and annealing process to lower the band-to-band (BTBT) tunneling across the channel direction [27]. It has been demonstrated that by placing two P^+ regions adjacent to source/drain regions in a JLT (SD_{Pocket}-SiCJLT), the volume depletion can be improved [28]. With P^+ pockets in the oxide region for $\beta - Ga_2O_3$ JLT, volume depletion improves [29]. However, JLT possesses some inherent limitations. JLT has two modes of operation: inversion and depletion. The channel of a JLT may be fully depleted either by applying a negative voltage (for NMOS) to turn it off or applying a high gate WF (P-type). Also, the channel has to be very thin (~5-10nm), leading to very low ON-current and often unreliable performance due to extreme fabrication constraints. The channel is highly doped to enhance I_{ON}. Depletion-mode transistors require additional circuitry and high-power dissipation for switching

applications in power electronics which increases the power budget, and hence enhancement-mode transistors are highly desirable.This work proposes an enhancement mode double-gate SiC JLT, with an embedded P^+ layer in the oxide region for lower OFF-state current and efficient volume depletion. We thoroughly explore the DC and AC performances of the device (P^+-SiCJLT) and compare it with a similar dimensional SiC JLT without an embedded P^+ layer and discuss the advantages and disadvantages. In addition, we also compare the P^+-SiCJLT with a SiCJLT with P^+ pockets adjacent to the source/drain region (SD_{Pocket}-SiCJLT).

3.6 Device Architectures and Simulation Set-up

The traditional SiC MOSFET was calibrated with an experimental device by Mudholkar et al. [30, 31] considering channel thickness of 1.2 µm, channel/(source/drain) doping concentration of $10^{17}/(9\times10^{19})cm^{-3}$, gate oxide thickness of 3 nm with SiO_2 as gate oxide material and a very thin layer of gold (0.1nm) for source, gate, and drain contacts as SiC JLT is not fabricated yet to the best of our knowledge. Specifically, a mesh with 5 nm length and 2 nm width was used near the channel/source-drain regions to ensure accuracy in capturing detailed device features. The mesh was optimized to balance computational efficiency with precision, focusing on areas with steep gradients where accurate simulation is crucial.

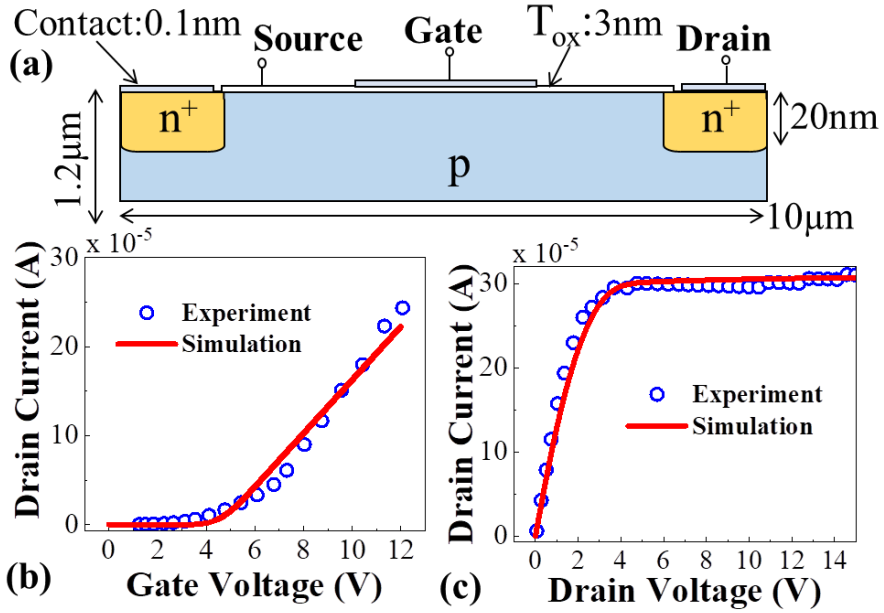

Fig. 3.3: Calibrated TCAD simulation with the (a) experimental device of (b) transfer characteristics at $V_{DS} = 50mV$ (c) output characteristics at $V_{GS} = 6V$ for T_{OX} (SiO_2)=3 nm, N_A=10^{17} cm^{-3}, $N_{source,drain}$=9×10^{19} cm^{-3}, T_{SiC}=1.2 µm, L=20 µm [30, 31].

Grid statistics were adjusted to ensure convergence and minimize numerical errors, providing reliable calibration data. The Fermi–Dirac statistics, Shockley–Read–Hall recombination, and Auger recombination were included. The mobility of SiC has been determined by fitting to be 210 cm/V-s. The mobility degradation is due to scattering at the $4HSiC - SiO_2$ interface and doping and transverse field dependencies of mobility were taken care of by the inversion and accumulation-layer mobility (IalMob) model. The Canali model was used for velocity saturation. All simulations were carried out using Sentaurus TCAD version R-2020.09-SP1 by Synopsys Inc. [32]. The transfer and output characteristics of the TCAD model are calibrated with experiments, as shown in Fig. 3.3(b) and 3.3(c). A SiC JLT can be designed using the calibrated parameters, as shown in Fig. 3.4(a), demonstrating higher performance than traditional MOSFET [33]. We use these parameters to introduce a P^+-SiCJLT device, as shown in Fig. 3.4(b). The substrate is 4H-SiC, and the oxide material is SiO_2. The channel/source(drain) length of the device was taken as 100/20nm, source-drain doping concentration (N_D) as 10^{19} cm^{-3}, and gate work function (WF) as 5.1eV.

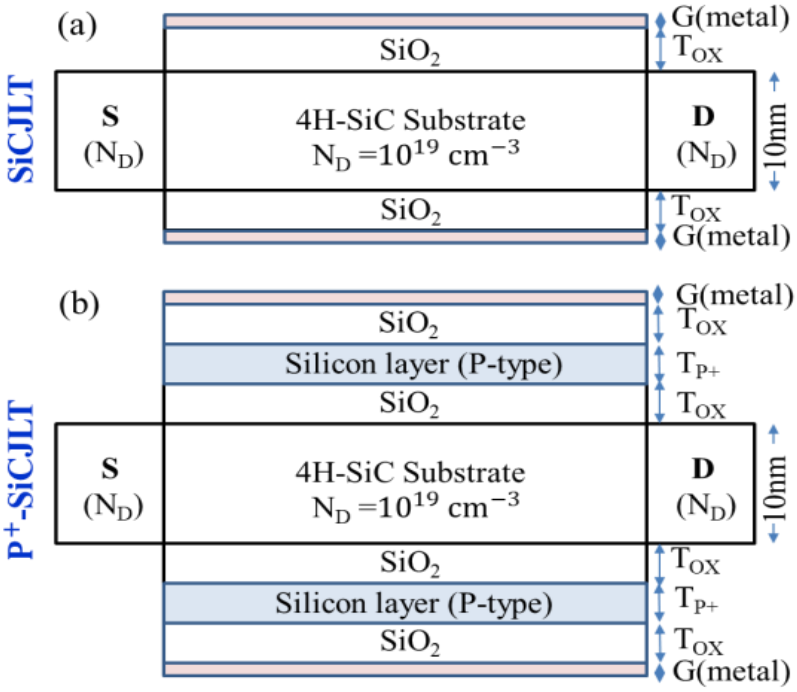

Fig. 3.4: Block diagram (a) SiCJLT (without the P+ layer in the oxide region) and (b) P+-SiCJLT.

Without the P+ layers in Fig. 3.5(a), the energy bands (conduction and valence bands) across the channel exhibit more gradual transitions. The conduction band E_C near the source and drain shows a weaker potential barrier, leading to higher leakage currents, especially at lower gate voltages. In contrast, with the P+ layers, the energy bands shift, creating steeper transitions near the source and drain. This shift results in better confinement of carriers in the channel, as the conduction band E_C shows a more substantial rise, forming a higher potential barrier that reduces leakage.

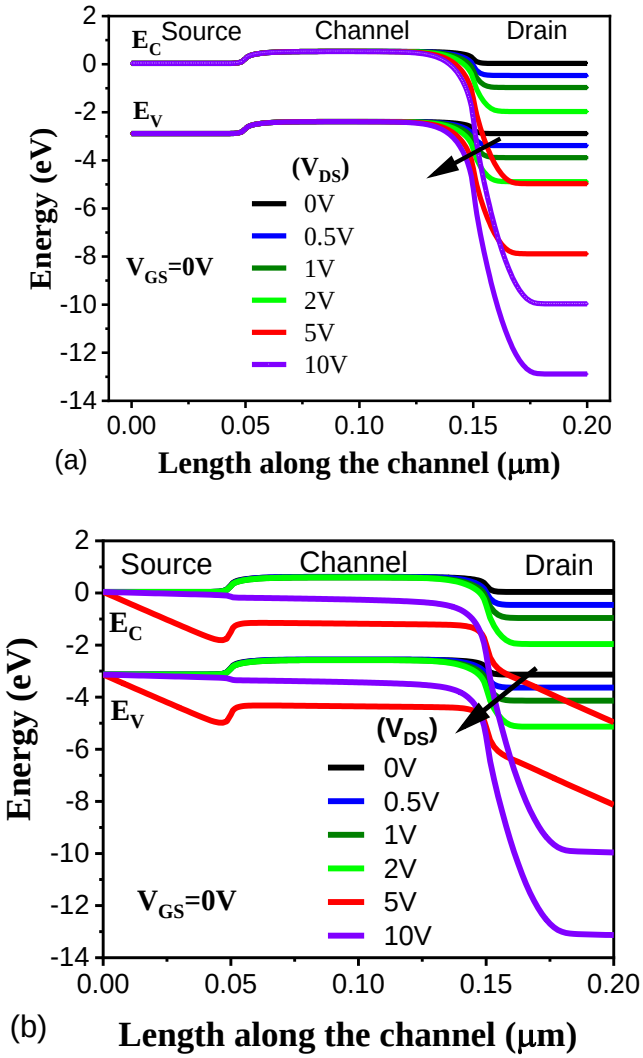

Fig. 3.5: Energy band diagram of (a) SiCJLT and (b) P^+-SiCJLT at $V_{DS} = 0{,}0.5V, 1V, 2V$ $5V, 10V$ and $V_{GS} = 0V$.

At V_{DS}=0.5V and V_{GS}=0V, the conduction band with the P+ layer shows a potential difference of approximately 1.5 eV between the source and drain compared to 1.0 eV in the device without the P+ layers. This 0.5 eV increase significantly improves carrier confinement.

The addition of P+ layers also affects the vertical energy profile across the silicon thickness. With the P+ layers, there is stronger band bending at the surface near the source and drain, which helps suppress the off-state leakage. Without the P+ layers, the conduction and valence bands are more uniformly distributed across the silicon thickness, resulting in weaker electrostatic control.

At V_{DS}=1V and V_{GS}=0V, the energy barrier in the vertical direction increases by approximately 0.7 eV when the P+ layers are included. This increase enhances the overall electrostatic control, leading to a better subthreshold slope and improved performance at higher temperatures.

The inclusion of P+ layers enhances device performance by creating sharper band bending near the source and drain, increasing electrostatic control, reducing leakage, improving the subthreshold swing, and enhancing the high-temperature stability of the device. The numerical shifts observed in the conduction band energies confirm the improvements provided by the P+ layers.

An embedded layer of Silicon in the SiO_2 is added to the proposed device. The embedded P^+ material (Si) has a thickness (T_{P+}) of 2-4 nm and a P^+ (boron) doping concentration (N_{P+}) of $10^{15} - 10^{18} cm^{-3}$ unless otherwise mentioned. The energy band diagram of the P^+-SiCJLT at $V_{GS} = 0V$ and $V_{DS} = 0{,}0.5\text{V}, 1\text{V}, 2\text{V}, 5\text{V}, \text{and } 10\text{V})$ are shown in Fig. 3.5(b). With an increase in V_{DS}, the conduction band of the drain and valance band of the channel overlapped, resulting in better electrostatics for the device. As evident, because of the P^+ pockets, the device exhibits full depletion in the OFF-state. The bias condition at the OFF state is V_{GS} =0 V and a small drain voltage, typically V_{DS} =50 mV. The physical reason for full depletion in the OFF state is the presence of the P+ pockets, which enhance the electric field across the channel, effectively depleting carriers even at zero gate bias. This leads to a wide depletion region, preventing current flow and ensuring low leakage. For lower V_{DS}, there is no band overlapping, meaning that the device has higher tunnel width and hence offers lower leakage current, making the device a better fit for high voltage applications.

In this work, the term "P+" was used more generally to describe the p-type silicon layer incorporated in the top and bottom gate stacks of the device. The intention was to highlight that this layer has a higher doping concentration compared to typical intrinsic or lightly doped p-type regions.

However, it is acknowledged that using the term "P+" may have led to some confusion, as the doping concentrations in the range specified do not achieve degenerate doping levels. The doping concentrations used $10^{15} - 10^{18} cm^{-3}$ were chosen to optimize the electrostatic control of the device while maintaining a balance between performance and fabrication feasibility. The layer should more accurately be referred to as a "moderately doped p-type layer" rather than "P+," as the doping levels do not reach the degenerately doped regime.

3.7 Result and Discussion

The transfer characteristics of a P^+-SiCJLT for P^+ layer doping concentration (N_{P+}) of $10^{15}, 10^{16}, 10^{17}, 10^{18}, 5 \times 10^{18}$, and 10^{19}cm^{-3} at a P^+ layer thickness (T_{P+}) of 2 nm and its comparison with the equivalent dimension SiCJLT (i.e., $T_{OX} = 4\text{nm}$) is shown in Fig. 3.6. It is seen that with an increase in doping concentration of the P+ layer beyond 10^{18}cm^{-3}, the electrostatics is improved. For example, from a N_{P+} shift from 10^{18}cm^{-3} to 10^{19}cm^{-3} , there is an I_{OFF} improvement of slightly more than one decade. However, for N_{P+} change from10^{15}cm^{-3} to 10^{18}cm^{-3}, there is negligible change in both I_{OFF} and I_{ON}. Therefore, even though electrostatics is better at $N_{P+} = 10^{19}\text{cm}^{-3}$, we have considered N_{P+} of 10^{18}cm^{-3} for all simulations to have minimum scattering as well as to see the worst-case scenario of electrostatics. P+-SiCJLT in a double gate architecture helps in realizing an effective volume depletion region. A double-gate P^+-SiCJLT exhibits enhancement mode operation, advantageous for power electronics switching applications. On the other hand, SiCJLT exhibits a depletion mode operation. Depletion mode operation requires extra circuitry, which increases the losses as well as the cost of a power electronic switch. With an increase in the value of N_{P+}, better gate control and I_{ON}/I_{OFF} is expected. With lower I_{OFF}, the low WF gate metal can be chosen. In Silicon-based JLT, a p-type gate WF (>5eV) and an ultra-thin semiconductor substrate thickness of ~5-10nm are required to fully deplete the channel. Such smaller thicknesses with uniform doping with low surface roughness are difficult and costly. Therefore, multiple WF can be selected according to the application for double-gate P^+-SiCJLT. The inset of Fig. 3.6 shows the transconductance (G_m) of a P^+-SiCJLT for different doping concentrations at a P^+ layer thickness of 2 nm. We compare this to an equivalent SiCJLT device. We find that for specified device dimensions and electrical biases ($V_{GS} = \sim 0.8 - 2.4V$), the P^+-SiCJLT better transconductance.

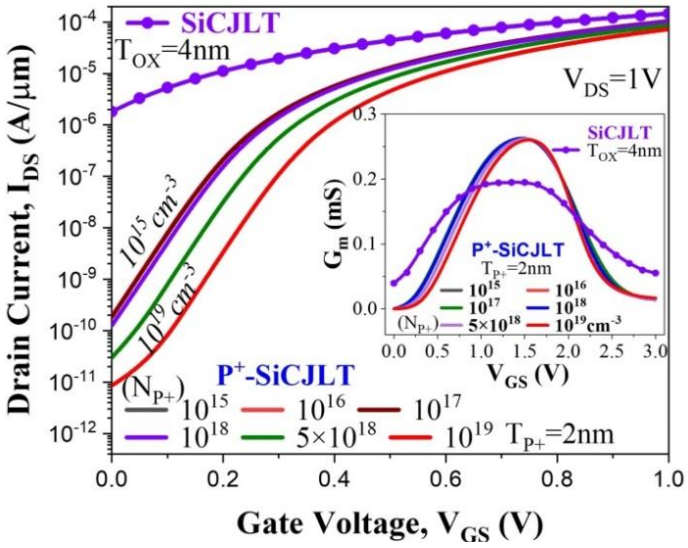

Fig. 3.6: Transfer characteristics of P+-SiCJLT for $N_{P+} = 10^{15}, 10^{16}, 10^{17}, 10^{18}, 5 \times 10^{18}$, and 10^{19}cm^{-3} and $T_{P+} = 2\text{nm}$, $L = 100nm$. This is compared with equivalent dimension SiCJLT at $T_{OX} = 4\text{nm}$. The inset of Fig. 3.6 shows the transconductance for the devices.

The I_{DS}-V_{GS} characteristics were obtained using a double-gate configuration for the P^+ SiCJLT. The applied bias on the P^+ layer in the gate stack is the same as the gate voltage, V_{GS}. The I_{DS}-V_{GS} characteristics remain almost unchanged over the doping range of $1 \times 10^{15} - 1 \times 10^{18}\ cm^{-3}$ because, within this range, the doping concentration is not high enough to significantly alter the electrostatic control of the channel.

For doping concentrations $\geq 1 \times 10^{18}\ cm^{-3}$, the increased carrier density in the P^+ layer leads to enhanced scattering and reduced carrier mobility, which physically explains the observed decrease in I_{DS}.

With P^+-SiCJLT, effective volume depletion can also be tuned as shown in Fig. 3.7(b). However, to deplete a similar dimensional SiCJLT, a high negative voltage ~ (-1.5V) is required (Fig. 3.7(a)). At a moderately higher V_{GS} ($>V_{TH}$), current flows in the center of the substrate in a JLT [4], and current is not hampered by $\text{Si} - \text{SiO}_2$ interface. This is in contrast to an IM MOSFET, where the current flows close to the Si/SiO_2 interface, which gives rise to several reliability issues like mobility degradation due to surface scattering, and interface defects leading to hot carrier degradation, and negative bias temperature instability, etc. P^+-SiCJLT, therefore, avoids these reliability issues as well. In addition, a P^+-SiCJLT has a near-zero vertical electric field in the ON-state, and thus undergoes negligible mobility degradation in ON-state [34].

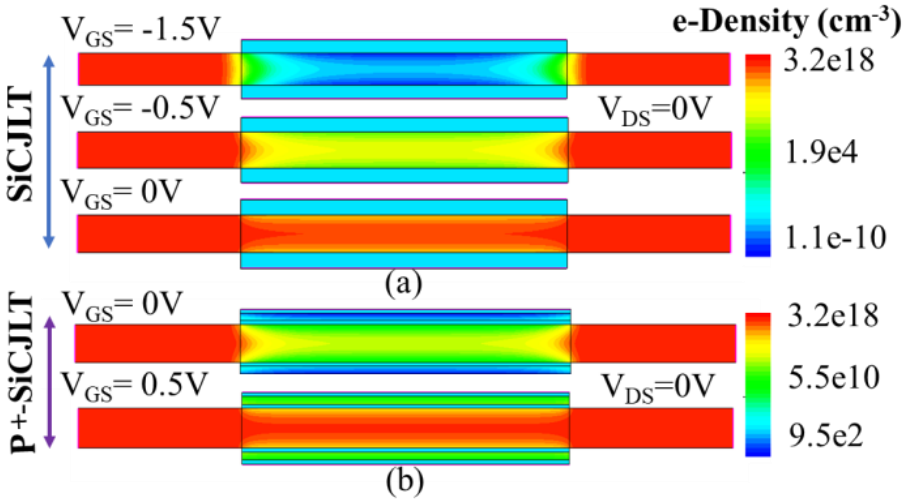

Fig. 3.7: E-density at $V_{DS} = 0V$ for (a) SiCJLT at $V_{GS} = -1.5V, -0.5V, 0V$, and (b) P$^+$-SiCJLT at $V_{GS} = 0V, 0.5V$ and $N_{P+} = 10^{18}\text{cm}^{-3}$ for the same device dimensions as Fig. 3.4.

3.7.1 Threshold Voltage Engineering

P$^+$-SiCJLT can be engineered to achieve customizable V_{TH} and higher performance, according to specific applications. Fig. 3.8(a) shows that better volume depletion can be achieved with higher WF, which will eventually have better I_{ON}/I_{OFF}. The inset of Fig. 3.8(a) shows that the V_{TH} increases with an increase in WF. Also, P$^+$-SiCJLT has a higher V_{TH} than SiCJLT by about 400mV, despite using the material with a similar WF. Currently, there is no analytical or empirical equation in the literature to aid the design the SiC junctionless FETs with varying threshold voltages to the best of our knowledge. Therefore, based on our rigorous simulations, we propose the following equations that predict the V_{TH}, achieved using linear curve fitting the simulation data. Please note that, these equations are not based on any theoretical model but on our simulation, to aid the circuit designer in designing a transistor best suited to a particular application. The V_{TH} (V) of SiCJLT and P$^+$-SiCJLT, at a given WF is given by

$$V_{TH}\ (\text{SiCJLT}) = \text{WF} - 5.23 \tag{3.1}$$

$$V_{TH}\ (\text{P}^+\text{- SiCJLT}) = \text{WF} - 4.91 \tag{3.2}$$

with 4 < WF <5.2. The V_{TH} can also be tuned by changing the doping concentration of the P$^+$ layer (N_{P+}). With an increase in N_{P+}, OFF-state current and I_{ON}/I_{OFF} improves and V_{TH} increases as seen in Fig. 3.8(b). Also, V_{TH} can be tuned by changing the oxide thickness. A device with thinner gate oxide has a higher V_{TH} as shown in Fig. 3.8(c).
It should be noted that such thin gate oxides may be leaky due to fabrication constraints.

If $T_{OX1} = T_{OX2}$, the V_{TH} of SiCJLT and P$^+$-SiCJLT can be written as:

$$V_{TH}\ (\text{SiCJLT}) = -0.47 \times T_{OX1}(= T_{OX2}) + 0.33 \quad (3.3)$$

$$V_{TH}\ (\text{P}^+\text{- SiCJLT}) = -0.52 \times T_{OX1}(= T_{OX2}) + 0.72 \quad (3.4)$$

with 1 nm < T_{OX1}=T_{OX2} < 3 nm. The P$^+$-SiCJLT provides another option to tune the V_{TH} of the device by changing the P$^+$ layer thickness. Simulations of devices with T_{P+} of 1nm, 2nm, and 3 nm and N_{P+} of 10^{18}cm^{-3}, are shown in Fig. 3.8(d). Equations (3.1-3.4) will be helpful in the Design Technology Co-Optimization (DTCO) of similar transistors. The development of these equations provides a solid foundation for understanding and predicting the threshold voltage behavior of P+-SiCJLT and SiCJLT devices in a specific geometry. This allows for easier integration into circuit simulations and provides insights into how different parameters affect device performance. By fine-tuning these relationships, we can now better model the behavior of junctionless transistors in power electronics applications, ensuring more accurate performance predictions. However, because these equations were tailored to a specific set of device

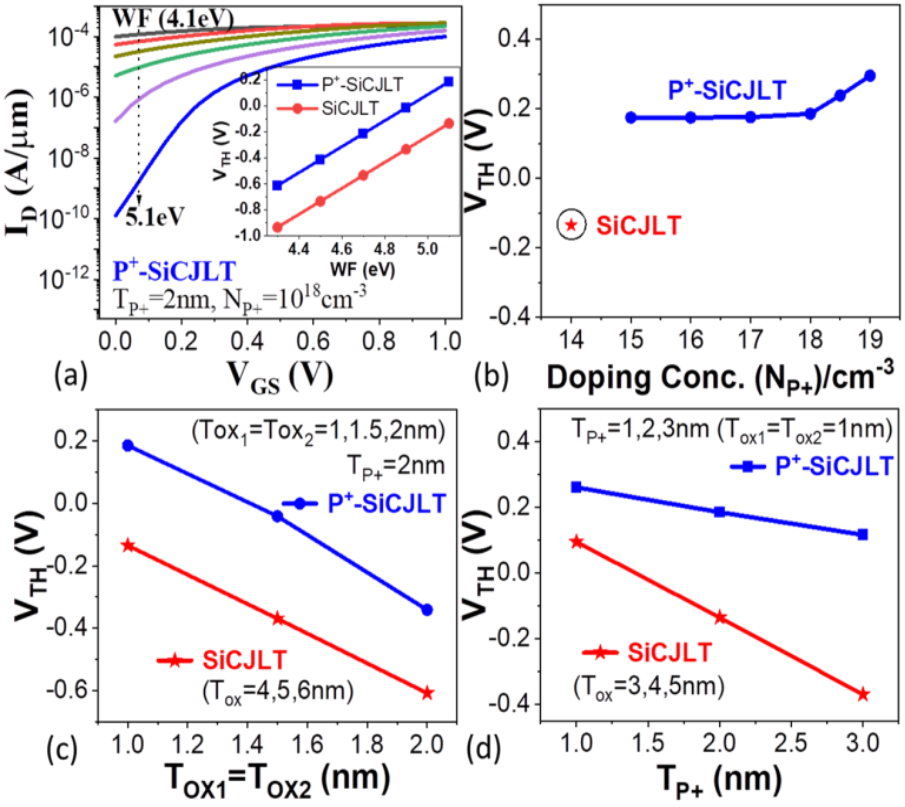

Fig. 3.8: P$^+$-SiCJLT is simulated with $N_{P+} = 10^{18}$cm^{-3}, and $T_{P+} = 2$nm for (a) I_{DS} with gate voltage for WF=4.1-5.1eV. Inset of this Fig. also shows the V_{TH} change with WF (b) V_{TH} change with N_{P+} (c) V_{TH} change with $T_{OX1} = T_{OX2} = 1\ to\ 2\ nm$ (d) V_{TH} change with T_{P+} = 1 to 3 nm. The characteristics are compared with equivalent dimension SiCJLT.

dimensions, they may not directly apply to devices with significantly different geometries (e.g., variations in channel length or width) without recalibration. The device with a thinner P^+ layer exhibits improved volume depletion and therefore has better electrostatics. Therefore P^+-SiCJLT provides the capability to tune the V_{TH}, in several different ways (P^+ layer thickness and P^+ layer doping) in addition to the traditional V_{TH} tuning approaches (WF, T_{OX}). This can provide the engineers with multiple fabrication options if a limit is reached with one parameter. Therefore the P^+-SiCJLT increases the scalability of JLTs.

The impact of parameters such as T_{OX1} and T_{OX2} on the electric field distribution and channel depletion were carefully analyzed. For instance, thinner gate oxides increase gate capacitance, which in turn raises V_{TH} by requiring a stronger gate field to invert the channel. The inclusion of the P+ layer in the P^+-SiCJLT increases V_{TH} by depleting the channel more effectively. T_{OX1} and T_{OX2} were defined based on how they affect gate control and depletion width. These parameters were adjusted to optimize electrostatic control and performance for the device applications explored in this study.

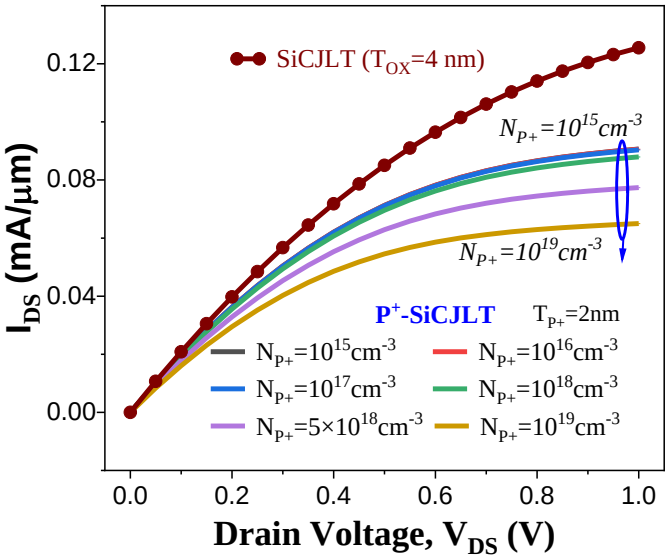

Fig. 3.9: Drain current with drain voltage for P^+-SiCJLT for $N_{P+} = 10^{15}\text{cm}^{-3}, 10^{16}\text{cm}^{-3}, 10^{17}\text{cm}^{-3}, 10^{18}\text{cm}^{-3}, 5 \times 10^{18}\text{cm}^{-3}, 10^{19}\text{cm}^{-3}$ at $T_{P+} = 2\text{nm}$. This is compared with equivalent dimension SiCJLT.

3.7.2 Lower Output Current

Fig. 3.9 shows the output characteristics of a P^+-SiCJLT for different P^+ doping concentrations, and the same is compared with equivalent dimension SiCJLT. P^+-SiCJLT has lesser I_{DS} than a SiCJLT. The primary physical mechanism for I_{DS} degradation with increasing P^+ layer doping at higher V_{DS} in P+ SiCJLT is the

enhanced depletion of the channel. As the P^+ doping increases, the built-in electric field becomes stronger, leading to a more significant depletion of carriers in the channel. This reduction of available carriers diminishes the current drive capability of the device, especially at higher drain voltages (e.g., $V_{DS} = 2V$), where the channel is further pinched off. The result is a reduced I_{DS}, not primarily due to scattering, but due to the more effective carrier depletion induced by the higher P^+ doping.

3.8 High-Temperature Performance of DG-SiCJLT and P^+-SiCJLT

With the proposed P^+-SiCJLT, the applicability of the JLTs will be further stretched because of the advantages ((increased scalability, enhancement mode operation, multiple ways to tune V_{TH}, etc.) The proposed P^+-SiCJLT is also advantageous in terms of intrinsic gain at room and even high T.

3.8.1 Drain Current at High-Temperature

Usually, with a rise in temperature (T), the threshold voltage (V_{TH}) falls and hence the drain current rises for all transistors. In an inversion mode device, though V_{TH} reduction increases I_D, mobility reduction due to phonon scattering eventually decreases the drain current [5, 35, 36]. In a JLT, with an increase in T, impurity scattering (mobility, $\mu \propto T^{3/2}$) and phonon scattering ($\mu \propto T^{-3/2}$) compensate for each other at a particular V_{GS} called zero temperature coefficient (ZTC) [37], and therefore, mobility reduction with higher T is lesser in a JLT compared to an IM MOSFET. Therefore, in JLTs, reduction in mobility with temperature is much lower than other types of transistors, and hence current increases marginally with a monotonous trend [38]. In conclusion, JLT shows better I_{ON} and I_{OFF} and hence superior I_{ON}/I_{OFF} than conventional transistors even at higher temperatures, making the device suitable for higher temperature applications.

There is a degradation of e-mobility with T increase as shown in Fig. 3.10. The transfer characteristics of a P^+-SiCJLT for a T range of 300K-600K and its comparison with SiCJLT are demonstrated in Fig. 3.11(a). With an increase in T, I_{OFF} degrades for both the devices. The I_{ON} is very marginally improved with an increase in T, unlike in conventional transistors. Therefore, I_{ON}/I_{OFF} is better for P^+-SiCJLT even at a higher T.

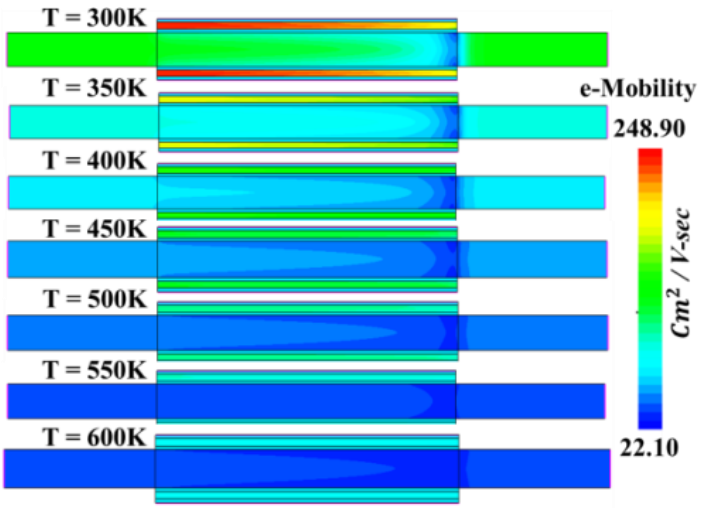

Fig. 3.10: Electron mobility for P^{+}-SiCJLT at T $= 300\text{K} - 600\text{K}$ at $50K$ $step\ size$ and $N_{P+} = 10^{18}\text{cm}^{-3}, T_{P+} = 2\text{nm}$.

SiCJLT has a higher output current than P+-SiCJLT and degrades with T as shown in Fig. 3.11(b). The ON-state current of a JLT is slightly lesser than conventional transistors because of its high doping concentrations (~$10^{18} - 10^{19}$ cm^{-3}) in the channel region. However, it is almost comparable, with an addition of other advantages. On the same note, SiC-MOSFET with two P-N junctions has a better current than SiC-JLT. The MOSFET typically shows a higher current drive for the same dimention as measured from TCAD simulation, capability due to the presence of the two P-N junctions. At V_{GS}=5 V and V_{DS}=10 V, the I_{DS} for the SiC-MOSFET was approximately 15 mA. The MOSFET showed more significant degradation in performance at elevated temperatures. At 450K, the V_{TH} shifted by approximately 200 mV, and the drain current dropped by about 35%, resulting in a considerable increase in leakage current in the subthreshold region. The subthreshold slope for the MOSFET increased significantly with temperature, reaching around 160 mV/dec.

In comparison, under the same conditions, the SiC-JLT exhibited a slightly lower current of about 12 mA due to the absence of strong P-N junctions controlling the current flow. On the other hand, the SiC-JLT exhibited much better high-temperature performance. At 450K, the threshold voltage shift was only about 50 mV, and the drain current decreased by less than 15%. Importantly, in the subthreshold region, the SiC-JLT maintained lower leakage currents due to the better electrostatic control offered by the junctionless architecture. The SiC-JLT maintained a lower subthreshold slope of

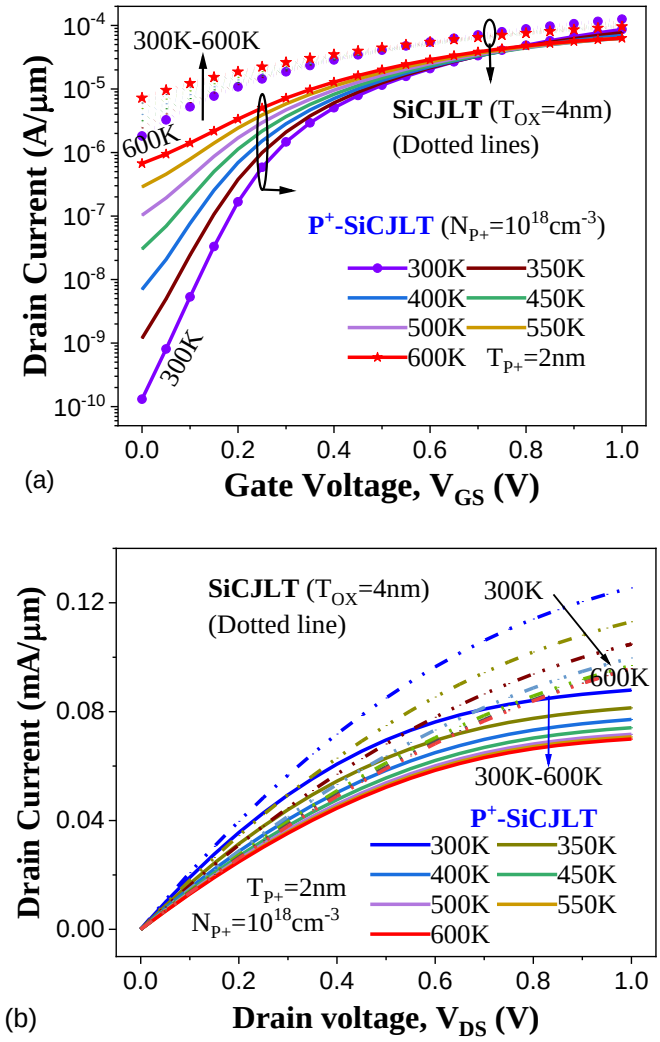

Fig. 3.11: (a) Transfer characteristics V_{DS} = 1V and (b) output characteristics P^+-SiCJLT at $T = 300\text{K}$ to 600K at 50K step size for $N_{P+} = 10^{18}\text{cm}^{-3}, T_{P+} = 2\text{nm}$ at V_{GS} = 1V & compared with equivalent SiCJLT.

approximately 90 mV/dec at 450K, indicating better control over the subthreshold current. Combining JLT with SiC has better prospects for high-temperature applications [27, 28]. Such type of device has enormous potential in high voltage power MOS devices, system-on panels, and 3D stacked applications. Other authors have previously studied the breakdown voltages of such devices, which is one of the primary requirements of power electronics applications. For, example, Cheng et al found that polysilicon GAA JLFET gives a breakdown voltage (BV) of ~60 V due to the GAA structure, while the planar polysilicon FET shows poor breakdown performance [39]. However, it is well known that GAA transistors suffer from fabrication complexities.

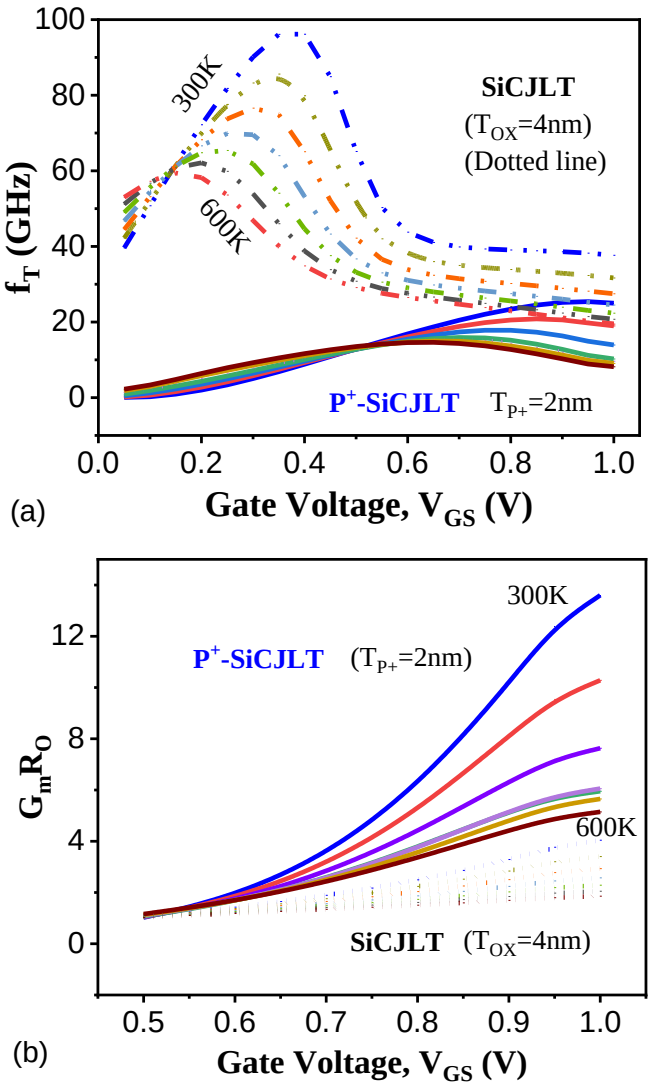

Fig. 3.12: (a) f_T with V_{GS} and (b) intrinsic gain with V_{GS} for P$^+$-SiCJLT at T = 300K – 600K at 50K step sizem for $N_{P+} = 10^{18}\text{cm}^{-3}$, $T_{P+} = 2\text{nm}$. This is compared with equivalent dimension SiCJLT.

Therefore, SiC JLTFET has been proposed to increase the breakdown voltage characteristics [27, 33]. Here in this paper, we propose a better transistor with much higher current performance and threshold voltage tunability.

GAA transistors require precise control over nanowire dimensions and multiple deposition steps for gate-all-around structures, which can be challenging and costly. In contrast, the P+-SiCJLT uses conventional planar processes with the addition of a P+ layer, which is simpler to integrate into existing fabrication lines. The P+-SiCJLT fabrication process avoids the need for advanced lithography and complex 3D structures, leading to lower overall production costs compared to GAA transistors.

3.8.2 Unity-gain Cut-Off Frequency at High Temperature

The unity-gain cut-off frequency, f_T $(= G_m/2\pi(C_{GS} + C_{GD}))$ is one of the most important figures-of-merit for device applications in radio frequency applications. Where, C_{GS}, C_{GD} are gate-to-source, and gate-to-drain capacitances respectively, including fringing and overlap capacitances. Small signal AC device simulation is executed at $V_{DS} = 1V$ with an applied frequency of 1 MHz for the P^+-SiCJLT with a P^+ layer thickness of 2nm. f_T is often influenced by geometrical parameters and parasitic capacitances. Minimum parasitic is desired for better f_T performance.

As shown in Fig. 3.12(a), there is a higher f_T for SiCJLT compared to P^+-SiCJLT. f_T is degraded with an increase in T, for both the devices. Also, shown in Fig. 3.12(b) is the intrinsic gain $(= G_m R_0)$ of the P^+-SiCJLT for $\mathrm{T} = 300 - 600\mathrm{K}$ for $N_{P+} = 10^{18}\mathrm{cm}^{-3}$ and $T_{P+} = 2\mathrm{nm}$ at a drain voltage of 1V. R_0 is the output resistance. The intrinsic gain of a transistor is its maximum possible voltage gain, regardless of the bias point. Even though JLT has a slightly lesser G_m compared to a conventional MOS transistor, the intrinsic gain is better for a JLT as compared to its junction-based counterpart. P^+-SiCJLT has better gain than SiCJLT both at room and high T, though for both the devices, gain decreases with an increase in T.

Table 3.1 Performance comparison of SiCJLT, sd_{pocket}-sicjlt, P^+-sicjlt

	V_{TH}	Mode	Temp	I_{ON}/I_{OFF}	$f_T@V_{GS} = 1V$	$G_m R_O@V_{GS} = 1V$
SiCJLT	-ve	Depletion	300K	80	3.7×10^{10}	4.04
			400K	58	2.7×10^{10}	2.93
			500K	40	2.2×10^{10}	2.28
SD_{Pocket}-SiCJLT [28]	+ve	Enhancement	300K	7.0×10^{3}	9.3×10^{9}	1.98
			400K	0.5×10^{3}	8.5×10^{9}	1.96
			500K	2.3×10^{2}	7.9×10^{9}	1.90
P^+-SiCJLT	+ve	Enhancement	300K	8.0×10^{5}	2.5×10^{10}	13.59
			400K	1.0×10^{4}	1.3×10^{10}	7.62
			500K	0.9×10^{2}	9.6×10^{9}	6.05

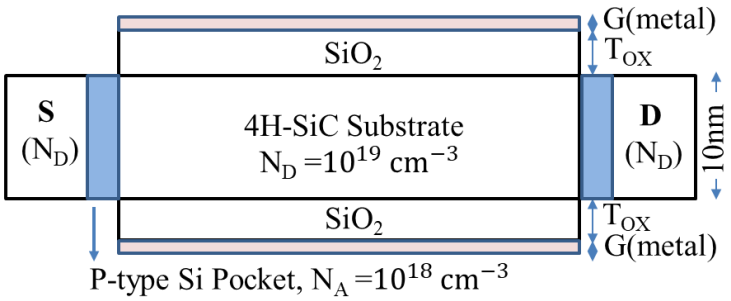

Fig. 3.13: Block diagram of SD_{Pocket}-SiCJLT with P+ pocket thickness on 5nm.

3.9 Comparison with Devices Featuring Embedded Pockets in Substrate near Source/Drain Contact

Finally, to see if the embedded P^+pocket will have any advantages if placed on any other area, other than that in oxide, the device is compared with a device with embedded P^+ pockets of 5nm wide at source and drain sides (SD_{Pocket}-SiCJLT), and P^+ doping of $5 \times 10^{18}\ cm^{-3}$ shown in Fig. 3.13 [28]. We use similar models and parameters as in the case of other JLTs. SD_{Pocket}-SiCJLT is calibrated with [28]. Fig. 3.14 shows the comparison of $I_{DS} - V_{GS}$ characteristics for SiCJLT, SD_{Pocket}-SiCJLT, and P^+-SiCJLT. As shown in Table 3.1, P^+-SiCJLT outperforms the other devices considered in terms of I_{OFF}, I_{ON}/I_{OFF} and enhancement mode operation, and intrinsic gain at room temperature. In addition, the V_{TH} tunability will also suffer in a device with P^+ pockets near the source/drain.

Therefore, P^+-SiCJLT not only improves the I_{ON}/I_{OFF} ratio and scalability but also the efficacy of the transistor configuration for a power electronic switch.

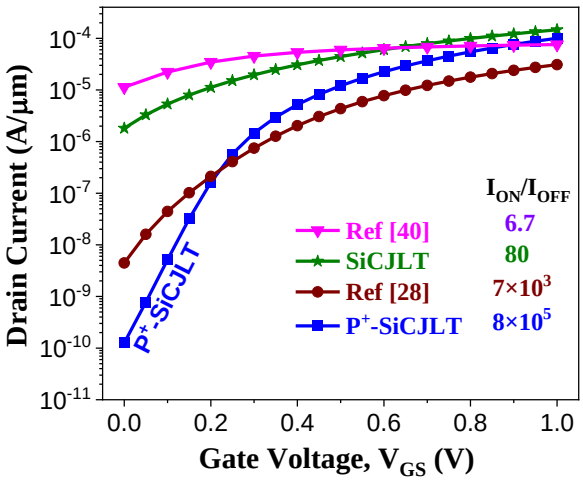

Fig. 3.14: I_{ON}/I_{OFF} ratio comparison of P^+-SiCJLT at $N_{P+} = 10^{18}$cm^{-3}, $T_{P+} = 2$nm, with equivalent SiCJLT ($T_{OX} = 4$nm), and, SDPocket-SiCJLT (pocket width of 5 nm and $T_{OX} = 4$nm).

As can be seen from Fig. 3.14, out of all the devices, namely P^+-SiCJLT, SiCJLT, SD_{Pocket}-SiCJLT [28] and embedding two P+ pockets in buried oxide [40]; SiCJLT and P^+-SiCJLT has the similar order of ON-state currents at $V_{GS} = 1V$; while P^+-SiCJLT has better OFF-state current at $V_{GS} = 0V$ by few orders of magnitude at room temperature. As these devices are to use in circuit simulations and eventually to some systems, evaluating circuit performance parameters at temperatures 300-500K are essential and are shown in Table 3.1. The devices are evaluated and compared in terms of switching capability (I_{ON}/I_{OFF} ratio), speed of operation (unity gain cut-off frequency, f_T) and the maximum voltage gain of the transistor ($G_m R_o$). The I_{ON}/I_{OFF} of P^+-SiCJLT is 114 and 10^4 times higher than SD_{Pocket}-SiCJLT and SiCJLT respectively at 300K. The value decreases with an increase in temperature for each device. SiCJLT, however has highest f_T followed by P^+-SiCJLT (1.48 times higher) and SD_{Pocket}-SiCJLT. As expected, f_T decreases, with an increase in temperature for all of the devices. P^+-SiCJLT offer an intrinsic gain that is 6.9times higher than SD_{Pocket}-SiCJLT and 3.4 times higher than SiCJLT at room temperature. Even at 500K, the intrinsic gain value of P^+-SiCJLT is almost 3 times better than the other devices considered. Therefore, it can be concluded that P^+-SiCJLT outperforms SD_{Pocket}-SiCJLT and SiCJLT in terms of I_{ON}/I_{OFF} and $G_m R_o$ as compared to other devices; even though f_T for P^+-SiCJLT is only 1.48 times inferior to SiCJLT and better than SD_{Pocket}-SiCJLT.

For high voltage or power electronics applications, a normally OFF MOSFET is favored for safe high-voltage operation and to alleviate OFF-state power dissipation. Depletion mode transistors require extra fail-safe circuitry in a power electronics circuit which leads to power dissipation [41, 42]. Enhancement mode transistors, on the other hand do not necessitate extra circuitry and therefore are power efficient and cost effective. To achieve an appreciable high current, a device needs to be highly doped, which however, results in a negative V_{TH}. There are significant efforts being made to convert a depletion mode transistor to enhancement mode one with including fundamental changes in structure designs at the cost of extra process steps and complexity, few examples are as follows. Chabak et al., fabricated an enhancement-mode Ga_2O_3 MOSFET empowered by arrays of Sn-doped non-planar fins on a semi-insulating (100) $\beta - Ga_2O_3$ substrate to shift the V_{TH} from negative to positive value [42]. Because this is a non-planer kind of device, it needs additional fabrication steps to achieve enhancement mode operation and, therefore, is costly. Feng et al, realized the

enhancement mode operation of a Ga_2O_3 MOSFET by integrating a laminated-ferroelectric (FE) charge storage gate (L-FeG) structure by replacing the normal gate dielectric material with an FE dielectric, which is again costly and may have reliability issues because of FE materials [43]. Naydenov et al, demonstrated that the junctionless FinFET with SiC material could be very attractive for lower voltage applications [44]. Therefore, in comparison to the existing methods for converting depletion to enhancement mode that needs extra process steps; our proposed structure achieves this enhancement mode operation just by inserting P+ pocket in relatively simple fabrication steps that is inexpensive and incredibly less time-consuming. This improvement in power dissipation becomes advantageous at higher temperatures and voltages. Therefore, the slight loss in current is compensated hugely by an immense gain in power loss.

3.10 Fabrication steps for the proposed device

The proposed structure can be fabricated in multiple ways. One of the possible fabrication workflows is described here.

Step 1: Bonding: The fabrication process can start with a SiC wafer bonded to an SOI wafer, as in [17]. Another option is the hydrophobic wafer bonding process [45] (Fig. 3.15(a)).

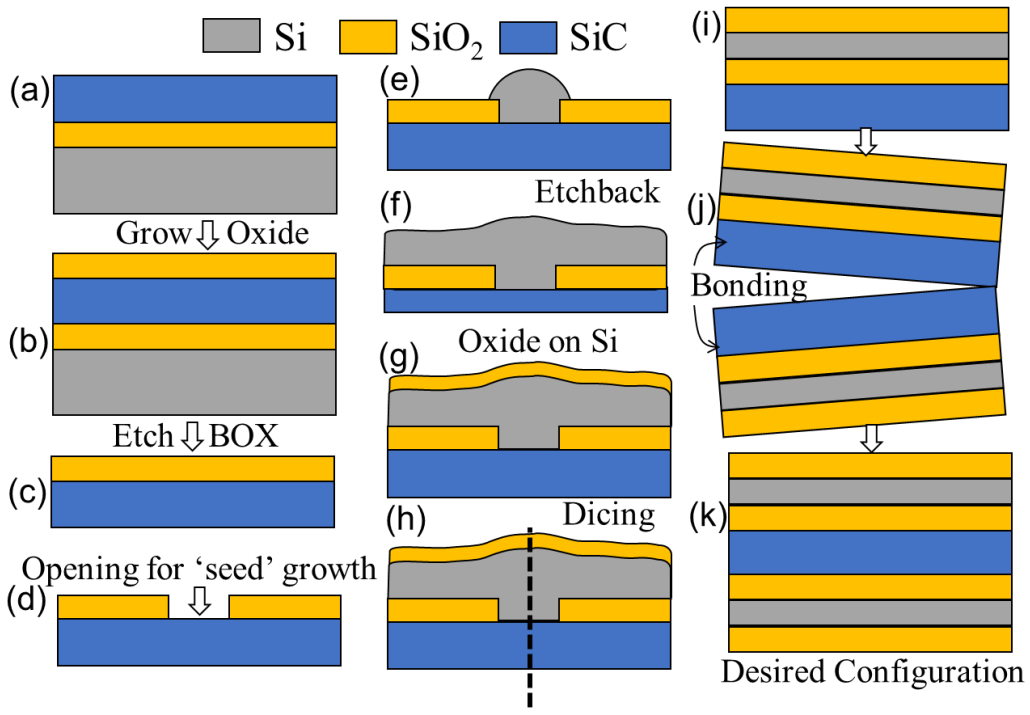

Fig. 3.15: (a)-(k) Fabrication steps of a P^+-SiCJLT.

Step 2: Growth of SiO2: The first SiO_2 layer can be deposited on the SiC substrate using wet oxidation in the presence of N_2O and subsequent annealing in NO to reduce the impact of interface traps in SiC/SiO_2, following the method proposed in Mudholkar et, al. [30] (Fig. 3.15(b)).

Step 3: Deposition of Si using 'Seed Growth' Method: Once the SiO_2 layer has been obtained, the Silicon layer (for embedded P^+) can be grown using the 'seed method' employed in SOI wafers [46]. The growth of an epitaxial layer of silicon-on-insulator dioxide has been achieved previously, following the 'seed growth method' in several reports. In their paper, Kim et al. [47] achieved the growth of Silicon on SiO_2. They also confirm a highly crystalline state by cross-sectional imaging and diffraction pattern analysis, surface roughness analysis, and wide-range epitaxy analysis. Researchers have also successfully co-integrated Logic Ultra-Thin Body and Box (UTBB) devices and bulk-Si I/O devices on the same chip, using a similar fabrication technique [48]. Not only Silicon, but deposition of epitaxial layers of materials like GaAs [49–51], and germanium [52, 53], on SiO_2 also has been reported using similar procedures (Fig. 3.15(c) –(f)).

Step 4: Growth of SiO_2: SiO_2 can be further deposited on the newly grown Silicon using atomic layer deposition [54] or thermal oxidation [55] (Fig. 3.15(g)).

Step 5: Bonding to form double-gated structure: The fabricated wafers can then be diced and bonded using techniques such as hydrophobic wafer bonding process, to achieve the desired double gated structure [29, 54] (Fig. 3.15(h)- (k)).

3.11 Summary

We have proposed a new design of SiC junctionless transistors, by embedding P^+ pockets in the oxides (P^+-SiCJLT). P^+-SiCJLT exhibits enhancement mode operation and offers excellent electrostatics which has enormous potential for application in high power electronics, memory, and IoT. The device offers multiple options for tuning the V_{TH} for different applications, by changing the P^+ layer thickness, P^+ layer doping, workfunction, and oxide thickness. This tremendously improves the device's scalability, as it is not limited by the fabrication constraint of a single dimension. We compared our device with an equidimensional traditional SiC JLT till high T. Although P^+-SiCJLT has a slightly lower On-current than an equivalent SiCJLT device, at the same applied bias, the improvement in I_{ON}/I_{OFF} makes up for it. P^+-SiCJLT offers better gain and inferior f_T than SiCJLT, making P^+-SiCJLT more fit for lower power and higher voltage

applications. The excellent characteristics of the P^+-SiCJLT are retained at a high temperature making it suitable for power electronics applications. With all these advantages, our device configuration takes a significant step forward toward the practicality of commercializing junctionless FETs.

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