CHAPTER 4
Reliability of JL-TFET in Harsh Environment

Contents

4.1 Introduction

The ability to reduce the size of devices, especially MOSFETs, has long been an important factor in the semiconductor industry since it has allowed for the development of increasingly efficient integrated circuits (ICs) as aforementioned. However, conventional MOSFETs have encountered challenges as the need for improved power efficiency has increased, especially in obtaining subthreshold slopes (SS) below 60 mV/decade. The restriction is a noteworthy obstacle to the continued reduction of gadget size. A technology that demonstrates potential for low-power applications is the tunneling field-effect transistors (TFET), as it can achieve SS values of less than 60 mV/decade.

Junctionless transistors (JLT) exhibit better SCEs, and therefore, the channel length can be reduced further to a lower value compared to a conventional MOSFET. A JLT has homogeneous and uniform doping and bears no PN junction in the source-channel-drain path making the fabrication process of process relatively simpler and cost-effective than a junction-based device as mentioned in previous chapter [1, 2]. TFETs have been studied immensely for low-voltage applications [3, 4]. A TFET functions by a distinct mechanism called Band-to-Band Tunneling (BTBT). In this case, carriers do not need high energy to cross a conventional energy barrier since they can tunnel straight from the valence band of the source to the conduction band of the channel. However, even if the device has a lower subthreshold slope; the ON-state current is lesser, resulting in a lower I_{ON}/I_{OFF} ratio (typically $<10^{-6}A$) at lower voltages [5]. Other drawbacks of TFETs are ambipolar conduction, large gate-to-drain capacitance, etc [6, 7]. Pocket doping [8], gate work-function engineering [9], hetero material [10], gate-to-drain overlap [11], hetero-dielectric TFET [12], etc are investigated to address these shortcomings. Combining both JLT and TFETs, we have studied JL-TFET for low-power and high-temperature applications. Because there is no junction, JL-TFETs provide better gate control, which improves performance metrics like speed and power efficiency. Furthermore, JL-TFETs show lower leakage current, which solves a major issue with traditional FETs, especially at smaller feature sizes. Future semiconductor technologies may find JLTFETs appealing due to their simplified fabrication method, which has the potential to reduce costs and improve scalability. Moreover, as the temperature changes, device performance parameters such as ON-OFF current ratio (I_{ON}/I_{OFF}), transconductance (G_M), threshold voltage (V_{TH}), and cut-off

frequency (f_T) change significantly which will affect overall performance in an IC and that is our main concern for JL-TFET.

Furthermore, with the growing prevalence of electronic devices in radiation-prone areas, there is a concern about their susceptibility and tolerance to radiation-induced damage. Radiation can originate from several sources, such as nuclear reactors, medical equipment, other technological gadgets, and cosmic rays, etc [13, 14]. The impact of radiation on transistors is a critical consideration, especially in critical applications such as medical devices, nuclear power plants, and aircraft, etc. Transistors are vulnerable to a range of radiation types, including gamma rays, neutron radiation, and ionizing radiation like alpha and beta particles [15–17]. In the upcoming section, we delve into the effects of ionizing radiation on device properties, focusing on aspects such as $I_{DS} - V_{GS}$ characteristics, threshold voltage shifts (ΔV_{TH}), and degradation of other electrical parameters. In addition, we have examined the radiation-hardening techniques specifically for JL-TFETs by using the process variation method to mitigate the effects of radiation-induced damage. Optimizing the oxide thickness and the substrate thickness to minimize the introduction of defects and ensure uniform device characteristics can improve radiation hardness.

Another major reliability issue with JL-TFETs is HCI, which can damage the gate oxide and affect overall device performance due to the strong electric fields inside the device that can produce hot carriers. We examine methods to reduce HCI impact in JL-TFETs, aligning with their distinctive design requisites [18, 19].

4.2 Structure and Operating Principle of JL-TFET

The TFET can operate as an n-type or p-type device, depending on the dominant carrier type in the channel at the time of activation. A device is referred to as "n-type TFET" if electrons are the main carriers in the channel, and "p-type TFET" if holes are the predominant carriers. A key structural difference between TFETs and conventional MOSFETs lies in the doping types of the Source, Channel, and Drain regions. In MOSFETs, the Source and Drain are typically of the same doping type, whereas in TFETs, they are of opposite types. The channel of both p-TFETs and n-TFETs is intrinsically doped, whereas in NMOS and PMOS MOSFETs, the channel doping is p-type and n-type, respectively.

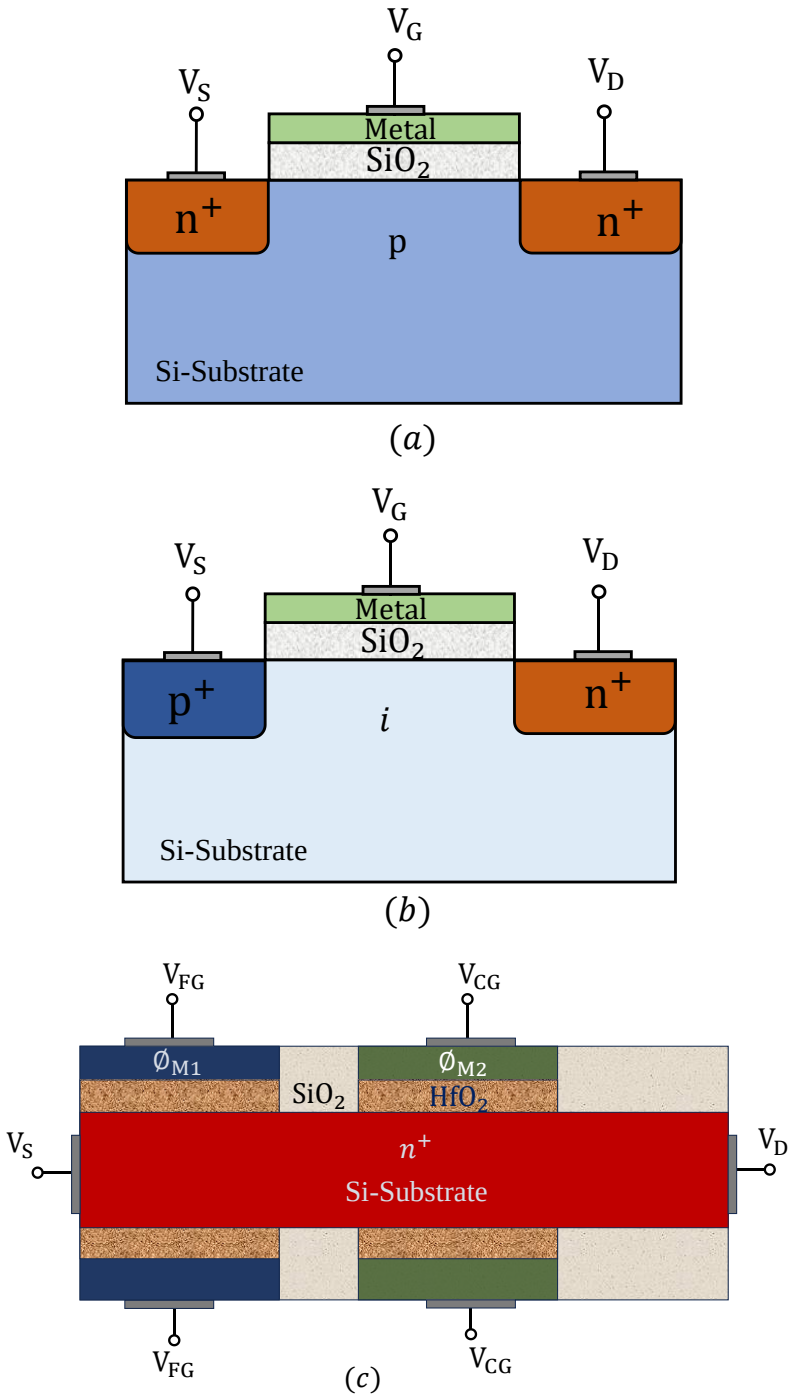

Fig. 4.1: Cross-sectional view of a conventional n channel (a) MOSFET (b) TFET (c) JL-TFET

Fig. 4.1(a)-(c) illustrates the cross-sectional views of a conventional MOSFET, TFET, and JLTFET respectively, with the sources grounded as depicted. In the case of a conventional MOSFET, the operation relies on the formation of an inversion layer beneath the gate when a positive gate bias is applied. This inversion layer allows current to flow between the source and drain terminals. By varying the voltage applied to the

gate, the conductivity of the channel can be controlled, enabling the MOSFET to act as a switch or an amplifier. In the case of a TFET, a heterojunction, or highly doped area, is added close to the channel region. Carriers can tunnel from the source to the channel when a voltage is supplied to the gate, which causes a tunneling current to flow through the barrier. In comparison to traditional MOSFETs, this tunneling current may have a lower power consumption and produce steep subthreshold slopes since it grows exponentially with the applied gate voltage.

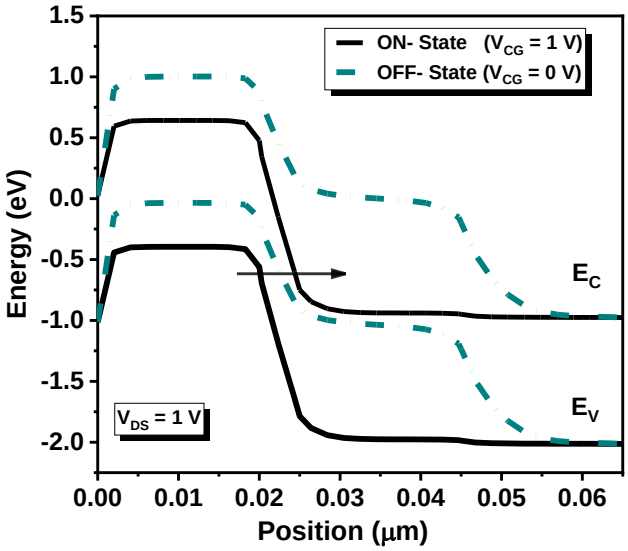

Fig. 4.2: Energy band diagram of JL-TFET at fixed drain bias $V_{DS} = 1V$, in the ON-state ($V_{CG} = 1V$) and OFF-state ($V_{CG} = 0V$) at $V_{FG} = 0V$ and ϕ_{M1}=5.9eV, ϕ_{M2}=4.25eV

Whereas, the JL-TFET functions by modulating the electric field within a uniform semiconductor channel to enable carrier transport via BTBT. JL-TFETs rely on a continuous channel and do not have strongly doped junctions as conventional TFETs do. The control gate (CG) and fixed gate (FG) are two fundamental ideas that are essential to JL-TFET functioning. The energy band structure of the channel is changed by the presence of this virtual p-type area that the FG creates. This changed band structure makes it easier for carriers to quantum tunnel over the channel when an appropriate voltage is placed between the source and drain, allowing the transistor to conduct current. By supplying a voltage, the control gate modifies the electric field inside the channel. In the OFF-state of an n-channel JL-TFET, where the control gate-to-source voltage (V_{CG}) is 0 V and the drain-to-source voltage (V_{DS}) is greater than 0, the channel conduction band (CB) is positioned above the valence band (VB) of the source. In this configuration there is no BTBT, resulting in a very low leakage current (Fig. 4.2). Instead, the leakage current in the OFF-state is primarily due to mechanisms such

as Trap-Assisted Tunneling (TAT), Shockley-Read-Hall recombination (SRH), and gate oxide leaks.

As the V_{CG} is increased from zero bias to a positive value, the CB of the channel gradually moves downwards. Once it aligns with the VB of the source at a sufficient V_{GS}, electrons start tunneling from the source VB to the channel CB. The positive drain voltage then drives these tunneling electrons toward the drain. Similarly, in a p-channel JL-TFET, when a sufficient negative bias is applied to the gate terminal, the VB of the channel rises above the CB of the source. This allows carriers (holes) to tunnel into the channel, and the negative drain voltage sweeps these entering holes toward the drain.
By regulating the carrier concentration, this modulation creates a virtual junction inside the channel. To designate the source and drain areas, the FG keeps the voltage constant in the interim. Carriers close to the source region tunnel through the virtual junction's energy barrier and enter the conduction band when a negative gate voltage is applied. Current can flow through this tunneling mechanism from source to drain. Tunneling is not impeded by the lack of a physical connection since the virtual junction created by the electric field accomplishes the same function. The device's conductance is determined by the CG voltage, giving it exact control over how it operates. The transistor may be turned on or off and the current flow can be controlled by varying the gate voltage.

4.3 Traps in JL-TFET

Traps, or localized energy states within the semiconductor material, represent significant challenge in JL-TFETs. These traps can capture and release charge carriers, leading to performance degradation, increased leakage currents, and reduced device reliability shown in Fig. 4.3. Common trap types include interface traps, bulk traps, and border traps, each posing unique challenges to device operation. The interface traps are supposed to affect the drain current differently for different devices as per the working physics of the device. In tunnel FETs, these traps mostly occur due to a high electric field at the tunneling interface, the effect of temperature and hot carriers influences them [20]. In TFETs, the drain current is due to band-to-band tunneling (BTBT). Because the BTBT rate depends on the electric field exponentially, interface traps have a greater influence on the drain current on TFETs [21].

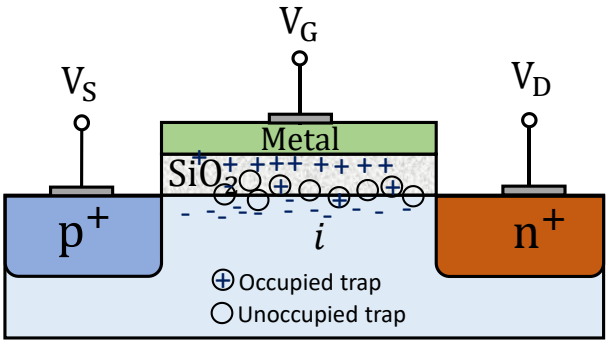

Fig. 4.3: Formation of traps in gate oxide layer of TFET.

The types of interface traps (donor or acceptor), their density (N_{OD}, $N_{OA} = N_O$), and the corresponding trap energy level (E_O) within the forbidden gap also carries a different impact on the drain current. Ehteshamuddin et al. observed that unlike donor-type traps; the acceptor-type traps deteriorate the BTBT mechanism in an n-TFET while it improves the same in a p-TFET [22]. The donor-like and acceptor-like interface traps play a critical role in threshold voltage and therefore drain the current of a device [23].

There are many reports on the effects of interface traps on drain current, random telegraph noise, in the presence of high temperature, etc., a few of them are discussed as follows. Pezzimenti et al concluded that the intrinsic defect concentration may be at least one order of magnitude lower than the epilayer doping concentration to avoid the formation of high-resistive paths for current [24]. Fan et al. observed substantial random telegraph noise (RTN) amplitude for a single acceptor trap near the tunneling junction; moreover, a donor trap originated even more severe impact over a broader region across the channel region, with the help of atomistic 3-D TCAD simulations. Further, they added that thinner equivalent oxide thickness or longer L_{eff}, work function variation, etc are some of the techniques that they found to control RTN amplitude depending on trap-type and the composition/orientation of metal-gate grain [25]. The location of the traps, bias conditions, and trap types impact RTN for both FinFETs and TFETs conferencing devices and circuit characteristics [26]. Ghosh et al. analyzed the effects of traps at higher temperatures for a buried oxide TFET and found that the linearity of the device improved with the rise in temperature [27]. They further added that the Gaussian trap influence is more compared to a uniform trap on the device and circuit performance of the device [28]. Gupta et al. proposed a heterogeneous gate dielectric junctionless-TFET (HD JL-TFET) that improved the transconductance, linearity, and distortion as compared with the conventional JL-TFET [29]. Huang et al., reported with positive-bias

and hot-carrier (HC) stress experiments and TCAD simulation, that the drain current degradation is mainly induced by the interface traps and/or oxide charge located above the tunneling region, which eventually reduces the tunneling field and tunneling current. The interface traps primarily encourage the degradation in transconductance, while the

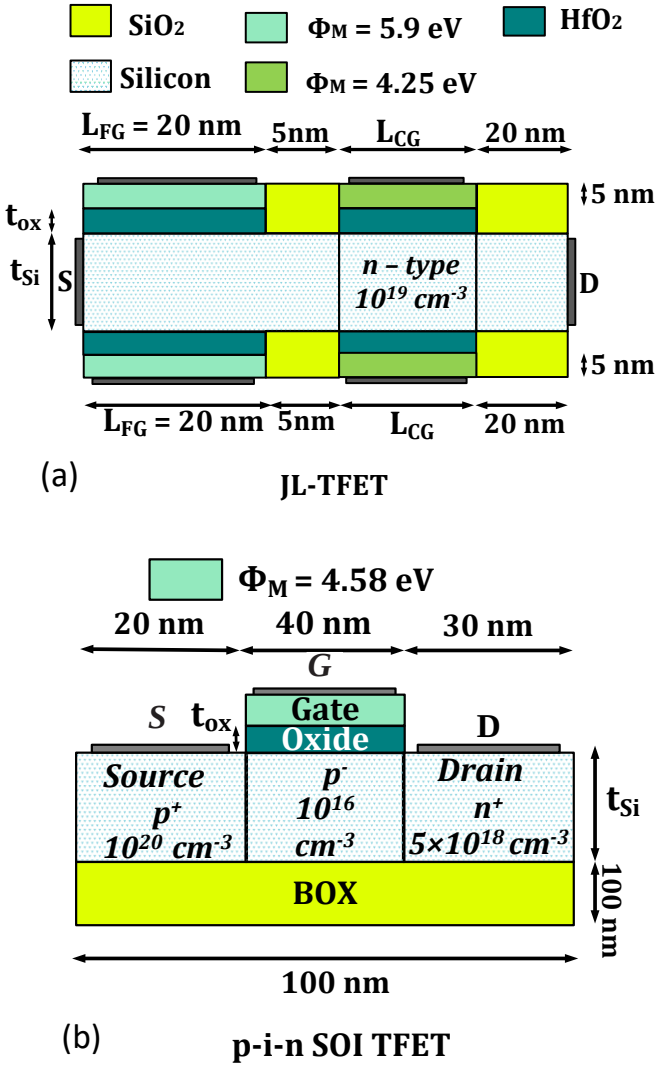

Fig. 4.4: Schematic of (a) JL-TFET and (b) p-i-n SOI-TFET.

oxide charge is responsible for a threshold-voltage shift in TFETs. Further, they added that the interface-trap generation is dominant with positive-bias stress, and the oxide-charge formation is vital under an HC stress in n-TFETs [30]. In conventional TFETs, high concentrations of acceptor-like interface traps suppress device ambipolarity, thus lowering the OFF-state current. With an optimized TFETs, namely, advanced $InAs$-based nanowire (NW) TFETs with Al_2O_3 as the high-κ gate insulator, they proposed

that the effects of interface traps can be reduced to an acceptable value [31]. Pandey et al., investigated the effect of a single charge trap random telegraph noise (RTN)-induced degradation in III–V heterojunction tunnel FET (HTFET)-based SRAM, which exhibits significant energy/performance enhancements even in the presence of RTN. To be specific, HTFET-based SRAM provided 48X lower read access delay and 1.5X reduced power consumption over Si-FinFET ST SRAM operating at their respective minimum supply voltages [32]. Sant et al., verified both theoretically and experimentally that the trap density at the semiconductor-oxide interface has to be suppressed to achieve a sub-thermal SS, eg., for a sub-thermal SS, the density of interface traps density, $D_{IT} \leq 10^{12}\ cm^{-2}eV^{-1}$ [33]. Conventional MOSFET and TFETs follow the same trend for threshold voltage shift and subthreshold swing degradation induced by interface traps, however, impacts on I_{ON} are different because of different conduction. N-type TFET is intrinsically more immune to V_{TH} shift induced by acceptor/donor interface traps than an n-type MOSFET [20].

Therefore, it is of utmost importance to know the effect of traps on JL-TFET at high temperatures that are not reported to the best of our knowledge. Moreover, both junctionless transistors and TFET are advantageous for low-power applications. It would be interesting to know if JL-TFET is opportunistic at a higher temperature.

4.4 Device Simulation and Calibration

Fig. 4.4(a) shows the 2-D schematic of the JL-TFET architecture with a highly doped N-type Concentration of $1 \times 10^{19}\ cm^{-3}$. The JL-TFET has a channel length, $L_{CG} = 20\ nm$, and height $T_{Si} = 10\ nm$. The gate dielectric (HfO_2) thickness is taken as $T_{OX} = 2\ nm$ in between metal gate contact and channel to get the optimized results of the device [34–36]. The FG is set to 0 V. This choice is made to establish a consistent reference point for the device operation, ensuring that the modulation of the electric field and the formation of the virtual p-type area are controlled solely by the CG. The separation between the lateral front gate (L_{FG}) and lateral control gate (L_{CG}) was determined based on physical criteria such as electrostatic control and device stability. A separation of 5 nm was selected to ensure effective modulation of the channel, avoiding interference between the gates. This design was validated through the I_{DS}-V_{GS} characteristics, as shown in Fig. 4.4(a), which demonstrated optimal current conduction and stable threshold voltage (V_{TH}). We have used the optimized value for this from Akaram and Ghosh's published article [36].

Additionally, the chosen separation minimized short-channel effects, reducing drain-induced barrier lowering (DIBL) and maintaining a reliable V_{TH}. The reduced parasitic capacitances and overlap capacitance between the L_{FG} and L_{CG} contributed to improved high-frequency performance, while minimizing fringing effects.

Reducing the separation below 5 nm would introduce significant fabrication challenges. These include increased difficulty in achieving precise lithography and alignment, leading to potential gate overlap and unwanted coupling effects. The smaller separation could also result in higher parasitic capacitances, adversely affecting the device's high-frequency and switching performance.

Fig. 4.4(b) the conventional p-i-n SOI-TFET structure with the same dimension is used as in the case of JL-TFET with a single gate over the channel region with a metal workfunction $\varphi_M = 4.58\ eV$. This work function has been used to match the V_{TH} of both devices at room temperature. The threshold voltage is measured using the constant current method at a constant drain current $I_D = 1 \times 10^{-7}$ A/ µm. For the p-i-n SOI-TFET the doping concentrations in the source (p^+-type), channel (p^-), and

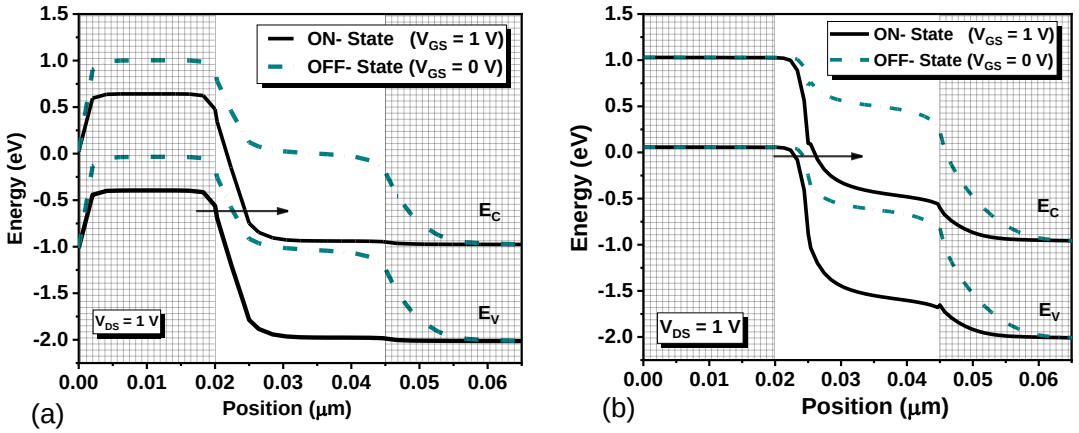

Fig. 4.5: Energy band diagram of (a) JL-TFET and (b) p-i-n SOI TFET at a fixed drain bias $V_{DS} = 1V$, in the ON-state ($V_{GS} = 1V$) and OFF-state ($V_{GS} = 0V$) at T=300K.

drain (n^+-type) regions are $1 \times 10^{20}\ cm^{-3}$, $1 \times 10^{16}\ cm^{-3}$, and $5 \times 10^{18}\ cm^{-3}$ respectively as mentioned in [37] for best performance. The energy band diagram for JL-TFET is shown in Fig. 4.5(a) at a constant drain bias $V_{DS} = 1V$ for both ON-states ($V_{GS} = 1V$) and OFF-state ($V_{GS} = 0V$). It has been observed that a band-to-band tunneling path is forming while input bias is changing from $V_{GS} = 0V$ to $V_{GS} = 1V$.

All simulations are carried out using Sentaurus TCAD Version R-2020.09-SP1 by Synopsys Inc. [38]. The simulation set-up has been calibrated with the transfer

characteristics of JL-TFET shown in Fig. 4.6 [36]. The propagation of errors from the published simulation to the presented data was insignificant. Based on the sensitivity analysis performed, the error percentage is estimated to be within 2-14%, mainly due to differences in model assumptions and material parameters. High doping concentrations in the substrate enable the bandgap narrowing (BGN) model. Because of the high impurity atom inside the channel, in the recombination part, Shockley-Read-Hall (SRH) model is

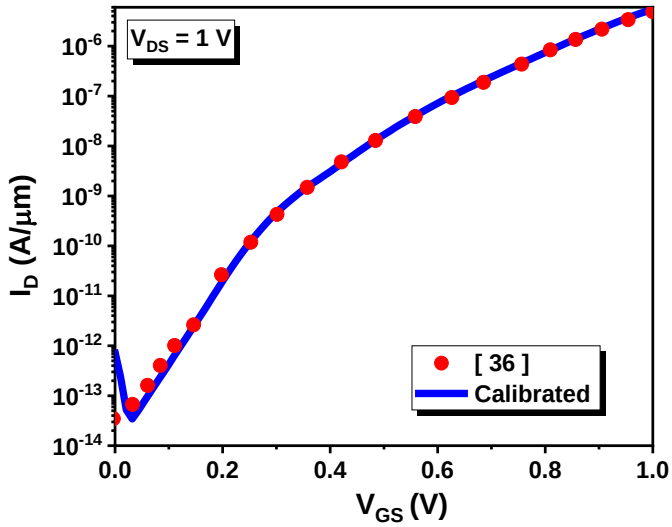

Fig. 4.6: Calibration of the simulation set-up with simulation dataset [36] for gate length $L_{GC} = 20\ nm$, thickness $T_{Si} = 5nm$, Oxide (HfO_2) thickness $T_{OX} = 2\ nm$ and doping n-type concentration of $1 \times 10^{19}\ cm^{-3}$.

used. Along with the SRH effect, recombination of the carrier is also temperature-dependent [39]. The performance of the TFET has been investigated at varying temperatures from analog design perspectives. As the gate bias increases beyond the

Table 4.1: Parameter of nonlocal path band-to-band tunneling

Symbol	Parameter Name	Calibrated Value
A	A_{path}	$2.6 \times 10^6 cm^{-3}s^{-1}$
B	B_{path}	$4.2 \times 10^6 Vcm^{-1}$
D	D_{path}	$-0.45\ eV$
ε_{op}	P_{path}	$0.037\ eV$

threshold voltage, tunneling of the mobile carriers increases, so drain current increases exponentially. The nonlocal band-to-band tunneling (BTBT) model is used for the tunneling of carriers. Calibration of the simulated dataset is traced by changing A_{path}, B_{path} and D_{path} in the parameter section of the silicon substrate as shown in Table 4.1.

4.5 DC and Analog/RF Performance of JL-TFET

From Table 4.1, it is noted that the ON-state current of the device increases with temperature. The ON-OFF current ratio (I_{ON}/I_{OFF}) for both the devices is comparable at high temperatures. It is observed that the OFF-state current of the JL-TFET also increases more with temperature than p-i-n SOI-FET as evident from Table 4.1. To analyse the V_{TH} variation with an increase in T, firstly, we matched the threshold voltage for both devices at room temperature by changing the metal workfunction in the p-i-n SOI-TFET. Metal workfunction $\varphi_M = 4.58\,eV$ for the gate contact material of p-i-n SOI-TFET gives a perfect match of the threshold voltage $V_{TH} = 0.56V$ at room temperature. Fig. 4.7 shows the fluctuation in threshold voltage with the temperature at a fixed drain-to-source bias, $V_{DS} = 1V$, the threshold voltage for both devices decreases at higher temperatures.

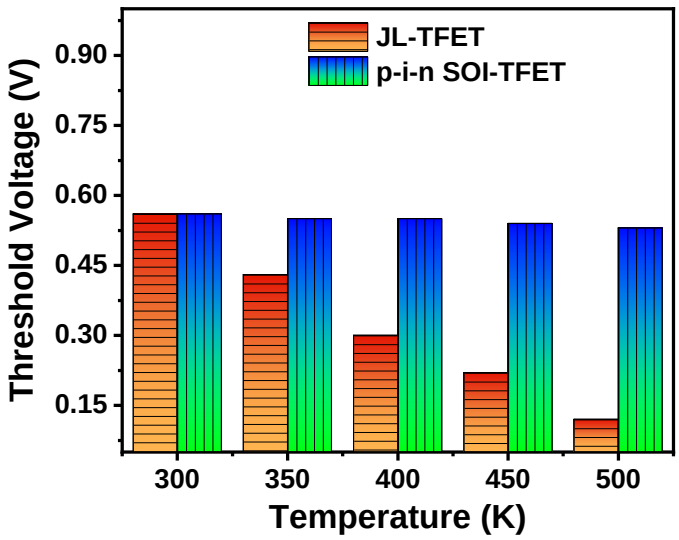

Fig. 4.7: Threshold Voltage with Temperature for JL-TFET and p-i-n SOI-TFET for $T_{OX} = 2nm$, $L_{CG} = 20nm$ and $V_{DS} = 1V$.

The Subthreshold Swing (SS) another important parameter, which convey the device's switching speed is expressed as

$$SS = \partial V_{GS}/\partial(\log_{10} I_D) \tag{4.1}$$

Transconductance ($G_M = \partial I_D/\partial V_{GS}$) is extracted from the transfer characteristics and plotted in Fig. 4.8(a) which is a significant metric for analog circuit design. The transconductance of the device describes how well the amplification can be performed for circuit applications. The transconductance of JL-TFET increases with temperature as in the conventional TFET.

For better performance of the device, total gate capacitance (C_{GG}) of the device must be less, which affects the cut-off frequency of the device. Fig. 4.8(b) describes the total gate capacitance (C_{GG}) variation with temperature. f_T of the device is explicate as

$$f_T = \frac{G_M}{2\pi(C_{GS}+C_{GD})} = \frac{G_M}{2\pi C_{GG}} \tag{4.2}$$

f_T is a function of C_{GS} and C_{GD}, which are also dependent on temperature. For TFETs,

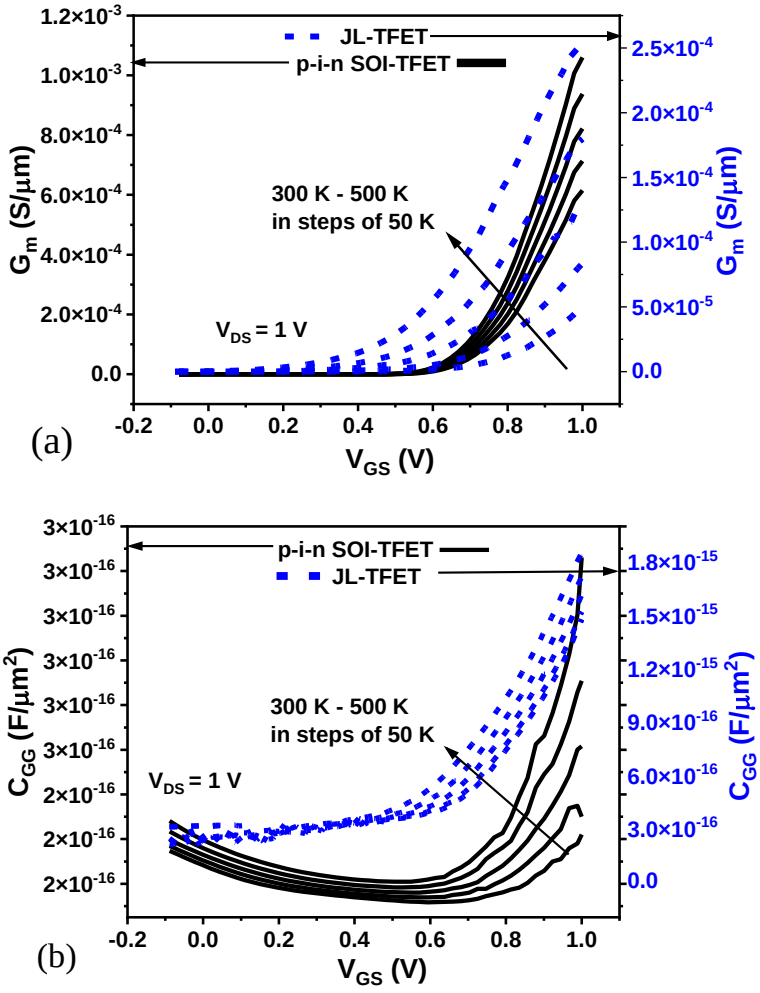

Fig. 4.8: (a) G_M (b) C_{GG} Variation with Temperature at fixed $V_{DS} = 1V$, $L_{CG} = 20\,nm$, $T_{Si} = 10\,nm$, $T_{OX} = 2\,nm$.

C_{GD}has Miller capacitance, which means it acts like parasitic capacitance when get bias is low and at high V_{GS} it behaves like an inversion capacitance. Cut-off frequency for both the devices for temperature variation is shown in Fig. 4.9(a).

All the performance Figure of Merit (FOM) are calculated using input frequency of 1MHz. The gain bandwidth product of the device at DC gain 10 unit is defined as

$$GBW = \frac{G_M}{2\pi \times 10 \times C_{GD}} \tag{4.3}$$

The GBW product that has maximum values of 2.8 MHz and 2.1 GHz are observed for JL-TFET and p-i-n TFET respectively as seen in Fig. 4.9(b).

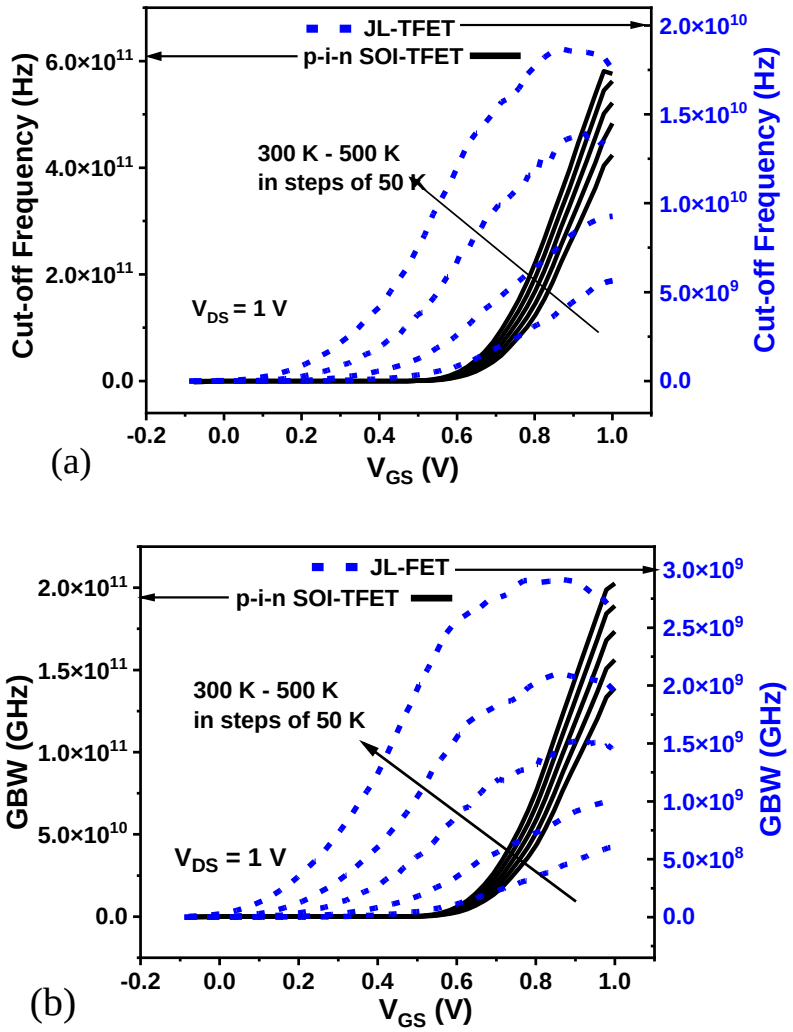

Fig. 4.9: (a)f_T (b) GBW vs gate bias voltage for both devices at $V_{DS} = 1V$, $L_{CG} = 20\,nm$, $T_{Si} = 10\,nm, T_{OX} = 2\,nm$.

4.6 High-temperature Performance of JL-TFET

TFET was found to be more resistant to V_{TH} roll off with an increase in temperature.

While the temperature dependency is feeble in the BTBT-dominated area, it is more in the low electric field range because of the strong temperature dependency of SRH generation–recombination [40]. On the other hand, junctionless transistors show high-temperature advantages in terms of lesser I_{ON}/I_{OFF} degradation with temperature [41]. Because JL-TFET is studied by many authors as advantages over TFET in terms of a) excellent ON-OFF characteristics b) lower subthreshold swing and better switching performance [36]. In addition, that they reported JL-TFET is relatively easy to fabricate, so it would be interesting to see the high-temperature performances of the device in comparison to p-i-n SOI-TFET.

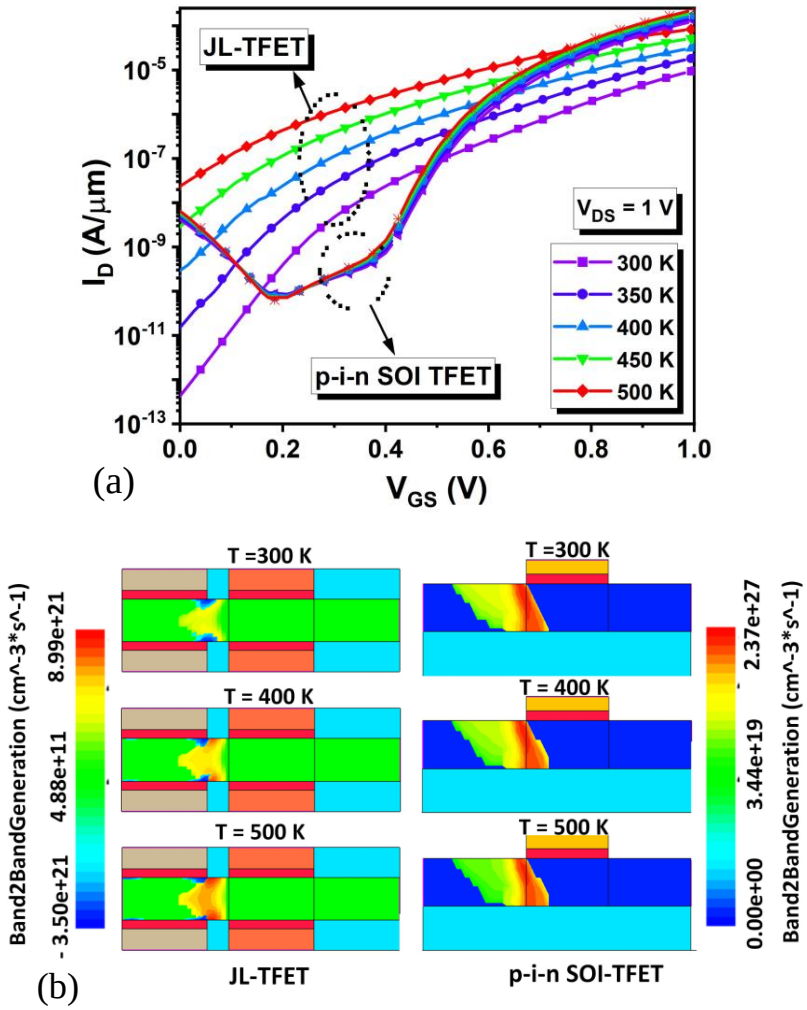

Fig. 4.10: (a)Transfer characteristics with temperature for JL-TFET and p-i-n SOI-TFET at $V_{DS} = 1V$ $L_{CG} = 20\ nm$, $T_{Si} = 10\ nm$, $T_{OX} = 2\ nm$ (b) BTBT profile with temperature for both JL-TFET and p-i-n SOI-TFET at $V_{GS} = 1V$ and $V_{DS} = 1V$.

In Fig. 4.10(a) the transfer characteristics are plotted for both the devices by varying the temperature from room temperature (~300K) up to 500K at $V_{DS} = 1V$. It is observed that there is more ON or OFF-current variation with temperature for JL-TFET.

However, JL-TFET still holds better I_{ON}/I_{OFF} till $T{\sim}400K$, after which p-i-n SOI-TFET outperforms. This is because the probability of band-to-band generation is increased more in JL-TFET than in p-i-n SOI-TFET with temperature. For p-i-n SOI-TFET the probability of band-to-band generation is more but less sensitive with temperature as shown in Fig. 4.10(b) and more is explained below.

The current ($|I| = q\int GdV$, where q is the charge of electron and G is generation rate and V is the applied field) is determined by Kane's Model, where G(E) is given by [40]:

$$G(E) = A\frac{E}{\sqrt{E_g}}\exp(-B\,E_g^{\frac{3}{2}}/E) \tag{4.4}$$

Where E = Electric Field, E_g= Band Gap, A, and B are the constant parameter depending on the effective mass of valance and conduction band. We have considered the phonon-assisted tunneling process in our physics model for which A and B can be expressed as

$$A = \frac{g(m_V m_C)^{3/2}(1+2N_{op}){D_{op}}^2(qF_0)^{5/2}}{2^{21/4}h^{5/2}{m_r}^{5/4}\rho\varepsilon_{op}[E_g(300K)+\nabla_C+\nabla_V]^{7/4}} \tag{4.5}$$

$$B = \frac{2^{7/2}\pi{m_r}^{1/2}[E_g(300K)+\nabla_C+\nabla_V]^{3/2}}{3qh} \tag{4.6}$$

The values of constants are directly related to a physical parameter that influences the device's characteristics. After calculating the $m_r$value from the default values while calibrating, we have changed the other parameters to get the expected transfer characteristics with the values shown in Table 4.1. On the other hand, in the non-local BTBT model, the current depends on the bend edge profile along the specified path. In this model, the electric field is locally defined at each mesh point by setting length and permeable permission in the specified region interface within the math section of the s-device [42]. The crystal lattice of the semiconductor material gets expanded and interatomic bonds are broken with the increase in temperature which can be written as

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{(T+\beta)} \tag{4.7}$$

$E_g(0)$= Band gap at 0K, α, and β are constant for the best fit of the experimental data. Reduction of energy bandgap with temperature affects the ON-state current as well as OFF-state current as the tunneling distance is reduced [43]. With an increase in temperature, the number of broken bonds also increases more in n-type semiconductors

than intrinsic type semiconducting material. A p-i-n SOI-TFET needs more thermal energy than n channel JL-TFET. Hence JL-TFET is more temperature sensitive.

The threshold voltage (V_{TH}) is matched for both devices at room temperature by tunning the metal work function of p-i-n SOI-TFET. Metal workfunction $\varphi_M = 4.58\,eV$ of p-i-n SOI-TFET matches the threshold voltage ($V_{TH} = 0.56V$) at room temperature. Table 4.2 shows threshold voltage variation with the temperature at fixed drain-to-source bias, $V_{DS} = 1V$. We have traced the threshold voltage by using the

Table 4.2: Electrical Parameters For Variation in Temperatures of JL-TFET and p-i-n SOI-TFET

Temperature (K)		I_{ON}/I_{OFF} ($\times 10^6$)	V_{TH} (V)	SS (mV/dec)	G_m (mS)	(G_m/I_D)	C_{GG} (fF)	f_T (GHz)	GBW (GHz)
300	JL-TFET	7.18	0.56	56	0.049	14.1	1.4	5.6	0.6
	p-i-n TFET	0.00899	0.56	58	0.61	1478.8	0.23	420	130
350	JL-TFET	3.8	0.43	58	0.083	16.65	1.5	9.2	0.99
	p-i-n TFET	0.00906	0.55	62	0.71	1486.6	0.24	480	150
400	JL-TFET	0.2189	0.30	61	0.12	2119.2	1.6	13	1.4
	p-i-n TFET	0.00922	0.55	73	0.82	1508.5	0.25	520	170
450	JL-TFET	0.03244	0.22	69	0.17	2501.7	1.7	17	1.9
	p-i-n TFET	0.00933	0.54	87	0.93	1526.1	0.26	560	180
500	JL-TFET	0.00613	0.12	123	0.25	2740.8	1.8	22	2.5
	p-i-n TFET	0.00948	0.53	143	1.06	1547.1	0.29	570	200

constant current method ($V_{TH} = V_{GS}\ at\ I_{DS} = 10^{-7}A$). For a p-i-n SOI-TFET, V_{TH} is marginally altered compared to a JL-TFET, where is a good chance; because of lesser reduction of an energy band gap in p-i-n SOI-TFET with temperature as the channel is intrinsic-type which contains a smaller number of mobile charges, than the n-type heavily doped charges and from the band diagram we can see small tunneling width is

present. For a p-i-n TFET channel in intrinsic and drain is n-type, but less doped compared to n-channel JL-TFET. At higher gate voltage, velocity gets saturated, mobility degrades more in p-i-n TFET than JL-TFET). For the same reason, subthreshold swing [$SS = \partial V_{GS}/\partial(\log_{10} I_D)$] is lesser temperature sensitive for p-i-n SOI-TFET than a JL-TFET as shown in Table 4.2.

Transconductance ($G_m = \partial I_D/\partial V_{GS}$) is slightly better for p-i-n SOI-TFET. Moreover, G_m of p-i-n SOI-TFET is lesser sensitive to temperature than the other device. However, G_m/I_D is better for a JL-TFET at a higher temperature. The cut-off frequency of the device, $f_T = G_m/2\pi C_{GG}$, where C_{GG} is the total gate capacitance is better for p-i-n SOI-TFET and lesser sensitive to temperature than JL-TFET. For the same reason, the gain bandwidth product of the device, $GBW = G_m/2\pi \times 10 \times C_{GD}$ at DC gain of 10 units, is better for p-i-n SOI-TFET even at a higher temperature than JL-TFET. Overall, from Table 4.2, it can be concluded that a) I_{ON}/I_{OFF} the ratio is comparatively higher for JL-TFET till $T = 400K$, after which the p-i-n SOI TFET has moderately better value b) p-i-n SOI TFET has better transconductance from low-high temperatures, c) there is more threshold voltage variation with T for JL-TFET, d) JL-TFET offers relatively better subthreshold swing compared to p-i-n SOI TFET, e) p-i-n SOI TFET has better gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}), cut-off frequency (f_T) and gain bandwidth product (GBW) performance than JL-TFET. In conclusion, JL-TFET is a better fit for low-power applications and p-i-n SOI TFET is more profitable for high-speed applications compared to a JL-TFET.

4.7 Improvement of Ambipolar Behavior in a JL-TFET

In this section, two different gate materials in the control gate part of different work function φ_{M1} and φ_{M2} are considered, where φ_{M1} is kept fixed to 4.25 eV, and φ_{M2} is varied to study the transfer characteristics of JL-TFET for different temperatures. The increase in the work function in the channel drain region increases the tunnel length for both the ON-state and OFF-state current. Thus, increasing φ_{M2}, slightly decreases the current as tunnel length increases. There is an increase in ambipolar current as φ_{M2} is increased which is shown in Fig. 4.11(b) through a BTBT contour for $\varphi_{M2} = 4$ eV and $\varphi_{M2} = 4.25$ eV at $V_{GS} = -0.1\,V$. Decreasing the value of φ_{M2}, increases the OFF-state current which is the leakage current.

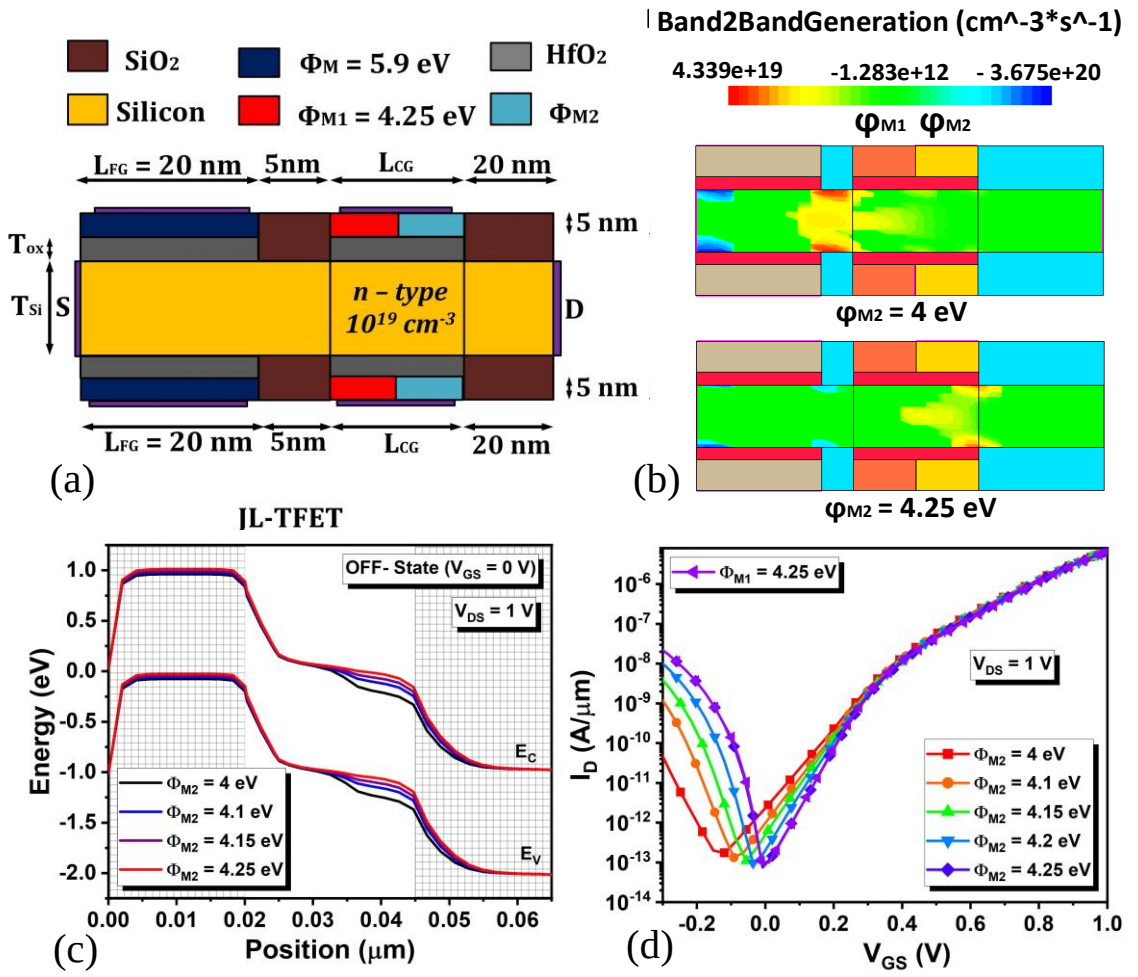

Fig. 4.11: (a) Schematic diagram for dual gate material JL-TFET, (b) BTBT contour for the dual control gate material $\varphi_{M2} = 4$ eV and $\varphi_{M2} = 4.25$ eV at $V_{GS} = -0.1V$, (c) Energy Band diagram variation of φ_{M2} at $V_{GS} = 0V$ (OFF-State condition), (d) Transfer characteristics with work function of the material near the fixed gate at T=300K.

This increase in leakage current is due to the shift in energy band in the upward direction that leads to increasing tunnel length as shown in Fig. 4.11(c). At the super threshold region, there is no change in ON-state current (Fig. 4.11(d)) because the energy band remains fixed without any shift in the upward and downward direction in the source channel region. As the V_{GS} decreases, the energy band of the channel region shifts upward due to which the electrons from the valence band of the channel tunnel to the conduction band edge of the drain, thereby increasing the ambipolarity [3, 44]. So, for better performance ambipolar behavior can be reduced by shifting the energy band of the channel/drain region to a downward direction which can be done by reducing the value of the work function. The work functions in the dual material gate JL-TFET can be optimized for the improvement of I_{ON}, which is a drawback for the device.

4.8 Reliability Issues in JL-TFET

The effect of HCI on JL-TFET's long-term dependability, highlighting probable degradation pathways and suggesting preventative measures is analyzed in this section. Under various negative bias situations, NBTI-induced performance deterioration is investigated, offering insights into the stability of V_{TH} and general device properties. In addition, the study evaluates JL-TFETs' immunity to ionizing radiation, which is important for applications in radiation-prone areas. The findings provide valuable insights for improving the reliability of semiconductor devices in future technologies. They emphasize key considerations when designing and selecting materials to enhance the durability of JL-TFETs against challenges like HCI, NBTI, and radiation.

4.8.1 Hot Carrier Injection (HCI)

In an n-type JL-TFET, due to accumulation, a high-field spacer charge region develops at the oxide-semiconductor interface near the channel drain. Electrons then drift towards the drain region, gaining energy and getting accelerated by the electric field, becoming hot. These hot carriers may generate extra electron–hole pairs in the channel, especially in the depletion region of the drain above the pinch-off region[45–47]. The generated hot electrons are injected from the Silicon to the HfO_2 region, perpendicularly to the oxide region due to HCI. As depicted in Fig. 4.12(a), the disparity in drain current (at room temperature) between JL-TFET with the HCI model and without the HCI model is more pronounced compared to the p-i-n SOI-TFET with the HCI model and without it. This occurs because SRH-recombination increases by a factor of 4.2 in the HCI phenomenon in JL-TFET, as opposed to p-i-n SOI-TFET.

In a JL-TFET, since there is no p-n junction in the source-channel-drain region and the entire channel region acts as the conducting channel, the HCI phenomenon initiates whenever electrons tunnel through the energy barrier in that specific region (as illustrated in Fig. 4.12(b)). This results in a higher number of electron-hole pairs (EHP), leading to one order more SRH-recombination in JL-TFET compared to p-i-n SOI-TFET, as shown in Fig. 4.12(c). In p-i-n SOI-TFET, the HCI phenomenon occurs only in the channel drain region, and the EHP generation is compensated by the intrinsic region.

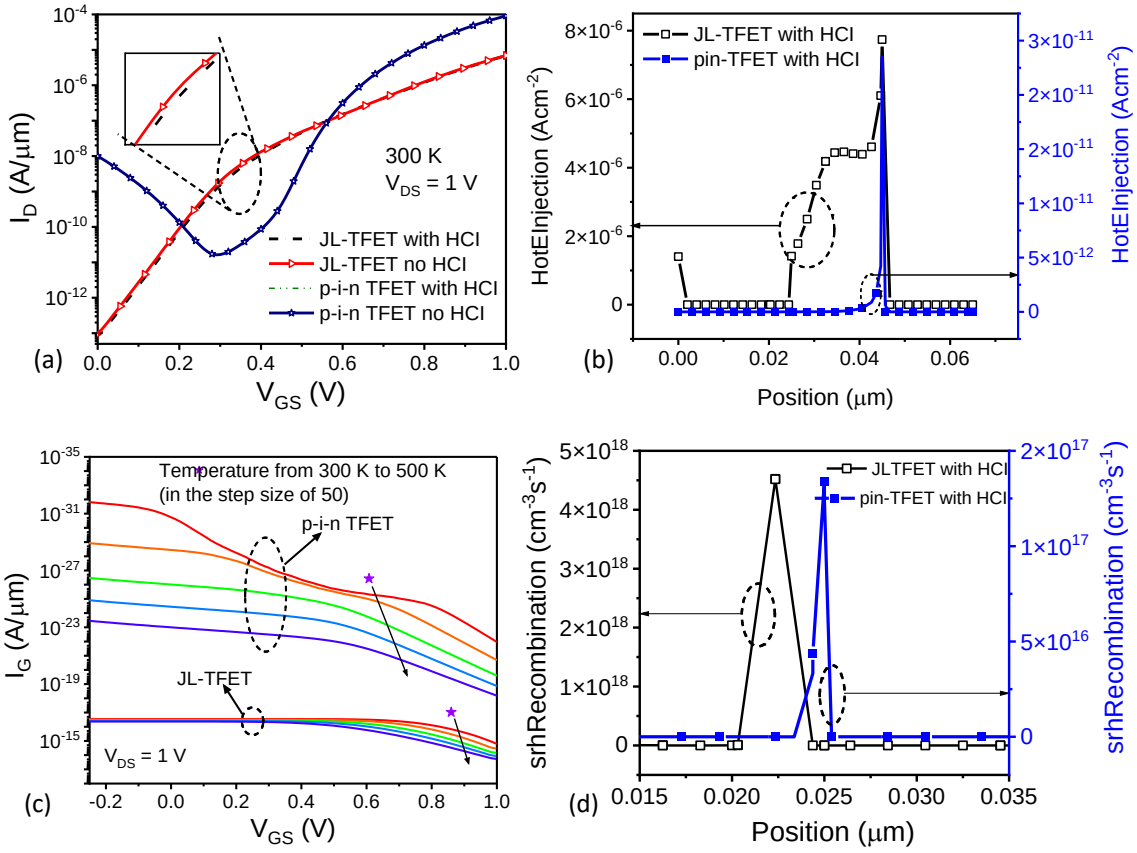

Fig. 4.12: (a) Transfer characteristics curve for both p-i-n TFET and JL-TFET for 300K (b) Hot electron injection curve for both p-i-n TFET and JL-TFET for 300K (c) Gate leakage characteristics curve for both p-i-n TFET and JL-TFET with variation in temperature from 300K to 500K (d) SRH-Recombination curve for both p-i-n TFET and JL-TFET for 300K.

Hot electrons injected into the gate oxide near the drain region contribute to a gate current (I_G), as depicted in Fig. 4.12(d). The total hot-carrier injection current is calculated from the following equation [48]:

$$I_g = \frac{2qAg_v}{4} \int P_{ins} \int_0^{\infty} g(\varepsilon) v(\varepsilon) f(\varepsilon) \left(\int_0^1 \Gamma \left(\varepsilon - \frac{h^3 g(\varepsilon) v(\varepsilon) x}{8\pi m_{ins}} \right) dx \right) d\varepsilon ds \qquad (4.8)$$

The Spherical Harmonics Expansion (SHE) distribution hot-carrier injection model is used in the article to describe a model for measuring hot-carrier injection current in a semiconductor device. The model includes several parameters: the transmission coefficient (Γ), which is derived from the WKB approximation with image-potential barrier-lowering; the dimensionless prefactor (A = 1, by default); the valley degeneracy factor (g_v); the probability of electrons moving without scattering (P_{ins}); the density-of-states per valley per spin (g); the magnitude of electron velocity (v); and the effective mass of the insulator (m_{ins}). The nonequilibrium energy distribution, $f(\varepsilon)$ is obtained

from the lowest-order Spherical Harmonics Expansion of the semiclassical Boltzmann transport equation. This cutting-edge method improves our comprehension and modeling of semiconductor device behavior by offering a more realistic depiction of the HCI phenomenon.

This gate current can lead to the formation of interface traps, as the injected electrons become trapped in the oxide region on the drain side. The generated gate current exhibits a 4-order difference in the case of p-i-n SOI-TFET and a 1-order difference over the temperature range from 300K to 500K. Due to increase in temperature from 300 K to 500 K the mobility of carrier conduction increases which dominates the effect of hot carrier injection (HCI) where the flow of minority carriers is not affected hence band-to-band generation increases with HCI effect in case of increasing temperature. This results in the formation of interface states, while the generated holes tend to move toward the substrate. Hot electrons are more probable, as electrons more readily gain an electric field due to the small value of effective mass, and the energy barrier for holes is larger (approximately 3.4eV) compared to the energy barrier for electrons (approximately 1.5 eV). As a result, the surface potential in the drain region is altered, leading to the degradation of JL-TFET characteristics. The generation of EHPs at the source/channel junction increases with temperature in the presence of the HCI phenomenon.

4.8.2 Negative Bias Temperature Instability (NBTI)

Transistors operating in inversion mode exhibit the NBTI phenomenon, in a JL-TFET is related to the electric field in the channel region, it is completely dependent on the biasing conditions. An electrochemical reaction occurs in the vicinity of the silicon-gate oxide interface due to the high electrical field across the oxide and the high temperature. Positive charges eventually become trapped at oxide-semiconductor interface beneath a JL-TFET control gate.

Fig. 4.13 illustrates how the maximum and the average trap density increase with time. Unlike in a typical semiconductor, these positive charges only partially neutralize the negative gate voltage and do not contribute to conduction across the channel. Two distinct processes are associated with Bias Temperature Instability (BTI).

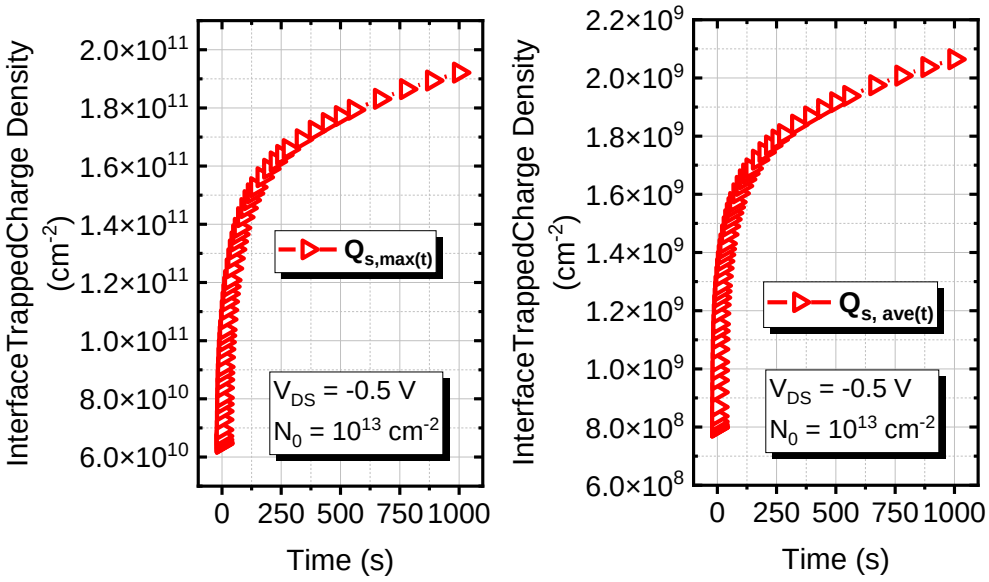

Fig. 4.13: Interface trapped charge density with time under negative bias condition.

One process involves the direct rupture of Si-H bonds in the oxide. Interface traps are generated when a p-type JL-TFET transistor is biased in inversion mode, caused by the breakdown of Si-H bonds along the silicon-oxide interface.

The capture rates for electrons and holes are given by [49]:

$$c_C^n = \sigma_n v_{th}^n n \exp[-H(E_i - E_C)/kT] \tag{4.9}$$

$$c_V^p = \sigma_p v_{th}^p p \exp[-H(E_V - E_i)/kT] \tag{4.10}$$

and the electron and hole emission rates given by

$$e_C^n = \sigma_n v_{th}^n N_C \exp[-H(E_C - E_i)/kT] \tag{4.11}$$

$$e_V^p = \sigma_p v_{th}^p N_V \exp[-H(E_i - E_V)/kT] \tag{4.12}$$

Where σ_n and σ_p are the capture cross-section of electron and hole respectively (by default $\sigma_n = 1.08 \times 10^{-15}\,cm^2$ and $\sigma_p = 1.24 \times 10^{-14} cm^2$). v_{th}^n and v_{th}^p are the thermal velocity of electron and hole (by default $v_{th}^n = 1.5 \times 10^7\,cm/s$ and $v_{th}^p = 1.2 \times 10^7\,cm/s$).

Trapping is the second incident that leads to BTI. Apart from the creation of interface states, holes coming from the p-type JL-TFET channel fill certain pre-existing traps in the dielectric bulk. The trapped charges are released throughout milliseconds to hours upon removal of the gate voltage. The V_{TH} degradation with time under negative

bias conditions shown in Fig. 4.14. As transistors have become smaller, the problem has been exacerbated due to reduced influence averaging across a smaller gate region [50, 51]. Furthermore, a recent study conducted between 300K and 500K revealed a decrease in NBTI with rising temperatures. However, the exact behavior of this impact at elevated temperatures is not yet clear. By expanding the study to include different

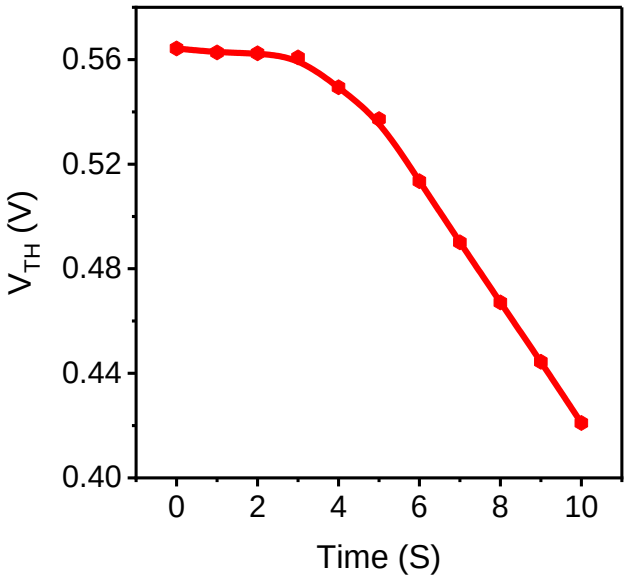

Fig. 4.14: V_{TH} degradation under negative bias conditions.

temperature scenarios, researchers hope to get more detailed information about how NBTI appears in JL-TFETs. This is essential to understanding the fundamental processes. Controlling device dependability and performance in practical situations where temperature variations are unavoidable. The wider temperature range makes it easier to analyze NBTI's effects on JL-TFETs in detail, providing important information that is essential for improving device design and reducing reliability issues. Overall, this analysis has the potential to improve the robustness and practical application of JL-TFET-based semiconductor technologies in various operating situations.

4.8.3 Radiation Effects

Ionizing radiation is strong enough to break electron bonds within atoms, creating free radicals and charged particles. This essentially introduces defects in the oxide region of the device, which essentially affects the reliability of the device [52–54]. Changes in the transistor's behavior and fluctuations in the V_{TH} can occur due to charge trapping in the gate oxide [29, 52]. Bulk damage can also happen, which affects carrier mobility and overall device performance. Bulk damage is induced by atoms

moving around in the semiconductor crystal lattice [55]. Thoroughly assessing the radiation impact on JL-TFET is essential to ensure the durability and reliability of electronic systems in applications where radiation is a significant concern, such as high-energy physics experiments or aerospace applications. Radiation-induced EHP

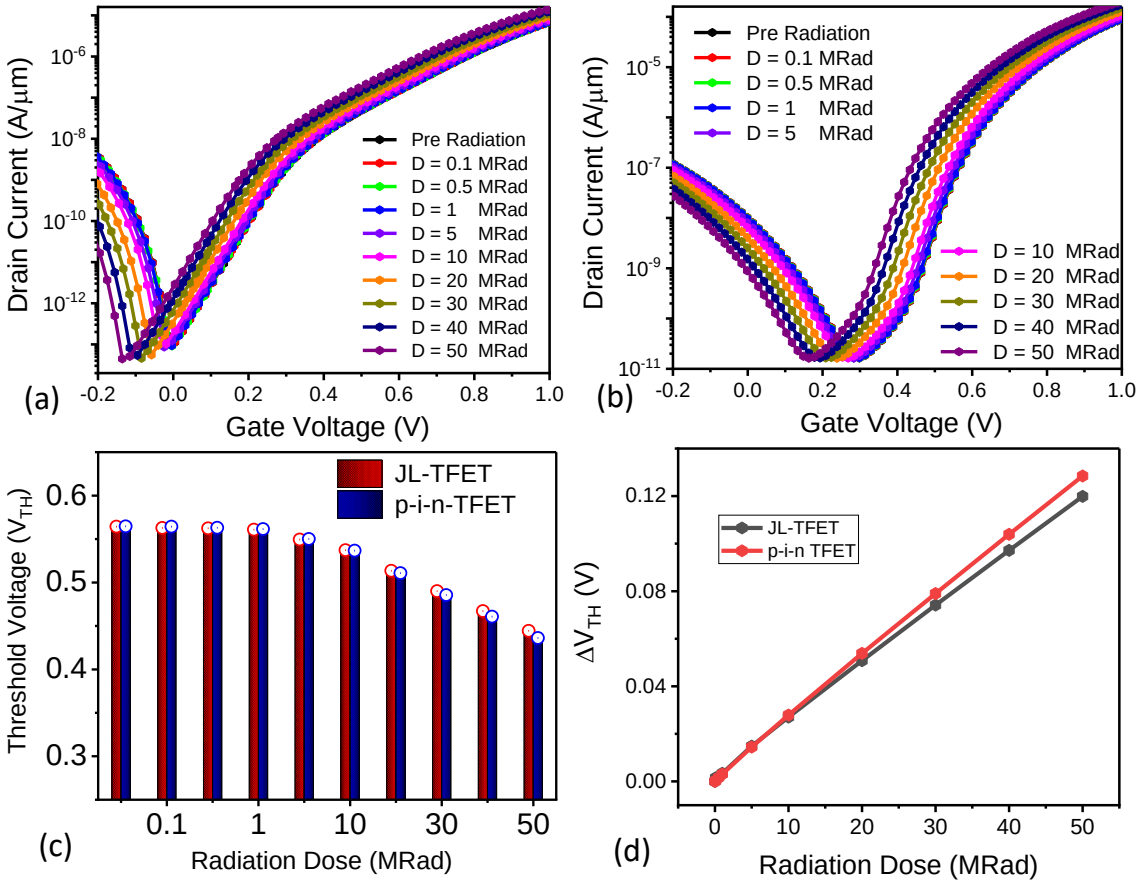

Fig. 4.15: Transfer characteristics of (a) JL-TFET and (b) p-i-n SOI-TFET at $V_{DS} = 1V$ (c) V_{TH} and (d) ΔV_{TH} of JL-TFET and p-i-n SOI-TFET with TID.

formation can have cumulative effects from prolonged exposure to ionizing radiation. This cumulative effect (commonly referred to as TID), quantifies the total amount of energy deposited in the substance. Fig. 4.15(a) and Fig. 4.15(b) show the transfer characteristics of the JL-TFET and p-i-n SOI-TFET with the inclusion of radiation dose. The calibration and fitting characteristics of the device were carefully determined by utilizing information from a carefully calibrated predecessor [56]. When the transfer characteristics are examined, an immediate trend becomes apparent: as the radiation dose rises, the device's OFF-state current degrades more than its ON-state current. The rate of change of the dose with respect to time, or dR/dt, indicates how quickly the JL-TFET is exposed to radiation as the radiation dosage increases over time. This

deterioration has a major effect on critical parameters, such as the V_{TH}, which presents difficulties for analog circuit applications and emphasizes the need for radiation-hardened semiconductor designs [57]. The decline in the V_{TH} for both devices with radiation dose is compared and illustrated in Fig. 4.15(c). The equation given below

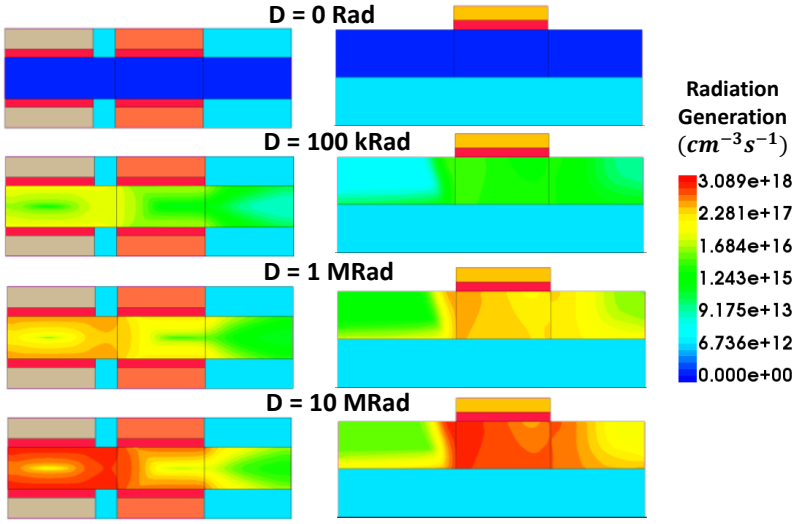

Fig. 4.16: Radiation generation profile of JL-TFET and p-i-n SOI-TFET with radiation.

connects the maximum permitted gate leakage current in a JL-TFET to the rate of radiation-induced defect development. Before radiation exposure, the V_{TH} of JL-TFET was 0.54 V. After exposure to a radiation dose of 50 Mrad, the V_{TH} degraded to 0.44 V, similar to that of the V_{TH} of the p-i-n SOI-TFET. The shift in the V_{TH} with TID is depicted in Fig. 4.15(d). The gate oxide layer of the device is primarily affected by ionizing radiation, which can result in gate oxide damage, increased leakage currents, the creation of interface states, and subsequent charge trapping. The performance of the JL-TFET may deteriorate as a result of these influences. A mathematical model is employed to extract the number of traps at the interface and within the bulk oxide region based on the maximum EHP generation profile at a specific radiation dosage over a fixed period.

The EHP generation profile for both JL-TFET and p-i-n SOI-TFET with TID is illustrated in Fig. 4.16. The following relationship is used to extract the EHP generation with radiation exposure.

$$G_{max} = g_0 \frac{dR}{dt} Y(\vec{E}) \tag{4.13}$$

Where, g_0 is the quantity of EHP produced in a unit volume per unit dose. Radiation

dosage rate $\frac{dR}{dt}$ (rad/s), $Y(\vec{E})$ is the yield function. The values of g_0 is 7.88×10^{12} $rad^{-1}cm^{-3}$, and m = 0.7 (constant value derived from experiment) for γ irradiation, respectively [53]. The mathematical models provided in equations 4.14 and 4.15 for the calibration of N_{it} and N_{ot}, which are based on experimental data in our TCAD

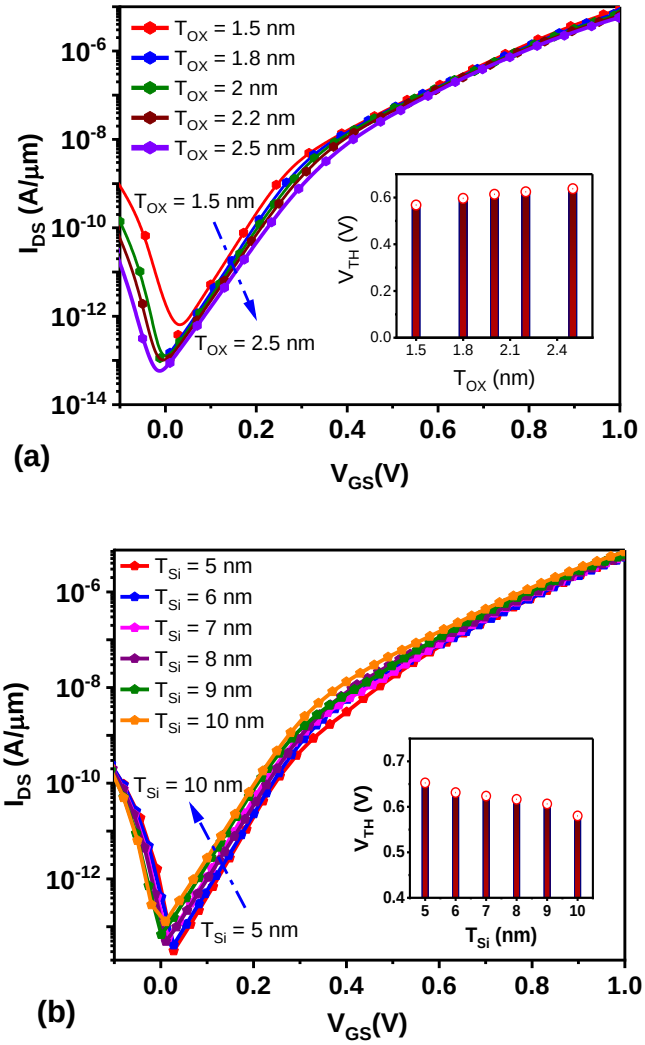

Fig. 4.17: Transfer characteristics of JL-TFET with (a) oxide thickness and (b) substrate thickness for a radiation dose of 1MRad at $V_{DS} = 1V$.

simulator, have also been added. As a result, N_{it} and N_{ot} will change in a more practically significant way, to extract the behavior of the device with TID.

The best-fitted curve from the extracted data of N_{it} follows the general expression:

$$N_{ot} = (1 - a_{ot})G_{TID}t \tag{4.14}$$

$$N_{it} = (1 - a_{it})a_{it}D^{b_{it}} \tag{4.15}$$

Where, a_{it} ($cm^{-2}\cdot rad^{-1}$) and b_{it} (constant) →fitting coefficients, as calculated in [52], G_{TID} → total EHP generation rate due to γ radiation, D→total absorbed dose (rad).

The modulation of the V_{TH} with the process parameters is shown in Fig 4.17 at 1MRad dose. A suitable method to reduce the radiation-induced changes in V_{TH} is to modulate the thickness of the oxide and substrate. This strategy is especially important for radiation-hardened semiconductor devices, to maintain steady performance even under extreme radiation environments. The oxide thickness is crucial because it affects the electric field distribution inside the device.

Similarly, changes in substrate thickness can customize the charge distribution, providing another way to adjust the radiation resistance of the device. Variations in T_{ox} from 1.5 nm to 2.5 nm result in a significant rise in V_{TH} from 0.56 to 0.63, Fig. 4.17(a) demonstrates the influence of T_{ox}on JL-TFET performance. Similar to this, changes in substrate dimensions between 5 and 10 nm cause a decline in V_{TH} from 0.65 to 0.58 plotted in Fig. 4.17(b). When designing JL-TFETs for a given application, it is critical to achieve the ideal dimensions, especially in radiation conditions where accuracy is critical to the device's dependability and functionality. In addition to being a technological difficulty, striking the right balance is essential to guaranteeing the device's reliable operation and ability to withstand difficulties brought on by radiation.

4.8.4 Role of Interface Traps on JL-TFET at High-Temperature

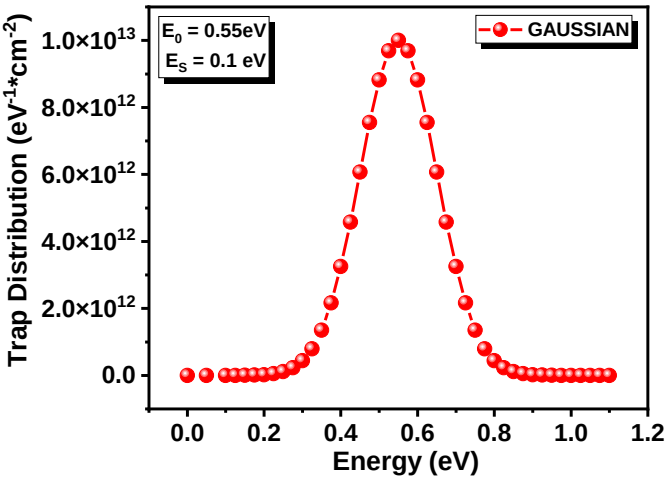

Fig. 4.18: Gaussian distribution trap in the oxide-semiconductor interface.

In a dielectric material like SiO_2, HfO_2, and many more oxides, charges may be trapped in the form of impurities at the interface. The trapped oxide charges arise out of the defects which are caused due to empty atomic valences at the Si-SiO_2 interface causing

charges to get trapped at the interface [58]. In this section, a circumstantial investigation of the role of trap type, trap density concentration, trap energy levels and trap energy width in affecting the characteristics of JL-TFET with HfO_2, high$-k$ gate dielectric is presented.

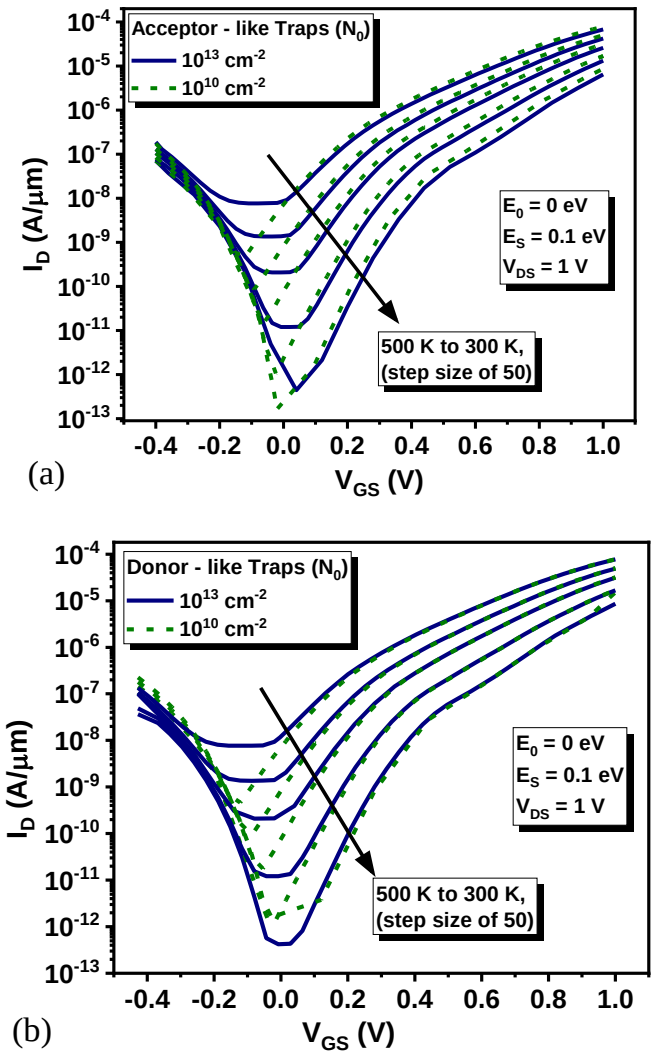

Fig. 4.19: Trap transfer characteristics curve for drain current versus gate-to-source voltage for different peak density concentrations for different temperatures (a) acceptor-like traps, (b) donor-like traps.

In this analysis, the Gaussian trap distribution is selected as it closely follows experimental evidence as compared to uniform and exponential distributions [59], defined mathematically as [42]

$$D_{Gau} = N_0 \, e^{\left(-\frac{(E-E_0)^2}{2E_S^2}\right)} \tag{4.16}$$

where, N_0 is the peak density concentration, E is the variable energy, E_0 is the position

of energy corresponding to peak density concentration, and E_S defines the width of the Gaussian distribution such that if $E = \sqrt{2}\,E_S$ then the concentration of the traps is $1/e$ of the peak density concentration, N_0. Two types of traps are taken into consideration, namely, acceptor-like traps, and donor-like traps. The former type of trap is considered in the upper half of the energy bandgap, while the latter is considered in the lower half of the energy bandgap. We have assumed that the localized interface trap charges are located at Si/HfO_2 interface where the capture cross section σ, $(\sigma_e = \sigma_h)$ is 10^{-14} cm^{-2}. Fig. 4.19 shows the transfer characteristics concerning traps for the increase in temperature, where two interface trap density concentration is taken into consideration

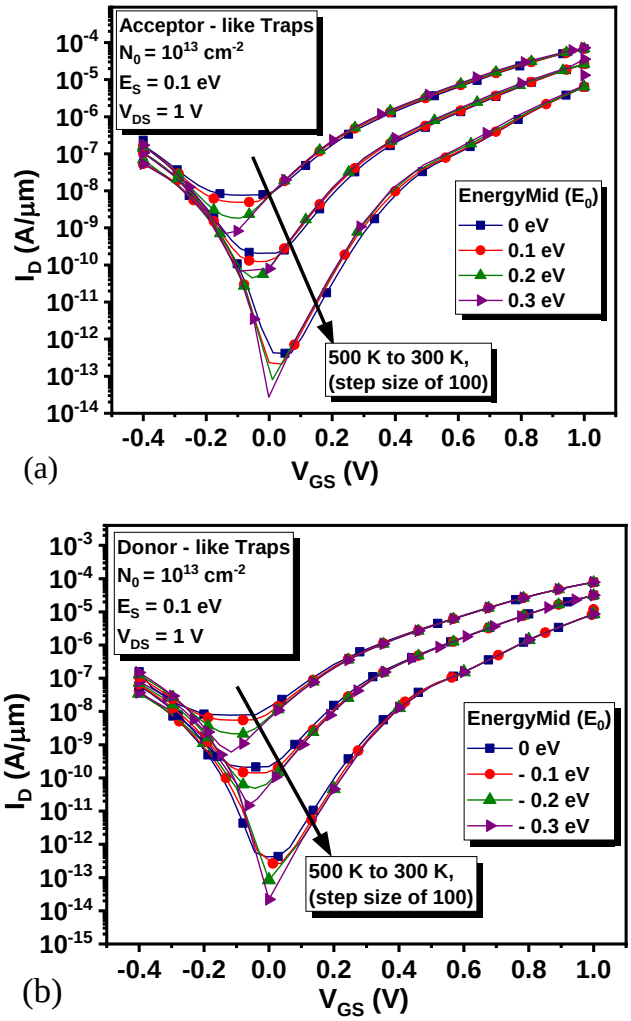

Fig. 4.20: Trap transfer characteristics curve for drain current versus gate-to-source voltage for different variations in Gaussian peak location for different temperatures (a) acceptor-like traps, (b) donor-like traps.

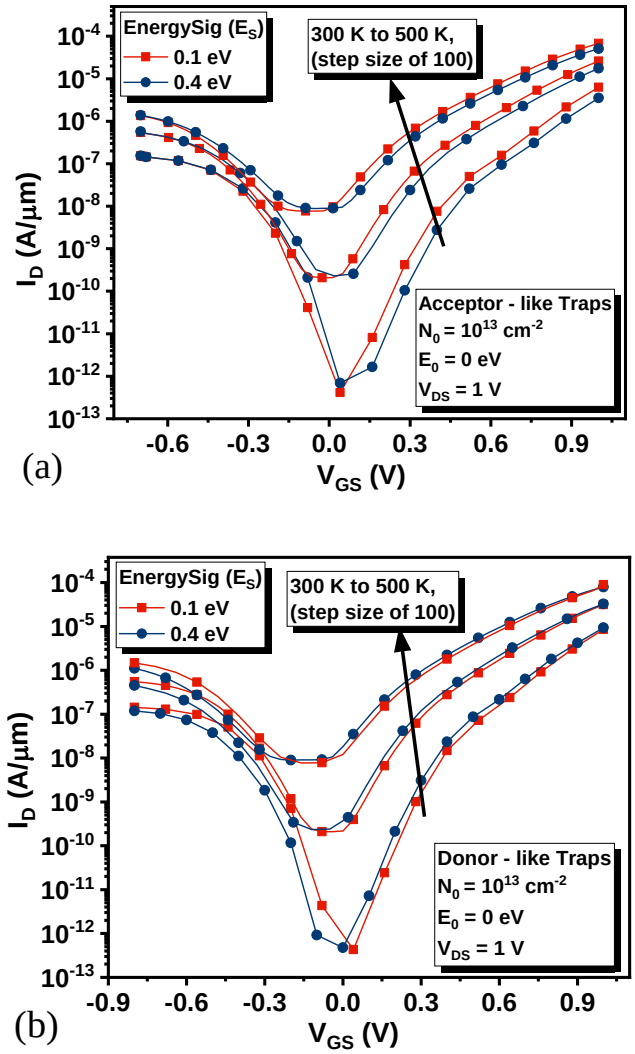

Fig. 4.21: Trap transfer characteristics curve for drain current versus gate-to-source voltage for various standard deviations on Gaussian-like traps for different temperatures (a) acceptor-like traps, (b) donor-like traps.

having maximum trap density concentration $N_0 = 10^{13}\,cm^{-2}$ and minimum trap density concentration of $N_0 = 10^{10}\,cm^{-2}$ for both acceptor-like traps and donor-like traps. The ON-State current and OFF-State current increase as the forbidden gap of the silicon decreases with an increase in temperature [22]. The more the trap concentration, the more the trapping of carriers, and the lower the current for acceptor–like traps. If the dissimilarity of the characteristics among acceptor-like traps and donor-like traps is observed, acceptor-like traps are found to affect the ON-state of the device as opposed to donor-like traps which affect the ambipolar state of the device [24]. However, the fact that both are similar in dominance in the OFF-state is observable from the characteristics.

4.8.5 Effect of Traps Due to Variation in Gaussian Peak Location

The peak position of the Gaussian distribution of traps has great significance in the current characteristics of JL-TFET. The results of these variations for both acceptor-like traps and donor-like traps from deep to shallow levels are shown in Fig. 4.20(a) and 4.20(b), respectively. We assume that the peak density concentration of interface traps such as donor-like traps and acceptor-like traps type is $10^{13}\,cm^{-2}$ where the energy distributions are located between $E_i + 0.3\,eV$ and $E_i - 0.3\,eV$ considering E_i as the reference level for an increase in temperature from 300 K to 500 K. Out of them, the peak position in the deep level at zero gate voltage has the maximum OFF-state current which decreases as we move to the shallow trap levels, whereas the ON-state current remains nearly same for all [60].

4.8.6 Effect of standard deviation on Gaussian-like traps

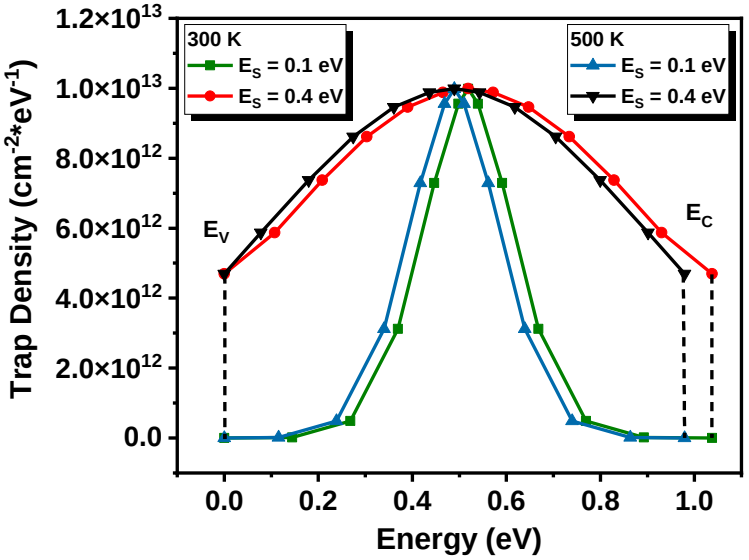

Fig. 4.22: Interface trap density as a function of energy for different standard deviations of the Gaussian distribution at T = 300 K, 500 K.

Fig. 4.21 represents the transfer characteristics due to variation of the standard deviation of Gaussian widths from 0.1 eV to 0.4 eV for temperatures ranging from 300 K to 500 K. Fig. 4.22 shows the Gaussian distributions for different E_S for the two temperatures. The widening of the Gaussian distribution with an increase in E_S shows a high distribution of interface trap density over the energy bandgap. As a result, more carriers have the probability to get trapped, and hence, the current changes. On the other hand, due to the impact of temperature, the energy bandgap for T = 500 K is lower than that for T = 300 K due to temperature-dependent bandgap shrinking. In the case of donor-

like traps, a dominant effect is observed in its ambipolar state as pointed out in Fig. 4.19(b), and in case of acceptor-like traps, a dominant effect is observed in its ON-state as pointed out in Fig. 4.19(a).

4.9 Summary

This article describes the study of temperature analyses for a JL-TFET on analog design parameters at higher temperatures and reported a descriptive investigation into the device performance using calibrated TCAD simulations and compared the results with a p-i-n SOI-TFET. An effort was also to improve the ambipolar performance of a JL-TFET. This work explores the HCI, TID, NBTI and process induced device reliability of JL-TFET.

JL-TFET is lesser degraded with HCI due to junctionless nature. Gate current creates traps near the drain, altering transistor behavior significantly with T for a transistor. Interestingly, I_G changes negligibly with T in a JL-TFET, and therefore formation of traps are also lesser. V_{TH} drop from 0.54 V to 0.44 V at a dose of 50 Mrad, which is consistent with p-i-n SOI-TFET performance. The V_{TH} increases significantly from 0.56V to 0.63V when the oxide thickness changes from 1.5 nm to 2.5 nm, indicating how sensitive JL-TFET performance is to oxide dimensions. On the other hand, the V_{TH} decreases from 0.65 to 0.58 when the substrate's dimensions are changed from 5 nm to 10 nm, highlighting the crucial significance that substrate characteristics play. The dimensions are changed from 5 nm to 10 nm, highlighting the crucial significance that substrate characteristics play. The generation of trapped charges in the gate dielectric, which modifies the electric field distribution, is the main reason for the V_{TH} reduction in JLTFETs produced by radiation dosage. This causes a shift in the V_{TH} due to increased gate leakage current and less channel control. Furthermore, by changing carrier mobility and density, radiation-induced flaws in the semiconductor material can also contribute to V_{TH} degradation. A time-dependent charge release from pre-existing traps in the dielectric bulk is revealed by exploring trapping-induced bias temperature instability (BTI). These thorough numerical results highlight the complex interactions between HCI, radiation, and NBTI that affect JL-TFET characteristics.

The effects of interface traps on the device performance are also investigated. The significant conclusions are listed below:

- As the temperature increases, the ON-state current (I_{ON}) for both JL-TFET and p-i-n SOI-TFET increases, unlike an inversion mode MOSFET, where I_D degrades with temperature.
- JL-TFET has a better I_{ON}/I_{OFF} ratio compared to a p-i-n SOI-TFET till T=400K, after which p-i-n SOI-TFET outperforms in temperature behaviour.
- JL-TFET outperforms in terms of better SS resulting in better quick switching to high T.
- Because of its better I_{OFF} and hence scalability; JL-TFET is a better fit for low-power applications such as memory devices. In addition, JL-TFET has fewer fabrication steps, and therefore, is cost-effective, compared to a p-i-n SOI-TFET.
- p-i-n SOI-TFETs offer better cut-off frequency (f_T) and better gain bandwidth product (GWP) till higher temperature making the device suitable for high-speed analog applications.
- Dual material technology helps in controlling ambipolar performance in a JL-TFET.
- Acceptor-like traps dominantly affect the transfer characteristics in the ON-state region again donor-like traps dominantly affect the ambipolar state region where the observation is done accordingly the closer the peak trap density value to the mid bandgap region, the traps get degraded more.

4.10 Sample Sentaurus TCAD Code for JL-TFET

SDE code:

```
(sde:set-process-up-direction 0)
(define Lg @Lg@) ; Lenth of Channe
(define Ld 20e-3) ;   Lenth of Drain
(define Ls 25e-3);  Lenth of Source


(define x1 Ls)
(define x2 (+ x1 Lg))
(define x3 (+ x2 Ld))
(define Spacer 5e-3)

(define Wc @Wc@);  Width of channel
(define Tox 2e-3);       Oxide thickness
(define M 5e-3);         Metal thicknes
```

```
(define y0 (+ Tox M))
(define y1 (+ Wc Tox))
(define y2 (+ y1 M))

(define C_Doping @Doping@)

(sdegeo:create-rectangle (position 0 0 0) (position x1 (* Wc -1) 0) "Silicon" "Source_R")
(sdegeo:create-rectangle (position x1 0 0) (position x2 (* Wc -1) 0) "Silicon" "Channel_R")
(sdegeo:create-rectangle (position x2 0 0) (position x3 (* Wc -1) 0) "Silicon" "Drain_R")
(sdegeo:set-default-boolean "BAB")
(sdegeo:create-rectangle (position 0 Tox 0) (position (- x1 Spacer) (* y1 -1) 0) "HfO2" "P_Gate_Oxide")
(sdegeo:create-rectangle (position 0 y0 0) (position (- x1 Spacer) (* y2 -1) 0) "Metal" "P_Gate_Contact")
(sdegeo:create-rectangle (position x1 Tox 0) (position x2 (* y1 -1) 0) "HfO2" "C_Gate_Oxide")
(sdegeo:create-rectangle (position x1 y0 0) (position x2 (* y2 -1) 0) "GatePolySilicon" "C_Gate_Contact")
(sdegeo:create-rectangle (position 0 y0 0) (position x3 (* y2 -1) 0) "SiO2" "Spacer_Region")

(sdegeo:define-contact-set "C-Gate" 4 (color:rgb 1 0 1 ) "##")
(sdegeo:define-contact-set "P-Gate" 4 (color:rgb 1 1 0 ) "##")
(sdegeo:define-contact-set "Source" 4 (color:rgb 0 1 0 ) "##")
(sdegeo:define-contact-set "Drain" 4 (color:rgb 1 0 0 ) "##")

(sdegeo:define-2d-contact (list (car (find-edge-id (position 0 (* (/ Wc 2) -1) 0)))) "Source")
(sdegeo:define-2d-contact (list (car (find-edge-id (position x3 (* (/ Wc 2) -1) 0)))) "Drain")
(sdegeo:define-2d-contact (list (car (find-edge-id (position (/ (- Ls Spacer) 2) (* y2 -1) 0)))) "P-Gate")
(sdegeo:define-2d-contact (list (car (find-edge-id (position (/ (- Ls Spacer) 2) y0 0)))) "P-Gate")
(sdegeo:define-2d-contact (list (car (find-edge-id (position (+ x1 (/ Lg 2)) (* y2 -1) 0)))) "C-Gate")
(sdegeo:define-2d-contact (list (car (find-edge-id (position (+ x1 (/ Lg 2)) y0 0)))) "C-Gate")

(sdedr:define-constant-profile "Junctioless-n_Doped" "ArsenicActiveConcentration" C_Doping)
(sdedr:define-constant-profile-material "Substrate_Doping" "Junctioless-n_Doped" "Silicon")
```

```
(sdedr:define-refinement-size "Silicon_Substrate" 0.002 0.001 0.001 0.0005 )
(sdedr:define-refinement-placement"RefinementPlacement_Si_Sub"
"Silicon_Substrate" (list "material" "Silicon" ) )

(sde:build-mesh "snmesh" "-a -c boxmethod" "n@node@_msh")
```

SDEVICE code:

```
File {
   * input files:
  Grid=   "@tdr@"
  Doping="@tdr@"
  Parameter="@parameter@"
  * output files:
  Plot=   "@tdrdat@"
  Current="@plot@"
  Output= "@log@"
}

Electrode{
   {Name="C-Gate" voltage=0}
   {Name="P-Gate" voltage=0}
   {Name="Source" voltage=0}
   {Name="Drain"  voltage=1}
    }

Physics
{
   Temperature = @Temp@
    Fermi
    EffectiveIntrinsicDensity(BandGapNarrowing (oldSlotboom))
    Mobility ( DopingDependance )
    Recombination( SRH(DopingDependence TempDependence)
    Band2Band (Model= NonlocalPath)
    eBarrierTunneling(Band2Band TwoBand Transmission)
    hBarrierTunneling(Band2Band TwoBand Transmission))
}

Physics (Material = "Metal")
{
     MetalWorkfunction ( Workfunction= 5.9)
}
Physics (Material = "GatePolySilicon")
{
     MetalWorkfunction ( Workfunction= 4.25)
}

Plot{
  eDensity hDensity
```

```
  TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
  eMobility hMobility
  eVelocity hVelocity
  Potential SpaceCharge
  Electrostaticpotential
  ElectricField/Vector
  Doping DonorConcentration AcceptorConcentration
  SRH
  Band2Band
  Auger
  AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
  BandGap
  EffectiveBandGap
  BandGapNarrowing
  Affinity
  ConductionBand ValenceBand
}

Math {
  RelErrControl
  Digits=7
  ErRef(electron)=1.e10
  ErRef(hole)=1.e10
  Notdamped=650
  Iterations=500
  DirectCurrent
  Method =ILS
  -CheckUndefinedModels
  }

Math(RegionInterface = "Source_R/Channel_R")
{
    NonLocal(Length = 1.8e-6 Permeable Permeation = 2e-6)
}
Math(RegionInterface = "Drain_R/Channel_R")
{
    NonLocal(Length = 1.8e-6 Permeable Permeation = 2e-6)
}

    Solve {
 *-- Buildup of initial solution:
  *NewCurrentFile=""
 Coupled(Iterations=700){ Poisson }
 Coupled{ Poisson Electron Hole  }
 Quasistationary(
  MinStep=1e-30 MaxStep=0.01
  Goal{ Name="C-Gate"   Voltage=1}
     ){ Coupled{ Poisson Electron Hole }
   }
  }
```

Parameter File:

```
#define ParFileDir .
Material="HfO2" {
  #includeext "ParFileDir/HfO2.par"
}
Material="GatePolySilicon" {
  #includeext "ParFileDir/GatePolySilicon.par"
}
Material="Metal" {
  #includeext "ParFileDir/Metal.par"
}
Material="PolySilicon" {
  #includeext "ParFileDir/PolySilicon.par"
}
Material="SiO2" {
  #includeext "ParFileDir/SiO2.par"
}
Material="Silicon" {
  #includeext "ParFileDir/Silicon.par"
BarrierTunneling

{
     g      = 2.1 ,  0.66    # [1]
     mt     = 0.1,   0.11    # [1]
     alpha= 0.00 ,0.00    # [1]

}

Band2BandTunneling

{
     Apath1         = 2.6e+06              # [1/cm^3/sec]
     Bpath1         = 4.2e+06              # [V/cm]
     Dpath1         = -0.45                # [eV]
     Ppath1         = 0.037                # [eV]
     Rpath1         = 0                    # [1]
     MaxTunnelLength   = 1.8e-06       # [cm]

}
}
```

Bibliography

[1] Colinge, J.-P., Lee, C.-W., Afzalian, A., Akhavan, N.D., Yan, R., Ferain, I., Razavi, P., O'Neill, B., Blake, A., White, M., Kelleher, A.-M., McCarthy, B. and Murphy, R. Nanowire transistors without junctions. Nature Nanotech. 5, 225–229, 2010. https://doi.org/10.1038/nnano.2010.15

[2] Kranti, A., Yan, R., Lee, C.-W., Ferain, I., Yu, R., Dehdashti Akhavan, N., Razavi, P. and Colinge, J. Junctionless nanowire transistor (JNT): Properties and design guidelines. In:

2010 Proceedings of the European Solid State Device Research Conference. pp. 357–360, 2010.

[3] Tiwari, S. and Saha, R. Methods to Reduce Ambipolar Current of Various TFET Structures: a Review. Silicon. 14, 6507–6515, 2022. https://doi.org/10.1007/s12633-021-01458-w

[4] Ghoneim, H. From All-Si Nanowire TFETs Towards III-V TFETs, 2012.

[5] Strangio, S., Palestri, P., Esseni, D., Selmi, L., Crupi, F., Richter, S., Zhao, Q.-T. and Mantl, S. Impact of TFET Unidirectionality and Ambipolarity on the Performance of 6T SRAM Cells. IEEE Journal of the Electron Devices Society. 3, 223–232, 2015. https://doi.org/10.1109/JEDS.2015.2392793

[6] Gedam, A., Acharya, B., Mishra, G.P.: Junctionless Silicon Nanotube TFET for Improved DC and Radio Frequency Performance. Silicon. 13, 167–178 (2021). https://doi.org/10.1007/s12633-020-00410-8

[7] Nigam, K., Gupta, S., Pandey, S., Kondekar, P.N. and Sharma, D. Controlling the ambipolarity and improvement of RF performance using Gaussian Drain Doped TFET. International Journal of Electronics. 105, 806–816, 2018. https://doi.org/10.1080/00207217.2017.1409807

[8] Nagavarapu, V., Jhaveri, R. and Woo, J.C.S. The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor. IEEE Transactions on Electron Devices. 55, 1013–1019, 2008. https://doi.org/10.1109/TED.2008.916711

[9] Saurabh, S. and Kumar, M.J. Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices. 58, 404–410, 2011. https://doi.org/10.1109/TED.2010.2093142

[10] Strangio, S., Palestri, P., Lanuzza, M., Crupi, F., Esseni, D. and Selmi, L. Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits. IEEE Transactions on Electron Devices. 63, 2749–2756, 2016. https://doi.org/10.1109/TED.2016.2566614

[11] Chattopadhyay, A. and Mallik, A. Impact of a Spacer Dielectric and a Gate Overlap/Underlap on the Device Performance of a Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices. 58, 677–683, 2011. https://doi.org/10.1109/TED.2010.2101603

[12] Choi, W.Y. and Lee, W. Hetero-Gate-Dielectric Tunneling Field-Effect Transistors. IEEE Trans. Electron Devices. 57, 2317–2319, 2010. https://doi.org/10.1109/TED.2010.2052167

[13] Nigam, K., Kondekar, P., Chandan, B.V., Kumar, S., Tikkiwal, V.A., Dharmender, Singh, Km.S., Bhardwaj, E., Choubey, S. and Chaturvedi, S. Performance and Analysis of Stack Junctionless Tunnel Field Effect Transistor. Silicon. 14, 1549–1558, 2022. https://doi.org/10.1007/s12633-021-00958-z

[14] Tirkey, S., Sharma, D., Yadav, D.S. and Yadav, S. Analysis of a Novel Metal Implant Junctionless Tunnel FET for Better DC and Analog/RF Electrostatic Parameters. IEEE Transactions on Electron Devices. 64, 3943–3950, 2017. https://doi.org/10.1109/TED.2017.2730922

[15] Routh, S., Deb, D., Baruah, R.K. and Goswami, R. Junctionless Tunnel FET for High-Temperature Applications from an Analog Design Perspective. In: 2022 IEEE International Conference on Nanoelectronics, Nanophotonics, Nanomaterials, Nanobioscience & Nanotechnology (5NANO). pp. 1–4, 2022.

[16] Fleetwood, D.M., Winokur, P.S., Reber, R.A., Jr., Meisenheimer, T.L., Schwank, J.R., Shaneyfelt, M.R. and Riewe, L.C. Effects of oxide traps, interface traps, and ``border traps'' on metal-oxide-semiconductor devices. Journal of Applied Physics. 73, 5058–5074,

1993. https://doi.org/10.1063/1.353777

[17] Lyu, J.-S. and Lee, K.-S.N. Determination of the Interface Trap Density in Metal Oxide Semiconductor Field-Effect Transistor through Subthreshold Slope Measurement. Jpn. J. Appl. Phys. 32, 4393, 1993. https://doi.org/10.1143/JJAP.32.4393

[18] Agarwal, S. and Yablonovitch, E. Designing a low-voltage, high-current tunneling transistor. In: Kuhn, K. and King Liu, T.-J. (eds.) CMOS and Beyond: Logic Switches for Terascale Integrated Circuits. pp. 79–116. Cambridge University Press, Cambridge, 2015.

[19] Xiao, T.P., Zhao, X., Agarwal, S. and Yablonovitch, E. Impact of interface defects on tunneling FET turn-on steepness. In: Fourth Berkeley Symposium on Energy Efficient Electronic Systems (E3S). pp. 1–2, 2015.

[20] Qiu, Y., Wang, R., Huang, Q. and Huang, R. A Comparative Study on the Impacts of Interface Traps on Tunneling FET and MOSFET. IEEE Transactions on Electron Devices. 61, 1284–1291, 2014. https://doi.org/10.1109/TED.2014.2312330

[21] Boucart, K. and Ionescu, A.M. Double-Gate Tunnel FET With High-κ Gate Dielectric. IEEE Transactions on Electron Devices. 54, 1725–1733, 2007. https://doi.org/10.1109/TED.2007.899389

[22] Ehteshamuddin, M., Alharbi, A.G. and Loan, S.A. Impact of interface traps on the BTBT-current in tunnel field effect transistors. In: 5th International Conference on Electrical and Electronic Engineering (ICEEE). pp. 224–227, 2018.

[23] Tripathy, M.R., Samad, A., Singh, A.K., Singh, P.K., Baral, K., Mishra, A.K. and Jit, S. Impact of interface trap charges on electrical performance characteristics of a source pocket engineered Ge/Si heterojunction vertical TFET with HfO2/Al2O3 laterally stacked gate oxide. Microelectronics Reliability. 119, 114073, 2021. https://doi.org/10.1016/j.microrel.2021.114073

[24] Pezzimenti, F., Bencherif, H., De Martino, G., Dehimi, L., Carotenuto, R., Merenda, M. and Della Corte, F.G. Study and Assessment of Defect and Trap Effects on the Current Capabilities of a 4H-SiC-Based Power MOSFET. Electronics. 10, 735, 2021. https://doi.org/10.3390/electronics10060735

[25] Fan, M.-L., Hu, V.P.-H., Chen, Y.-N., Su, P. and Chuang, C.-T. Analysis of Single-Trap-Induced Random Telegraph Noise and its Interaction With Work Function Variation for Tunnel FET. IEEE Transactions on Electron Devices. 60, 2038–2044, 2013. https://doi.org/10.1109/TED.2013.2258157

[26] Fan, M.-L., Yang, S.-Y., Hu, V.P.-H., Chen, Y.-N., Su, P. and Chuang, C.-T. Single-trap-induced random telegraph noise for FinFET, Si/Ge Nanowire FET, Tunnel FET, SRAM and logic circuits. Microelectronics Reliability. 54, 698–711, 2014. https://doi.org/10.1016/j.microrel.2013.12.026

[27] Ghosh, P. and Bhowmick, B. Effect of temperature in selective buried oxide TFET in the presence of trap and its RF analysis. International Journal of RF and Microwave Computer-Aided Engineering. 30, e22269, 2020. https://doi.org/10.1002/mmce.22269

[28] Ghosh, P., Roy, A. and Bhowmick, B. The impact of donor/acceptor types of interface traps on selective buried oxide TFET characteristics. Appl. Phys. A. 126, 330, 2020. https://doi.org/10.1007/s00339-020-03505-6

[29] Gupta, S., Nigam, K., Pandey, S., Sharma, D. and Kondekar, P.N. Effect of Interface Trap Charges on Performance Variation of Heterogeneous Gate Dielectric Junctionless-TFET. IEEE Transactions on Electron Devices. 64, 4731–4737, 2017. https://doi.org/10.1109/TED.2017.2754297

[30] Huang, X.Y., Jiao, G.F., Cao, W., Huang, D., Yu, H.Y., Chen, Z.X., Singh, N., Lo, G.Q., Kwong, D.L. and Li, M.-F. Effect of Interface Traps and Oxide Charge on Drain Current

Degradation in Tunneling Field-Effect Transistors. IEEE Electron Device Letters. 31, 779–781, 2010. https://doi.org/10.1109/LED.2010.2050456

[31] Beneventi, G.B., Gnani, E., Gnudi, A., Reggiani, S., Baccarani, G.: Can Interface Traps Suppress TFET Ambipolarity? IEEE Electron Device Letters. 34, 1557–1559, 2013. https://doi.org/10.1109/LED.2013.2284290

[32] Pandey, R., Saripalli, V., Kulkarni, J.P., Narayanan, V. and Datta, S.: Impact of Single Trap Random Telegraph Noise on Heterojunction TFET SRAM Stability. IEEE Electron Device Letters. 35, 393–395, 2014. https://doi.org/10.1109/LED.2014.2300193

[33] Sant, S., Schenk, A., Moselund, K. and Riel, H. Impact of trap-assisted tunneling and channel quantization on InAs/Si hetero Tunnel FETs. In: 74th Annual Device Research Conference (DRC). pp. 1–2, 2016.

[34] Priya, G.L. and Balamurugan, N.B. New dual material double gate junctionless tunnel FET: Subthreshold modeling and simulation. AEU - International Journal of Electronics and Communications. 99, 130–138, 2019. https://doi.org/10.1016/j.aeue.2018.11.037

[35] Basak, S., Asthana, P.K., Goswami, Y. and Ghosh, B. Leakage current reduction in junctionless tunnel FET using a lightly doped source. Appl. Phys. A. 118, 1527–1533, 2015. https://doi.org/10.1007/s00339-014-8935-9

[36] Ghosh, B., Akram, M.W. Junctionless Tunnel Field Effect Transistor. IEEE Electron Device Letters. 34, 584–586, 2013. https://doi.org/10.1109/LED.2013.2253752

[37] Deb, D., Goswami, R., Baruah, R.K., Kandpal, K. and Saha, R. An SOI n-p-n Double Gate TFET for Low Power Applications. In: 2021 Devices for Integrated Circuit (DevIC). pp. 621–623, 2021.

[38] Sentaurus Device User: Sentaurus TCAD Version R-2020.09-SP1

[39] Schenk, A. A model for the field and temperature dependence of Shockley-Read-Hall lifetimes in silicon. Solid-State Electronics. 35, 1585–1596, 1992. https://doi.org/10.1016/0038-1101(92)90184-E

[40] Narang, R., Saxena, M., Gupta, R.S. and Gupta, M. Impact of Temperature Variations on the Device and Circuit Performance of Tunnel FET: A Simulation Study. IEEE Transactions on Nanotechnology. 12, 951–957, 2013. https://doi.org/10.1109/TNANO.2013.2276401

[41] Baruah, R.K., Paily, R.P.: High-temperature effects on device performance of a junctionless transistor. In: International Conference on Emerging Electronics. pp. 1–4, 2012.

[42] Sentaurus TM, Device User Guide, Version R-2020.09, September 2020. Mountain View, CA, Available online: https://www.synopsys.com, 2020. (Accessed 15 March 2023)

[43] Mishra, V., Verma, Y.K., Agarwal, L. and Gupta, S.K. Temperature impact on device characteristics of charge plasma based tunnel FET with Si0.5Ge0.5 source. Engineering Research Express. 3, 045012, 2021. https://doi.org/10.1088/2631-8695/ac310e

[44] Uddin Shaikh, M.R. and Loan, S.A. Drain-Engineered TFET With Fully Suppressed Ambipolarity for High-Frequency Application. IEEE Transactions on Electron Devices. 66, 1628–1634, 2019. https://doi.org/10.1109/TED.2019.2896674

[45] Suh Song, Y., Yeong Kim, K., Young Yoon, T., Jung Kang, S., Kim, G., Kim, S. and Hyun Kim, J. Reliability improvement of self-heating effect, hot-carrier injection, and on-current variation by electrical/thermal co-design. Solid-State Electronics. 197, 108436, 2022. https://doi.org/10.1016/j.sse.2022.108436

[46] Asthana, P.K., Ghosh, B., Rahi, S.B.M. and Goswami, Y. Optimal design for a high performance H-JLTFET using HfO2 as a gate dielectric for ultra low power applications.

RSC Adv. 4, 22803–22807, 2014. https://doi.org/10.1039/C4RA00538D

[47] Bentrcia, T., Djeffal, F., Ferhati, H. and Dibi, Z. A Comparative Study on Scaling Capabilities of Si and SiGe Nanoscale Double Gate Tunneling FETs. Silicon. 12, 945–953, 2020. https://doi.org/10.1007/s12633-019-00190-w

[48] Wang, Y., Li, Y., Yang, Y. and Chen, W. Hot Carrier Injection Reliability in Nanoscale Field Effect Transistors: Modeling and Simulation Methods. Electronics. 11, 3601, 2022. https://doi.org/10.3390/electronics11213601

[49] Grasser, T., Kaczer, B., Goes, W., Aichinger, Th., Hehenberger, Ph. and Nelhiebel, M. A two-stage model for negative bias temperature instability. In: IEEE International Reliability Physics Symposium. pp. 33–44. IEEE, Montreal, QC, Canada, 2009.

[50] Mahapatra, S. and Parihar, N. A review of NBTI mechanisms and models. Microelectronics Reliability. 81, 127–135, 2018. https://doi.org/10.1016/j.microrel.2017.12.027

[51] Chen, C., Chen, M. j., Wang, C. j. and Wu, K. A New NBTI Lifetime Model (Ig-model) and an Investigation on Oxide Thickness Effect on NBTI Degradation and Recovery. In: IEEE International Reliability Physics Symposium Proceedings. pp. 741–742. IEEE, San Jose, CA, USA, 2006.

[52] Schwank, J.R., Shaneyfelt, M.R., Fleetwood, D.M., Felix, J.A., Dodd, P.E., Paillet, P. and Ferlet-Cavrois, Vé. Radiation Effects in MOS Oxides. IEEE Transactions on Nuclear Science. 55, 1833–1853, 2008. https://doi.org/10.1109/TNS.2008.2001040

[53] Shiono, N., Shimaya, M. and Sano, K. Ionizing Radiation Effects in MOS Capacitors with Very Thin Gate Oxides. Jpn. J. Appl. Phys. 22, 1430, 1983. https://doi.org/10.1143/JJAP.22.1430

[54] Sujatha, R., Damle, R., Khan, A.R. and Ravindra, M. Study of the effect of gamma radiation on MOSFET for space applications. Indian Journal of Pure and Applied Physics. 56, 587–590, 2018.

[55] Barnaby, H.J. Total-Ionizing-Dose Effects in Modern CMOS Technologies. IEEE Trans. Nucl. Sci. 53, 3103–3121, 2006. https://doi.org/10.1109/TNS.2006.885952

[56] Routh, S. and Baruah, R.K. A comprehensive analysis of LDMOS transistors for analog applications under γ-radiation. Microelectronics Reliability. 148, 115159, 2023. https://doi.org/10.1016/j.microrel.2023.115159

[57] Routh, S., Deb, D., Baruah, R.K. and Goswami, R. Impact of High-temperature and Interface Traps on Performance of a Junctionless Tunnel FET. Silicon. 15, 2703–2714, 2023. https://doi.org/10.1007/s12633-022-02191-8

[58] Goswami, R., Bhowmick, B. and Baishya, S. Electrical noise in Circular Gate Tunnel FET in presence of interface traps. Superlattices and Microstructures. 86, 342–354, 2015. https://doi.org/10.1016/j.spmi.2015.07.064

[59] Wang, W., Hwang, J.C.M., Xuan, Y. and Ye, P.D. Analysis of Electron Mobility in Inversion-Mode \hboxAl_2\hboxO_3/\hboxIn_x\hboxGa_1 - x\hboxAs MOSFETs. IEEE Transactions on Electron Devices. 58, 1972–1978, 2011. https://doi.org/10.1109/TED.2011.2146255

[60] Deb, D., Goswami, R., Baruah, R.K., Kandpal, K. and Saha, R. Parametric investigation and trap sensitivity of *n-p-n* double gate TFETs. Computers and Electrical Engineering. 100, 107930, 2022. https://doi.org/10.1016/j.compeleceng.2022.107930