CHAPTER 1

Introduction

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Chapter 1: Introduction

1.1. Background:

For several decades, Silicon (Si) has been fundamental to the development of semiconductor devices, especially in Metal Oxide Field-Effect Transistors (MOSFETs), which follow Moore's Law [1]. The transistors invented in the late 1940s prompted the birth of modern electronics. Since then, the performance of Si-based devices has progressively improved through advancements in Metal-Semiconductor (M-S) interface engineering and device scaling. As silicon wafer line widths have reached the nanometer scale (10^{-9} m), corresponding to the size of only a few molecules, the material's physical and chemical properties undergo significant changes. With further scaling of the channel length, new challenges arise, including reduced carrier mobility, increased heat dissipation, and the emergence of short-channel effects. In addition, these developments have played a crucial role in optimizing key parameters, such as threshold voltage, which significantly impact the device's operating performance [2]. Various strategies have been implemented to uphold the momentum of Moore's Law, which include employing strained silicon, utilizing high-k dielectric materials, optimizing contact engineering at Metal-Semiconductor junctions, and innovating multi-gate Field-Effect transistors (FET) [3–5]. Despite that, the Si-based device undergoes numerous challenges like short- and long-channel effects, which can lead to inadequate threshold voltage control and unwanted switching behaviour [3,6]. These complications can be alleviated by reducing semiconductor thickness through pseudo-quantum confinement, where the movement of charge carriers is restricted in specific directions, leading to improved material performance. A notable implementation of this approach is Silicon-On-Insulator (SOI) technology, which employs a thin silicon layer over an insulating substrate to enhance device efficiency and mitigate these issues [7]. However, SOI technology has certain drawbacks, including high manufacturing costs, self-heating effects caused due to the insulating buried oxide layer, and limitations in its application to flexible electronics. The evolution of the FET structures over time is pictorially described in Fig. 1.1. Recently, research has shifted focus towards non-Si semiconductor devices. Looking forward, continuing the pace of Moore's Law will likely require new materials for the device channels, especially at the atomic scale [8,9]. Various studies have shown that 1D and 2D materials exhibit semiconducting properties, which can be tailored to meet specific application requirements. Non-Si materials, such as semiconductor Nanowires (NWs), Nanotubes (NTs), and Nanoribbons (NRs), represent a class of 1D materials, while Two-

Dimensional (2D) materials include Graphene, Black Phosphorus (BP), and Transition Metal Dichalcogenides (TMDs) [8–10].

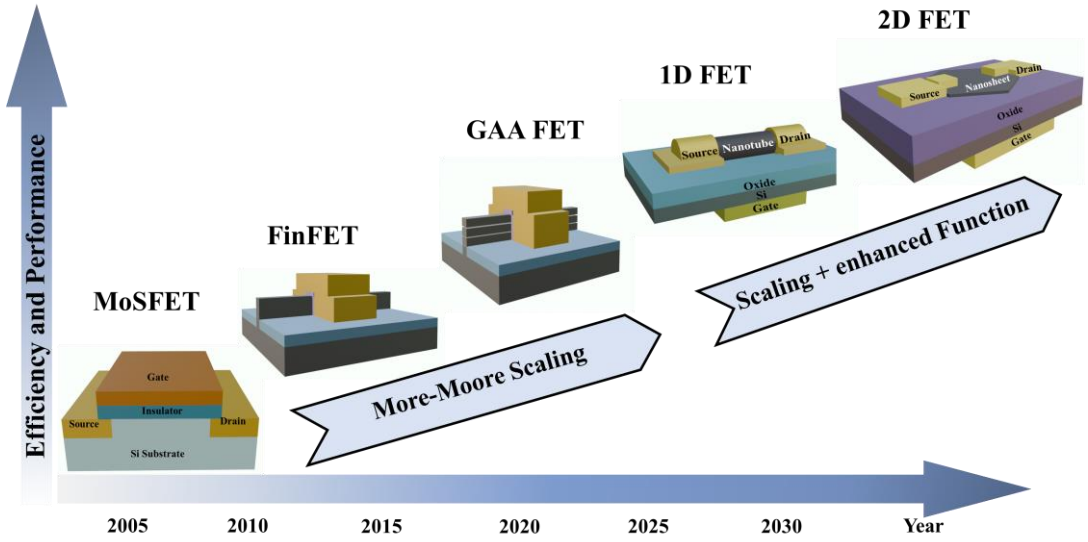

Fig. 1.1: Evolution of FET structures over time: From traditional Si-based MOSFETs to FinFET and Gate-All-Around (GAA) transistors, which are expected to dominate the market by the mid-2020s. The evolution continues with the incorporation of 1D and 2D materials like nanotubes and nanosheets, highlighting enhanced scaling and functionality in modern FET designs, and promising further advancements in efficiency and performance

1.1.1. 1D-Material based FET:

1D nanomaterials like nanorods [11], nanotubes[12] nanowires [13], nanoribbons [14], etc. have exceptional properties, making them a distinct group of materials for field effect device applications. These constructions are usually 1,000 times thinner than a strand of human hair [15]. These materials are categorized according to their shapes, sizes, diameters, and widths of the nanostructure. Fig. 1.2 represents the crystal structure of the 1D nanomaterials such as nanowires, nanotubes, nanorods, etc. [10]. These nanomaterials' desired shape, size and orientation are primarily obtained depending on the synthesis parameters including reaction time, precursor concentration, nucleation, growth rates and temperature [16,17]. Nanorods are solid, cylindrical structures, while nanotubes are hollow cylinders, and nanowires typically have a round cross-section,

resembling nanotubes [16,18,19]. Nanoribbons are distinct from cylindrical-shaped 1D materials, as they have a flat, planar structural morphology [20–22]. The lengths of these 1D materials typically range from a few to several hundred nanometers. Nanorods and nanotubes are generally synthesized from metallic materials (e.g., Au [23]) or semiconducting materials (e.g., Si [24], ZnO [25, 26], TiO_2 [27], Carbon [12]) exhibiting either metallic or semiconducting behaviour depending on their composition. For instance, adjusting the temperature during the synthesis can transition a material from forming plate-like nanosheets to elongated nanorods or nanowires [9,10]. Similarly, varying precursor concentrations or growth rates can favour specific anisotropic growth, leading to unique structural shapes [28]. The nanostructure has different significant characteristics, enabling specialized applications across various fields. By fine-tuning the morphology of 1D materials, researchers can exploit their distinctive functional properties for various applications, such as electronics, optoelectronics, catalysis, sensors, etc. [30–32]. Park et al. reported that N-channel ZnO nanorod FETs demonstrate exceptional electrical properties, including a mobility of approximately 75 $cm^2/V{\cdot}s$ and a transconductance of around 140 nS, significantly outperforming ZnO-based nanobelt structures [33]. Despite these advantages, challenges such as material availability, size constraints, fragility during fabrication, and difficulty in achieving reliable electrical contact limit the broader application of nanorods in FETs. These issues impact both performance and reproducibility. Nanowires offer another 1D platform, where precise size control plays a crucial role in determining device performance. High-performance FETs particularly benefit from nanowires with diameters below 20 nm, as noted by Lu et al. [34]. Furthermore, Cohen et al. reported on SiNW FETs, emphasizing that these devices, unlike those with Schottky source and drain contacts, exhibit unipolar transport, which enhances their functionality. The estimated electron mobility of SiNW FETs is comparable to that of bulk silicon, making them ideal for advanced electronic applications [35]. For carbon-based 1D materials, Carbon Nanotube (CNT) FETs and Carbon Nanoribbon (CNR) FETs offer distinct advantages. A comparative study by Ouyang et al. highlighted that while CNT-FETs exhibit a larger on-current due to higher quantum capacitance, CNR-FETs deliver superior performance in high-speed applications due to their higher carrier velocity and shorter intrinsic delay [36]. While CNT-FETs have a

larger on-current due to their higher quantum capacitance, CNR-FETs are better suited for high-speed applications.

These 1D nanostructures offer significant potential for enhanced electrochemical performance. Their high aspect ratios increase the surface area of electrodes, providing more active reaction sites for various applications. While their electrical conductivities may be lower compared to bulk materials, these properties can be improved by optimizing grain boundaries and surface conditions, facilitating efficient charge transfer by reducing scattering effects. The 1D material in the semiconductor device application shows superior electrical performance including high ON/OFF current ratio (I_{ON}/I_{OFF}) and low power consumption which make them attractive for high-performance devices [37, 38]. Despite their remarkable electrical properties, the 1D nanomaterials face significant challenges including device-to-device performance variations due to uncontrolled factors such as thickness, shape, size distribution and fabrication difficulties in device applications [28].

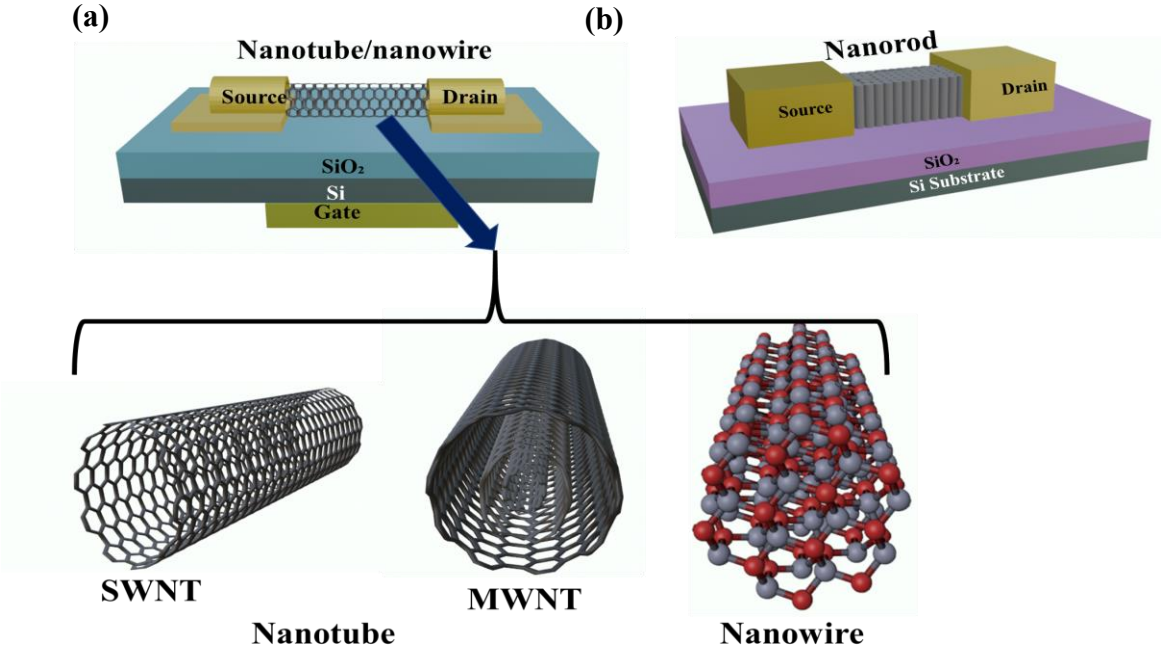

Fig. 1.2: Schematic representation of a 1D material-based FET structure: (a) A semiconducting channel composed of a nanotube or nanowire positioned vertically between the source and drain metal contacts, and (b) multiple nanorods arranged horizontally in the FET device, serving as the semiconducting channel between the source and drain metal contacts

However, 1D nanomaterials encounter several challenges that limit their broader application in advanced electronic devices. Issues such as material purity, chirality control, and the presence of crystal defects significantly impact their performance and reproducibility. Additionally, large-scale fabrication and integration into devices remain complex and challenging. Compared to 2D nanomaterials, 1D nanomaterials typically exhibit lower surface areas and are more susceptible to environmental instability, edge defects, and structural imperfections. Achieving precise width control and ensuring scalability in production further complicate their use in practical applications. Overcoming these limitations is essential for realizing the full potential of 1D nanomaterials in modern technologies [17, 37].

1.1.2. 2D-Material based FET:

The 2D layered materials including graphene, Black Phosphorus (BP), TMD, etc. have garnered significant attention in recent years due to their unique properties. Those materials have fascinating features like ultrathin layered structure, mechanical flexibility, and chemical stability making it ideal for various electronics and optoelectronics applications. In addition, these materials are stacked layer by layer, with the layers being vertically bonded through weak van-der Waals (vdW) forces. The ultrathin structures of 2D materials are particularly promising for nanoscale device applications due to their dimensions and atomic-level precision, as shown in Fig. 1.3 [39,40]. Moreover, the properties of 2D materials depend on their physical characteristics, including structural morphology, thickness, number of layers, and material quality [41]. In general, depending on the application requirements, thin films of 2D materials are either grown or prepared by directly exfoliating thin nanoflakes from bulk powder or crystal. High-crystal-quality films are essential for advanced technologies such as electronics, spintronics, optoelectronics, energy storage, solar cells, etc. [42]. The atomic structure of the various 2D materials is illustrated in Fig. 1.3.

The 2D semiconductor material of graphene was first demonstrated by Novoselov et al. in 2004 [43]. The graphene is a stacked building block of graphite, represented in Fig. 1.3(a). Graphene has a hexagonal lattice structure with one carbon atom thick layer where the atoms are present at each corner of the lattice. The bond length between two carbon atoms is 1.42 Å and the lattice constant is 2.46 Å [6,7]. The graphene has

exceptional properties such as being incredibly strong, yet lightweight, and exhibits extraordinary electrical and thermal conductivity [46]. This material is also highly flexible making it ideal for a wide range of applications, from electronics and energy storage to medical devices and composite materials [9,10]. Also, it has many other benefits such as high electrical and thermal conductivities in addition to mechanical strength and carrier mobility [49]. Graphene displays remarkable electrical conductivity, with electron mobilities surpassing 200,000 $cm^2/V \cdot s$ at room temperature [50]. In terms of its mechanical properties, it is the most durable material currently recognized, boasting a tensile strength of approximately 130 GPa and a Young's modulus of 1 TPa, all while maintaining a thickness of just one atom [51]. With its high thermal conductivity of up to 1500 to 5000 W/m·K and optical transparency that absorbs only about 2.3% of incoming light, it is perfect for thermal management and optoelectronic purposes [14,15]. Various synthesis techniques, such as mechanical exfoliation, Chemical Vapor Deposition (CVD), and chemical reduction of graphene oxide, enable its application across a wide range from small research samples to large-scale commercial use [39, 54]. However, graphene's zero-bandgap nature restricts its ability to toggle between conductive and non-conductive states, posing challenges to its integration into electronic devices like transistors [50]. Furthermore, its weak optical absorption limits its effectiveness in optoelectronic applications, where strong light-matter interactions are crucial for optimal performance [55].

Similar to graphene, the monolayer atomic structure of BP exhibits a puckered honeycomb lattice, with each phosphorus atom covalently bonded to three adjacent phosphorus atoms as depicted in Fig. 1.3(b) [56]. BP was first synthesized in 1914 by Bridgeman through a process involving white phosphorus, utilizing hydrostatic pressure of approximately 1.2 GPa and temperatures up to 200 °C [57]. BP exhibits exceptional tensile strain capabilities, reaching 27% in the zigzag direction and 30% in the armchair direction. It also demonstrates remarkable flexibility and a significantly lower Young's modulus (0.166 TPa in the zigzag direction and 0.044 TPa in the armchair direction) compared to graphene and TMD materials [58]. The individual layers of BP are held together by weak van der Waals forces with adjacent layers [56]. BP has emerged as a prominent focus in modern semiconductor research. Its exceptional carrier mobility, anisotropic electronic properties, and adjustable direct bandgap (2 eV) make it a

promising alternative to conventional Si-based semiconductors, paving the way for innovations in next-generation electronics and optoelectronics applications [59–61]. Despite its unique features, BP faces several significant challenges that hinder its potential for widespread adoption. One of the most pressing issues is the difficulty in scaling up the production of high-quality BP films. Maintaining consistent material quality at the nanoscale continues to be a significant challenge [62]. In addition, the uncontrolled nucleation during the BP growth process often results in inconsistencies in the structural and electronic properties of the material [59]. However, BP faces critical challenges, including air instability, scalability issues, integration barriers, and susceptibility to oxidation, which degrades its structural and electronic properties [63,64]. Ensuring the long-term effectiveness of BP-based devices requires robust protective strategies, such as encapsulation or surface modification, to prevent environmental degradation.

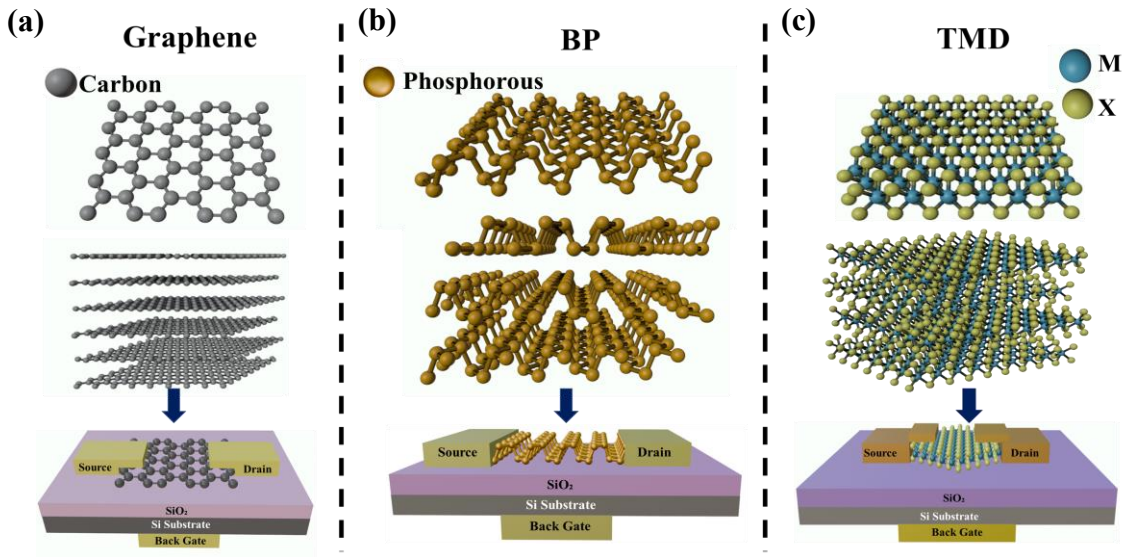

Fig. 1.3: Illustrates the atomic structures of 2D materials and their corresponding FET structures: (a) graphene (b) Black phosphorus and (c) Transition Metal Dichalcogenide

A new group of atomically thin layered 2D materials of TMD, with a graphene-like atomic structure has been demonstrated recently in several semiconducting device applications as depicted in Fig. 1.3(c) [65]. TMDs are some of the elemental layered crystals that are classified into three different types: semiconducting, such as MoX_2 and WX_2 compounds, metallic NbX_2 and TaX_2, and superconducting are $MoTe_2$, WTe_2, etc. as depicted in Fig. 1.4. The TMD structure with a formula of MX_2 and WX_2 has a graphene-like structure, where Molybdenum (Mo) or Tungsten (W) is a group of VI atom sandwich between two Chalcogen (X) atoms, M is a transition metal (Mo, W or Ti), and

X is a chalcogen atom (S, Se, etc.) [66]. Numerous researchers have reported that TMD materials exhibit a high physical and mechanical stability which can be suitable for wirable and flexible electronics. In addition, 2D-TMDs offer a high surface area, the absence of dangling bonds or charge traps on their surfaces and tunable bandgap making them highly promising for the development of high-quality nanoelectronics devices [65,67,68]. The layers of TMD materials are bonded by weak Van der Waals forces, enabling easy exfoliation from bulk nanosheets. However, the Graphene with a similar structure to that of TMDs is a zero-bandgap material which is not suitable for many electronics and optoelectronics applications [69]. In contrast, TMD has a sizable bandgap that can be tuned down by thinning the layers of nanosheets. The bandgap conversion occurs from the indirect bandgap of bulk material to the direct bandgap of monolayer nanosheet by thinning down the staked layers [4,5]. The similarity in the band structures of many semiconducting TMDs can be demonstrated using first-principles calculations and tight-binding approximations.

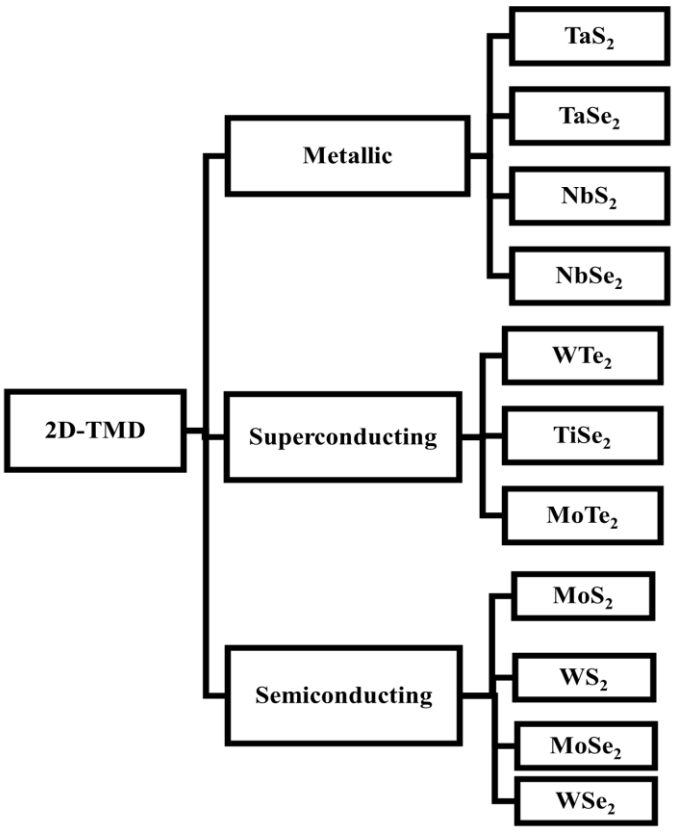

Fig. 1.4: 2D-TMD materials are categorized into three distinct types: Metallic, Superconducting, and Semiconducting

Layered 2D-TMDs are Molybdenum Disulfide (MoS_2), Tungsten Disulfide (WS_2), Molybdenum Diselenide ($MoSe_2$) and Tungsten Diselenide (WSe_2) are known for their distinctive semiconducting properties. Among these, MoS_2 and WS_2 are extensively used in semiconducting applications, exhibiting n-type semiconducting behaviour, while $MoSe_2$ and WSe_2 demonstrate p-type semiconducting properties [29,30]. Due to their multiple advantages, TMD materials have given rise to widespread interest in recent years as electronic materials, providing an attractive alternative to conventional semiconductors than zero-band graphene. TMD is used for many applications, such as FETs, photodetectors, sensors memory devices etc., the application of the TMD material-based device is represented in Fig. 1.5 [72–77].

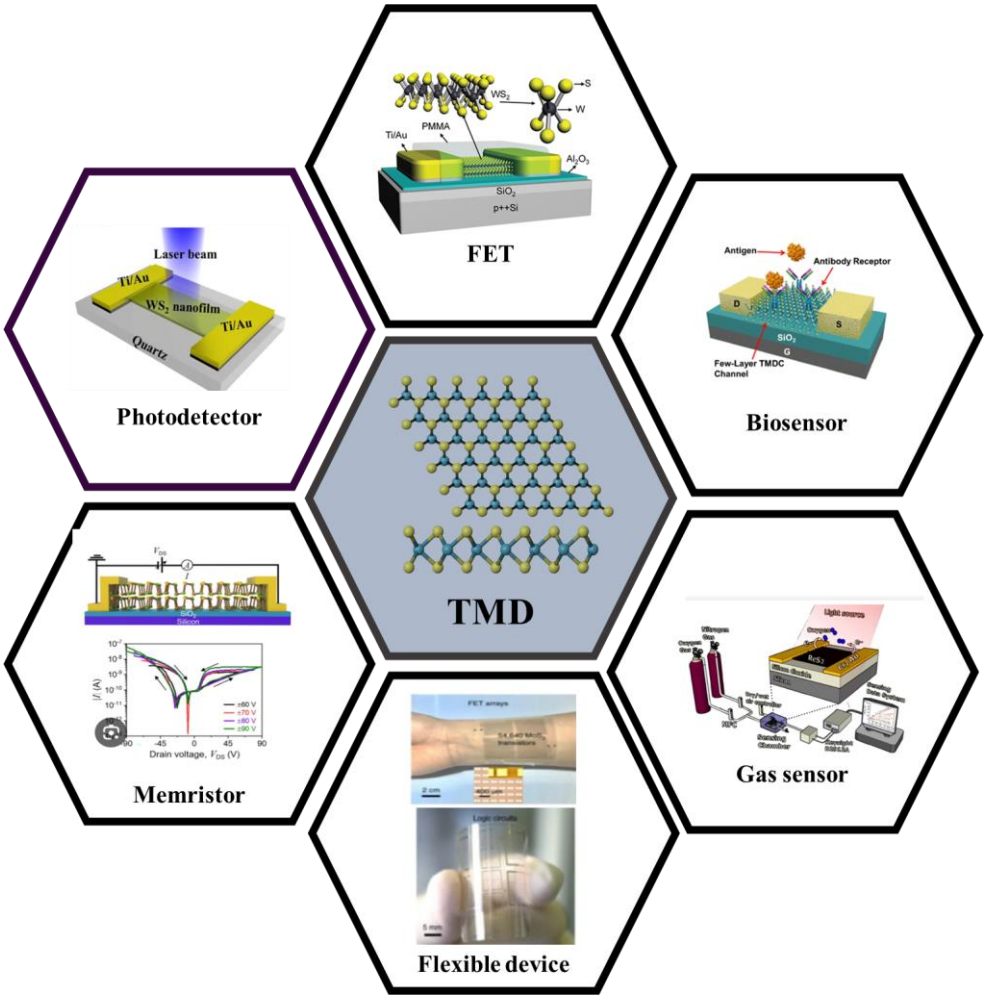

Fig. 1.5: Diagrammatic representation of various device architectures based on TMD material for various electronics and optoelectronic applications: FET, biosensor, gas sensor, flexible device, memristor and photodetector [78–83]

Recently, the n-type semiconducting property of a few layers of hexagonal structure of 2D MoS_2 and WS_2 has been extensively studied for FET applications [37,38]. One of the suitable advantages of the 2D-TMD material is that its electrical property depends on the number of layers. In bulk form, WS_2 nanosheets exhibit an indirect bandgap of ~1.4 eV in their bulk form, while in its monolayer form structure transitions to a direct bandgap of around 2.1 eV. Similarly, MoS_2 exhibits a direct bandgap of 1.8 eV in the monolayer and an indirect bandgap of ~1.2 eV in its bulk form [86]. As illustrated in Fig. 1.6, the bandgap of TMD materials transitions from an indirect bandgap to a direct bandgap. The indirect bandgap at the Γ-point primarily results from the hybridization of d-orbitals on the Transition Metal (M) atoms with antibonding p^z orbitals on the X atoms [87]. In bulk TMDs, strong interlayer coupling significantly influences these states, causing their energy levels to vary with the number of layers. However, the energy gap at the K-point remains largely independent of the number of layers in the nanosheets [88]. This is because the conduction band states at the K-point are predominantly formed by highly localized d orbitals on the M atoms. These states exhibit minimal interlayer coupling, as the M atoms are positioned centrally within the S-M-S unit cell, reducing their interaction with adjacent layers [89]. The variation in the band structure of TMDs is primarily due to quantum confinement effects, which are further influenced by doping and edge phenomena. Additionally, hybridization significantly influences the energy states near the Fermi level, resulting in elevated energy levels at specific points in the band structure.

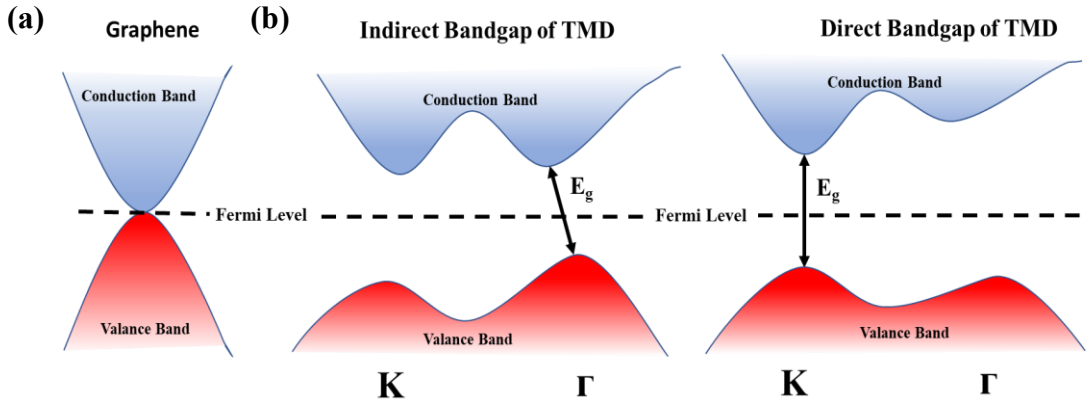

Fig. 1.6: Schematic depiction of energy band diagram of (a) graphene and (b) the indirect bandgap of bulk TMD and the direct bandgap of monolayer TMD

Chapter 1: Introduction

This research focuses on the application of WS_2 material in FETs, emphasizing the distinct advantages WS_2 offers over other TMDs, particularly MoS_2. While both materials share similar crystal structures and n-type semiconducting behaviour, WS_2 demonstrates superior physical, electrical, and thermal characteristics compared to other TMDs, making it more suitable for advanced electronic and optoelectronic device applications. A comparative overview is presented in Table 1.1, emphasizing the necessity of critically evaluating the specific ways in which WS_2 outperforms MoS_2 in FET applications. Notably, WS_2 exhibits a higher thermal oxidation temperature (~500 °C vs. ~400 °C) and melting point (1250 °C vs. 1185 °C), enabling more robust device operation under high-temperature and harsh environmental conditions, an essential criterion for next-generation nanoelectronics and aerospace applications. Additionally, WS_2 surpasses MoS_2 in terms of greater chemical stability, improved mechanical strength, a lower friction coefficient, and superior lubrication properties [83,84,86]. These characteristics make WS_2 particularly suitable for use in harsh environments, such as high-temperature and vacuum conditions, where enhanced stability and lower friction are crucial. In addition to its physical properties, WS_2 demonstrates superior electrical and optical performance compared to MoS_2 [93]. Electrically, WS_2 demonstrates a slightly wider bandgap (~2.1 eV vs. ~1.8 eV for monolayers), stronger optical absorption, and higher intrinsic carrier mobility compared to MoS_2, resulting in faster switching speeds and improved I_{ON}/I_{OFF} ratios, better electrostatic control in FETs [75]. WS_2 also shows lower hysteresis and reduced charge trapping effects, contributing to better device reliability and energy efficiency. Additionally, WS_2 exhibits superior sensitivity in various sensing applications and can sustain higher current densities in electronic devices [91,92]. Its low charge-trapping tendency further contributes to device stability and reliability, making it particularly well-suited for advanced semiconductor technologies, including flexible and wearable electronics [96]. These application-specific advantages, especially in thermal resilience, carrier transport, and optical response, justify the selection of WS_2 as the active channel material in this research. They also highlight its strong potential for future semiconductor device technologies that require high performance, environmental stability, and scalability.

Table. 1.1: Comparative study of the properties and applications of WS_2 and MoS_2

Aspect	MoS_2	WS_2	Ref. No.
Optical Absorption	Strong absorption in the visible range	Broader absorption range, from visible to near-infrared	[75]
Bandgap (eV) (Direct and indirect bandgap)	~1.8 and ~1.2	~2.1 and ~1.4	[86]
Mechanical Strength (Gpa) (Young's modulus and Tensile strength)	~270 and ~16	~302 and ~47	[90, 97, 98]
Lubrication	Effective in dry and humid conditions; used in standard lubrication systems.	Superior performance in high-temperature and vacuum environments due to better stability and lower friction.	[91]
Oxidize temperature (^oC)	~400	~500	[91]
Melting temperature (^oC)	1185	1250	[99, 100]
Friction Coefficient	~0.15–0.20 (depends on conditions, such as vacuum or air)	~0.03–0.08 (efficient for extreme environments).	[92, 101]
Field-effect transistors: Operating performance	Moderate hysteresis, indicating acceptable but not optimal reliability.	Minimal hysteresis, ensuring greater stability and reliability in electronic devices.	[96]
Field Effect Mobility ($cm^2/V{\cdot}s$) (Depending on environment conditions, temperature and thickness)	~30 for monolayers	~33 for monolayer	[93]
Molar Mass (g/mole)	160.07	247.98	[102]
Density (g/cm^3)	5.06	7.5	
Solubility in water	Insoluble	Slightly soluble	

To fully explore the potential of WS_2 and other TMDs as semiconducting channel materials for FET applications, several challenges must be addressed. These materials require precise manipulation and enhancement of their physical and electrical properties, particularly carrier transport in devices. Research has shown that TMDs often suffer from crystal defects, which can result in low carrier concentrations [103]. Furthermore, the integration of TMDs with metal contacts in device applications frequently encounters high contact resistance [104]. This arises due to mismatches in work function and low binding energy at the Metal-Semiconductor interface [105]. In FET applications, the choice of dielectric also plays a pivotal role, as it significantly influences electrical characteristics, particularly in switching behaviour and carrier mobility [106]. Key

improvements are essential to enhance FET performance, including reducing contact resistance, increasing field-effect mobility, optimizing the I_{ON}/I_{OFF} ratio, and achieving a low subthreshold swing [104–106]. These advancements are critical for the development of high-performance WS_2-based FETs.

Defects in the atomic lattice may form during synthesis, leading to atomic vacancies, chemical reactions, or thermal effects such as high-temperature treatments or annealing [103]. To overcome these challenges, substitutional doping can be achieved by directly replacing atoms within the lattice or by introducing dopants at interstitial sites between the existing atoms. Additionally, the distinctive nature of the vdW gaps in 2D materials allows atomic dopants to intercalate between layers, which can modify the material's morphological and electronic properties. Achieving precise regulation of doping density in thin semiconductor materials becomes increasingly challenging when their thickness is reduced to just a few nanometers, especially when employing ion implantation methods. This is due to the inherent limitations of such techniques, which often involve high-temperature and high-energy particle-based processes that may cause damage to the material. In contrast, molecular doping presents several advantages. It relies on a simpler experimental setup and avoids the need for high-energy and high-temperature conditions, making it more suitable for delicate materials [107]. Additionally, molecular doping typically results in isotropic doping profiles, ensuring uniformity across the material, which is critical for maintaining consistent electronic properties in thin semiconductor layers [108]. This method has garnered considerable attention as a promising alternative for doping ultra-thin semiconductors.

This study explores several important aspects that differentiate it from prior research on WS_2-based FETs. It adopts a systematic Chlorine (Cl) doping strategy using an adsorption-based process applied to Liquid-Phase Exfoliated (LPE) few-layer WS_2 nanosheets. Unlike earlier approaches that primarily employed chemical doping on CVD-grown WS_2 films, this work utilizes a eco-friendly and scalable exfoliation technique in an aqueous medium with the assistance of an organic surfactant, where the surfactant functions as an exfoliating agent in an aqueous medium. Prior to device fabrication, the prepared WS_2 material was thoroughly characterized to evaluate its crystallinity and electrical properties. The back-gated WS_2-FET was fabricated on a SiO_2-coated Si substrate, where the SiO_2 layer serves as the back-gate dielectric, and WS_2 nanosheets

were deposited on its surface to form the FET channel. To enhance the operational performance of WS_2-FETs, various strategies were employed, including n-type doping and the use of different metal contacts, which significantly improve the device's operating efficiency. In addition, the fabricated back-gated WS_2-FETs were extensively analyzed using spectroscopic analysis and electrical characterization techniques. Furthermore, this study provides an in-depth and quantitative evaluation of the impact of Cl doping on key device parameters, such as Contact Resistance (R_C), Schottky Barrier Height (SBH), Field-Effect Mobility (μ_{FE}), Threshold Voltage (V_{th}), and SubthresholdS (SS). The combined improvements in these metrics, particularly the notable reduction in R_C and SBH and the enhancement of mobility, demonstrate a significant advancement in device performance. In addition, the fabrication of FETs using small-area WS_2 nanosheets is also explored in detail, addressing challenges associated with nanoscale material handling and integration. Additionally, the use of contactless lithography and a comparative analysis of different metal contacts (Ti and Cr) offer valuable insights into contact engineering for WS_2-based devices.

1.2. Research Objective:

The prime focus of the research centered on the fabrication of WS_2 FET which has been accomplished through the following objectives_

Objective I: Synthesis and characterization of a few-layer 2H-WS_2 nanoflakes by facile and low-cost exfoliation method

The synthesis of uniform few-layer WS_2 nanosheets using simple and inexpensive techniques is challenging due to the difficulty in controlling the thickness of the nanosheets. One of the primary objectives of the research work is the exfoliation of few-layered WS_2 nanomaterials from bulk nanosheets by facile, low-cost and eco-friendly methods. Process optimization to find the crystalline quality and structural morphology of WS_2 was explored. Synthesized nanomaterial was characterized by Raman spectroscopy, Photoluminescence (PL), UV-Visible spectroscopy (UV-Vis) and X-ray diffraction (XRD) for measuring the number of layers. Optical characterization was done by Field Emission Scanning Electron Microscopy (FESEM), High Resolution Transmission Electron Microscopy (HRTEM), and Atomic Force Microscopy (AFM) to investigate the structural properties of the nanomaterial.

Objective II: Investigation for reduced Contact Resistance and Schottky Barrier Height of Metal-WS_2 junction

In the fabrication of semiconductor devices, metal contacts play a crucial role by forming the interface between the metal and the 2D semiconductor (WS_2) junction. The binding energy of the metal with WS_2 and the difference in metal work function and semiconductor electron affinity determines the electrical transport properties of the device. WS_2 exhibits higher SBH when in contact with high work-function metals such as Au (5.6 eV), Pt (5.65 eV), Pd (5.12 eV), and Ni (5.1 eV). The presence of high R_C and SBH adversely affects the current transport characteristics of the device. Achieving low R_C and SBH in WS_2 through the use of low-work function metal contacts is difficult due to S vacancies in the lattice of WS_2 nanosheets. The stoichiometry of WS_2 nanosheets can also deteriorate during synthesis, resulting in voids where atoms are missing from the crystal lattice. This disruption hinders electron transport within the WS_2 channel, reducing the electrical conductivity of the WS_2 device. Doping, which involves the introduction of foreign atoms or impurities into the crystal lattice of WS_2, is employed to improve its electrical conductivity, R_C, and SBH at the Metal-WS_2 interface.

Objective III: Fabrication and Electrical Characterization of WS_2 n-FET

In the fabrication of WS_2 FETs, oxide-based gate dielectrics were used. The oxide-based FET fabrication employed mask-less lithography with a laser writing process to create back-gated WS_2-FET devices. This involved patterning metal contacts on the nanosheet surface using mask-less lithography, followed by e-beam evaporation for source and drain metal deposition. Post-fabrication, spectroscopic analysis confirmed the material quality and successful fabrication of the nanosheets. Electrical characterization of the fabricated FETs was performed using Current-Voltage (I-V) measurement with a parameter analyzer to extract electrical parameters.

1.3. Thesis Organization:

- **Chapter 1:** Outlines the detailed explanation of the motivation behind the research. It also provides an overview of the thesis, assisting the reader an easy guide for navigating the subsequent chapters and sections.

Chapter 1: Introduction

This chapter provides an in-depth overview of the research motivation behind studying WS_2-FETs, discussing their potential applications, advantages, and drawbacks within FET technology. It highlights the distinct advantages of WS_2 nanosheets, particularly their unique properties, which make them promising candidates for emerging transistor technologies, offering extremely high electron mobility, an excellent I_{ON}/I_{OFF} ratio, and scalability for miniaturized devices. I have thoroughly reviewed the benefits of WS_2-FETs, such as low-power operation and improved performance in flexible electronics, as well as their challenges, including fabrication methods, material stability, and integration with current technologies. This examination lays the essential groundwork for understanding how WS_2-based FETs can function in modern electronics.

- **Chapter 2:** A concise literature survey on the 2D-TMD material WS_2 in FET applications has been provided, focusing on its properties, challenges and strategies to address these issues for effective implementation in field-effect transistors.

In this chapter, the author presents a comprehensive literature review on the application of 2D-WS_2 in FETs. The discussion covers the fundamental properties of layered WS_2 structures studied to date, along with various techniques for modifying these properties. An in-depth overview of common synthesis methods is provided, followed by a discussion on the electronic device applications of WS_2. Special focus is given to improving the performance of multi-layered WS_2-based FETs, particularly for low-voltage operations while addressing key challenges and proposing solutions to overcome these limitations.

- **Chapter 3:** Synthesis of WS_2 Nanosheets Using Surfactant-Assisted Exfoliation Method

This chapter demonstrated the synthesis process of WS_2 nanosheets using the LPE technique in an aqueous solution using an organic exfoliating agent, a method that efficiently produces high-quality nanosheets. The structural properties of the prepared WS_2 nanosheets were carefully investigated using several spectroscopic analyses to find the layers number, material prosperity, nanosheet thickness, etc. to confirm successful exfoliation and examine the material's crystallinity. These analyses offered valuable insights into the electronic and optical characteristics of the WS_2 nanosheets, emphasizing their potential for semiconductor applications. The findings demonstrate that LPE is a

viable approach for scalable production, opening up possibilities for integrating WS_2 nanosheets into electronic devices.

- **Chapter 4:** Effect of Cl Doping on Structural and Electrical Properties of Exfoliated WS_2 Nanosheets

This chapter demonstrated the impact of Cl doping on the structural and electrical properties of exfoliated WS_2 nanosheets. By introducing n-type doping onto the surface of WS_2, aimed to enhance its electronic characteristics. Spectroscopic analysis was employed to investigate the effects of this doping process, which allowed us to observe notable changes in the material's electrical properties. Among the key findings were the modulation of contact resistance and Schottky barrier height, both of which are critical parameters in determining the performance of WS_2-based electronic devices. The results demonstrate that Cl doping effectively tunes the electrical behaviour of WS_2, making it a promising approach for optimizing its performance in various applications, including transistors and other nanoscale electronic components.

- **Chapter 5:** Fabrication and Characterization of WS_2-FET

In this chapter, the fabrication and electrical characterization of WS_2-based FETs is presented. The research explores the intricate details of the fabrication process, focusing on critical factors such as the selection of materials, including dielectrics, substrates, and metal contacts. The back-gated WS_2 FET was fabricated on a SiO_2 layer, which, functions as a back gate dielectric in this device configuration. The chapter outlines essential steps in the fabrication, such as material deposition, patterning, and device integration. Furthermore, a comprehensive analysis of the electrical performance of the WS_2 FETs highlights how the dielectric materials contribute to enhancing characteristics like threshold voltage, mobility, and the I_{ON}/I_{OFF} ratio. These findings emphasize the potential of WS_2 as a leading candidate for future electronic devices.

- **Chapter 6:** Conclusion and Future Direction of Research

The conclusion summarizes the thesis, evaluating the key contribution of WS_2 in FET application. It underscores the material's advantages in enhancing the electronic properties of FETs while also addressing the challenges that need to be resolved for its successful integration into FET applications. It also expands the scope by proposing areas

for further investigation and exploring potential directions for future research to build on the current study.

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