CHAPTER 5

Fabrication and Characterization of WS_2-FET

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Chapter 5: Fabrication and Characterization of WS_2-FET

5.1. Introduction:

The semiconducting nature of WS_2 nanosheets has sparked considerable interest in FET applications due to its unique properties and compatibility with atomically thin device architectures[1–4]. WS_2 nanosheets, with a tunable bandgap larger than that of traditional silicon-based semiconductors, make a compelling case for next-generation FETs [5, 6]. This tunable bandgap can be engineered according to application needs, providing versatility in device performance [7–10]. However, WS_2-based FETs face challenges related to stability, as environmental effects degrade the intrinsic properties of WS_2 over time. This degradation negatively impacts the performance of WS_2 as a channel material, leading to reduced operating efficiency and reliability of WS_2-based FETs in practical applications [11, 12]. Numerous studies have shown that the mobility of CVD-grown WS_2 devices, ranging from 5.8 to 33 cm^2/ V.s, is significantly lower than the theoretically predicted values. This discrepancy is primarily attributed to factors such as interfacial charged impurities, surface traps, roughness of the underlying dielectric layer, atomic defects or vacancy etc. [13]. The interfacial characteristics, along with the inherent dielectric properties of the insulating layer, present significant challenges in device fabrication and electrical transport [15,16]. Furthermore, the process of transferring WS_2 flakes onto target substrates has a significant impact on the quality and performance of the device [16, 17]. For the fabrication of WS_2-based FETs, both liquid and dry transfer techniques are widely used, each of which offer distinct challenges in the transfer process, with results to the maintenance of nanosheets structural integrity and minimizing contamination [7,19,20]. The dry technique stands out among the two due to its simple transfer process, cost-effectiveness and high yield. However, it is often time-consuming which require careful handling to ensure precision and maintain the pristine properties of the material. Optimizing these transfer methods is crucial to ensure transfer stability and achieve superior electrical performance of fabricated devices.

The structures of 2D material-based FETs can be categorized into three types: back-gated, top-gated, and dual-gated, as depicted in Fig. 5.1. Each of these device structures presents specific challenges and applications. Illarionov et al. have highlighted that achieving a damage-free transfer of the oxide layer onto 2D materials remains a significant challenge [20]. This difficulty is particularly critical as it exacerbates the stability issues in 2D material-based electronic devices. These stability limitations

primarily arise from charge trapping caused by defects in the oxide layer, located near the channel/oxide interface. Choi et al. reported that when Al_2O_3 is used as a top gate on an MoS_2 surface, shallow and deep-level traps are present at or near the ALD-grown Al_2O_3 [21]. The existence of charge traps can result in transfer curve hysteresis of FET, which are often found at the interface between the semiconductor channel and the dielectric layer. The presence of traps can arise from various factors, including surface defects, impurities, or defects in the dielectric material. When the gate voltage is applied, charge carriers can become trapped at the dielectric-channel interface of FET, causing a delay in the device's response, as shown in Fig 5.1(a & b). As the gate voltage is swept back, the trapped charges are gradually released, leading to a shift in the transfer curve and resulting in hysteresis [22]. This hysteresis can significantly impact FET performance, causing instability in switching behaviour and affecting the device's reliability. Additionally, hysteresis can lower the on/off current ratio, degrade the threshold voltage, and increase power consumption due to energy loss from the charging and discharging of traps. Furthermore, hysteresis can cause inconsistencies in the current-voltage characteristics, making it difficult to control the FET's switching operation with precision.

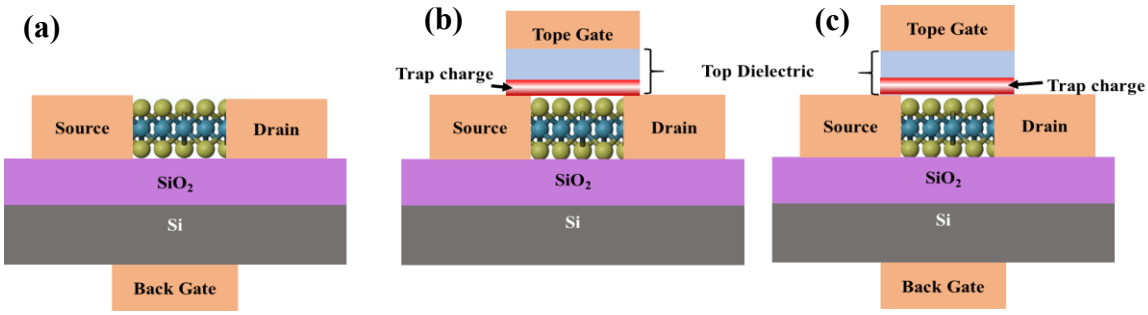

Fig. 5.1: Illustrative representation of the various 2D-FET structures. (a) Back-gate FET, where the gate electrode is located beneath the dielectric layer and the channel material. (b) Top-gate FET, where the gate electrode is positioned on top of the channel material with an insulating layer separating them (c) Dual-gated FET, which incorporates both top and back gates

A dual-gated FET features a sophisticated device architecture that incorporates two gate electrodes: a top gate positioned on the surface of the nanosheet and a back gate located on the backside of the device [23]. This configuration provides improved electrostatic control over the channel, enhancing the device's overall performance and

functionality. However, it shares similar limitations with top-gated FETs. Additionally, for MX_2 materials, challenges such as the absence of chemical bonds at the 2D surface, difficulties in dielectric deposition, and the scaling of the Equivalent Oxide Thickness (EOT) remain significant obstacles [24].

In this chapter, the fabrication and characterization of back-gated FL-WS_2-FET is presented. The devices were fabricated using Si/SiO_2 substrate where SiO_2 acts as the back-gate dielectric. The SiO_2/Si substrate is commercially available and it reduces fabrication complexity by eliminating the need for the deposition of gate dielectric. The back gate design is ideal for academic research of TMD-based FETs as it allows consistent gate control, facilitating the study of 2D materials such as WS_2 material which acts as a channel material [25,26]. The back-gated structure in 2D material-based FETs facilitates effective electrostatic manipulation of the channel, allowing for efficient modulation of charge carriers [17]. This leads to a higher current on/off ratio, reduced leakage current, and improved performance by minimizing interface traps [25]. As a result, the device experiences enhanced carrier mobility and greater stability, contributing to overall improved functionality and reliability. Furthermore, this design enables the investigation of device performance with limited intricacy in manufacturing, making it a perfect setting for initial material analysis and proof-of-concept research. The back-gated FET structure is well-suited for initial studies and characterization of 2D material-based FETs, providing a simple and efficient platform for evaluating device performance. However, its scalability and adaptability for more complex electronic systems present challenges that must be addressed when transitioning to more advanced device architecture [9,23]. Despite these limitations, back-gated FETs remain a reliable choice for WS_2-based research, offering a solution for the preliminary evaluation of device performance in the early stages of development [28].

To understand the influence of fabrication parameters, variations in device performance were systematically analyzed by employing different metal contacts and adjusting the channel lengths. To achieve a micron-scale channel, the source and drain contact regions were meticulously patterned using mask-less lithography, ensuring precise alignment and enhanced device reproducibility. Spectroscopic methods were employed to study and optimize the device structure, position of WS_2 nanosheet, etc. both pre and post-fabrication, ensuring robust stability and high-quality interfaces. The electrical transport characteristics of the fabricated WS_2-FET offer detailed insights into

the device's performance. Key parameters such as field-effect mobility, on/off current ratio, and subthreshold swing were derived from I-V measurements performed with a parameter analyzer. These findings demonstrate the promising potential of WS_2-based FETs in advanced semiconductor technology applications. The challenges in the fabrication process are also highlighted. Furthermore, the use of different metal contacts, variations in channel length and doping levels offer critical insights into the M-S interface, carrier concentration, mobility, and overall performance of the FETs.

5.2. Experiment:

5.2.1. WS_2-FET Fabrication:

Fig. 5.2 represents the fabrication process steps of the back-gated WS_2 FET began on a Si substrate coated with 300 nm SiO_2, which served as the back-gate dielectric. Prior to transferring the nanosheet, one side of the SiO_2 layer on the Si substrate was etched using Hydrofluoric Acid (HF), then rinsed with DI water and dried using a Nitrogen (N_2) flow. Then the HF-treated SiO_2-coated Si substrate was thoroughly cleaned with ACE, IPA, and DI water for 15 minutes each in a bath sonication and then dried with a flow of N_2 to eliminate any remaining impurities or particles from the substrate.

To make a WS_2 channel for FET, the WS_2 flake was transferred onto the SiO_2 substrate using a dry transfer method with scotch tape, as shown in Fig 5.2(a). Initially, a few-layer WS_2 nanosheet was obtained via liquid-phase exfoliation from bulk WS_2 powder then the exfoliated nanosheets were deposited onto the Si substrate and dried at 60 °C for an hour. The exfoliation process of a few-layer WS_2 flake is comprehensively discussed in Chapter 3. Then the exfoliated nanosheets were transferred using scotch tape onto the SiO_2 surface, eliminating the need for additional chemicals or high-temperature process.

Fig. 5.2(b-d) represents the photolithography process used as the patterning technique to define the source-drain contacts and the channel area. Prior to the lithography process, a positive photoresist was applied to the WS_2-coated SiO_2 substrate through spin-coating at 2000 rpm for 60 seconds. The coated substrate was then baked at 120 °C for 5 minutes to ensure proper adhesion and uniformity of the photoresist layer. The photolithography process was carried out using a high-resolution laser lithography system (Dilase 250, 50× magnification), featuring a 1 μm laser spot size and a writing speed of over 100 mm/s. The system is equipped with an inbuilt camera that enables precise

identification of particles on the substrate, facilitating accurate patterning of the selected region. In this process, a design was created using K-layout software to define the specified contact area at precise locations on the substrate. During the WS_2-FET fabrication, the prepared pattern was transferred onto a single WS_2 flake using a precise line-by-line laser writing technique as depicted in Fig. 5.2(c).

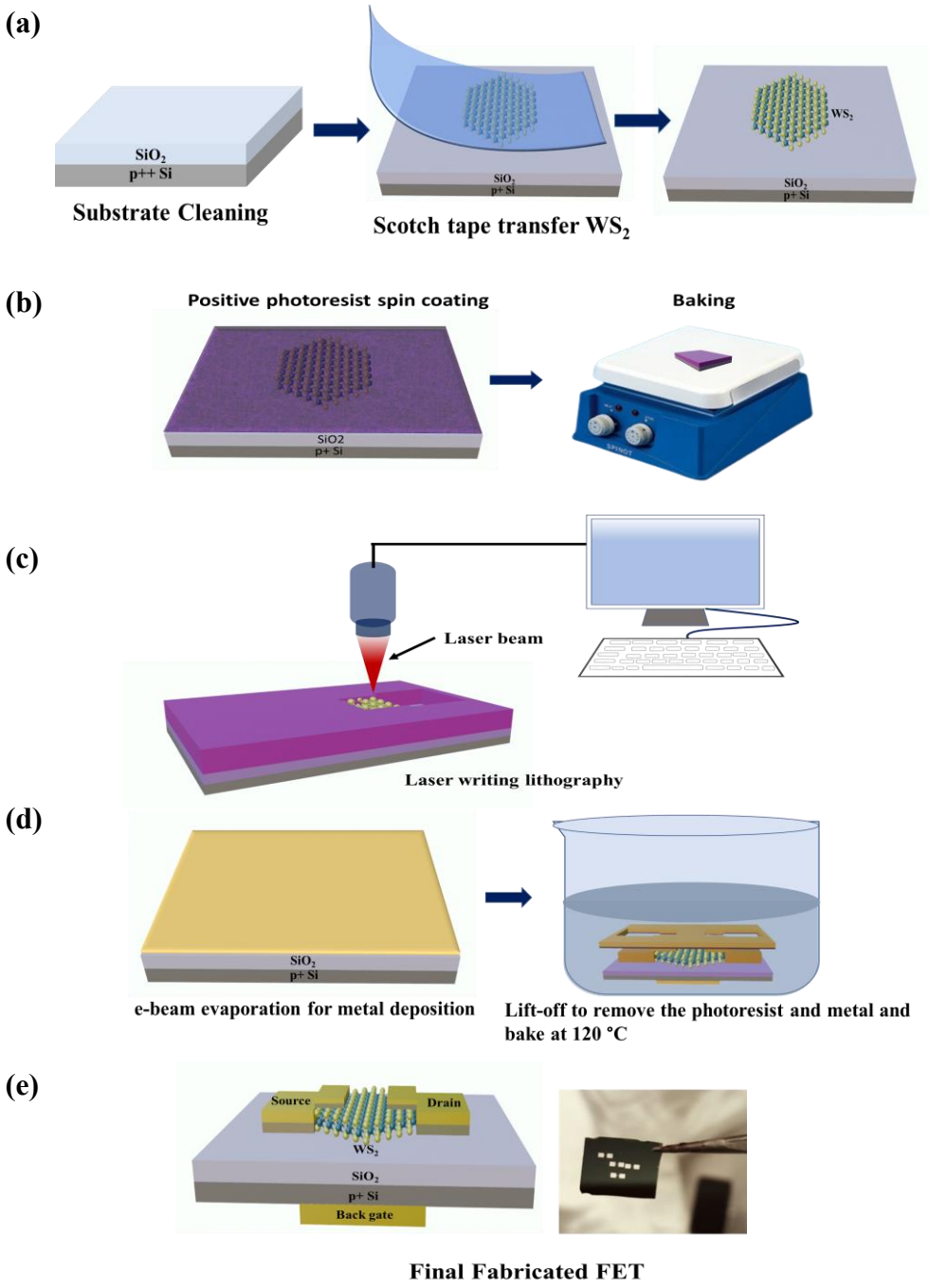

Fig. 5.2: Schematic depiction of the sequential steps of the device fabrication using contactless photography process

However, creating a microchannel of a few microns on a small nanosheet (<10 μm) is extremely challenges due to potential pattern overlaps. Conventional photolithography poses challenges in fabricating channel lengths below ~8-10 μm. Achieving patterns in areas smaller than 10 μm is particularly difficult, as it requires precise alignment of the lithography mask on the substrate. To address these limitations, the fabrication of the FET was carried out using a two-step lithography process using laser writing photolithography. This approach ensures greater precision in patterning and allows for the realization of micron-scale spacing between contacts on the WS_2 surface. A channel area of 2-4 μm x 5 μm is successfully patterned without requiring external masks using two-step laser writing photolithography. This method offers an alternative approach for fabricating 2D-FET devices by overcoming the challenges of contact lithography, particularly the difficulty of accurately aligning patterned masks on nanosheets smaller than 10 μm.

First, the pattern for one side contact area was exposed to the laser, with the corresponding pattern file applied to a specific region of the WS_2 nanosheet. After defining one side of the contact area, the laser-exposed substrate was developed in a photoresist developer solution for ~30 seconds to dissolve the illuminated region. It was then rinsed with DI water, dried with a N_2 flow and baked at 120 °C for 5 minutes to remove any remaining residues from the exposed area.

The Metal electrodes of Cr/Ag and Ti/Ag(~5/70 nm thick) were deposited using e-beam evaporation. Excess metal and photoresist were removed through a lift-off process, which involved soaking the substrate in acetone at room temperature for 10-15 minutes, as shown in Fig. 5.2(d). To eliminate any remaining metal particles, a gentle flow of N_2 was used to wash away the impurities.

After successfully preparing the metal contact on one side of the WS_2 flake, the opposite side of the contact area was patterned using the same process. This process involved applying a layer of photoresist, followed by metal deposition, and finally, a lift-off technique. However, precise control over the contact area is crucial due to the small size of the flake and the micron-scale spacing required between the contacts. Lastly the back side of the metal contact Aluminium (Al) which acts as a gate contact was deposited through thermal evaporation. The final device structure is depicted in Fig. 5.2(e).

High-resolution optical microscopy was employed to obtain clear images of the device structure to verify the morphology and correct placement of metal contacts on the

nanosheet surface. Additionally, the fabricated FET nanosheets were first analyzed using Raman spectroscopy with a 532 nm laser source (Raman Model: CPX100) and further the structural morphology of the nanosheets were examined using AFM and FESEM.

5.2.2. Electrical Characterization of WS_2-FET:

The structural and morphological properties of the fabricated FET were analyzed using spectroscopic techniques, while the electrical characteristics of the back-gated WS2 channel-based FET device were evaluated by applying a DC voltage. Measurements were performed in a dark chamber at room temperature.

5.3. Results and Discussion:

5.3.1. Spectroscopic Analysis of WS_2 Film Before and After Fabrication:

Raman spectroscopy is a premier high-resolution technique essential for the detailed study of the fundamental properties and structural characteristics of 2D materials. The Raman spectra were measured using a 532 nm laser, and displayed two vibrational peaks between 300-500 cm^{-1} which appear on the x-axis of the Raman spectra, corresponding to the A_{1g} and E^1_{2g}modes as shown in Fig. 5.3(a). The Raman spectra were meticulously recorded before and after the fabrication processes. The intensity difference between the A_{1g} and E^1_{2g}peaks is ~65 cm^{-1}, indicating a few-layer nanosheets [29–31]. In addition, a second-order longitudinal acoustic 2LA(M) mode is identified at 347.91 cm^{-1} for pre and post-lithography processed samples. Although this 2LA(M) mode overlaps with the first-order E^1_{2g}mode, the application of multi-peak Lorentzian fitting techniques allows for the precise determination of peak positions within the spectra, as depicted in Fig. 5.3(b). Interestingly, while the lithography process does not alter the positions of the peaks, there is a slight decrease in intensity, which is likely attributed to impurities introduced during the fabrication process.

The optical characteristics of the exfoliated WS_2 nanosheets after device fabrication were thoroughly investigated using PL measurements conducted on the same instrument with an excitation wavelength of 532 nm at room temperature. As shown in Fig. 5.3(c), a prominent emission peak corresponding to the A-exciton was observed for the WS_2 nanosheets [32]. It is noteworthy that the position of this peak remained constant

despite variations in the excitation wavelength, although the peak's intensity either decreased or dispersed. A distinct sharp peak observed near 1.8 eV (equivalent to 655 nm) corresponds to the indirect band gap emission, signifying the presence of few-layer WS_2. Fig. 5.3(d) shows the examination of the WS_2-FET structure after fabrication, where an optical microscope was used to inspect the contact area and verify the correct placement on the nanosheet surface.

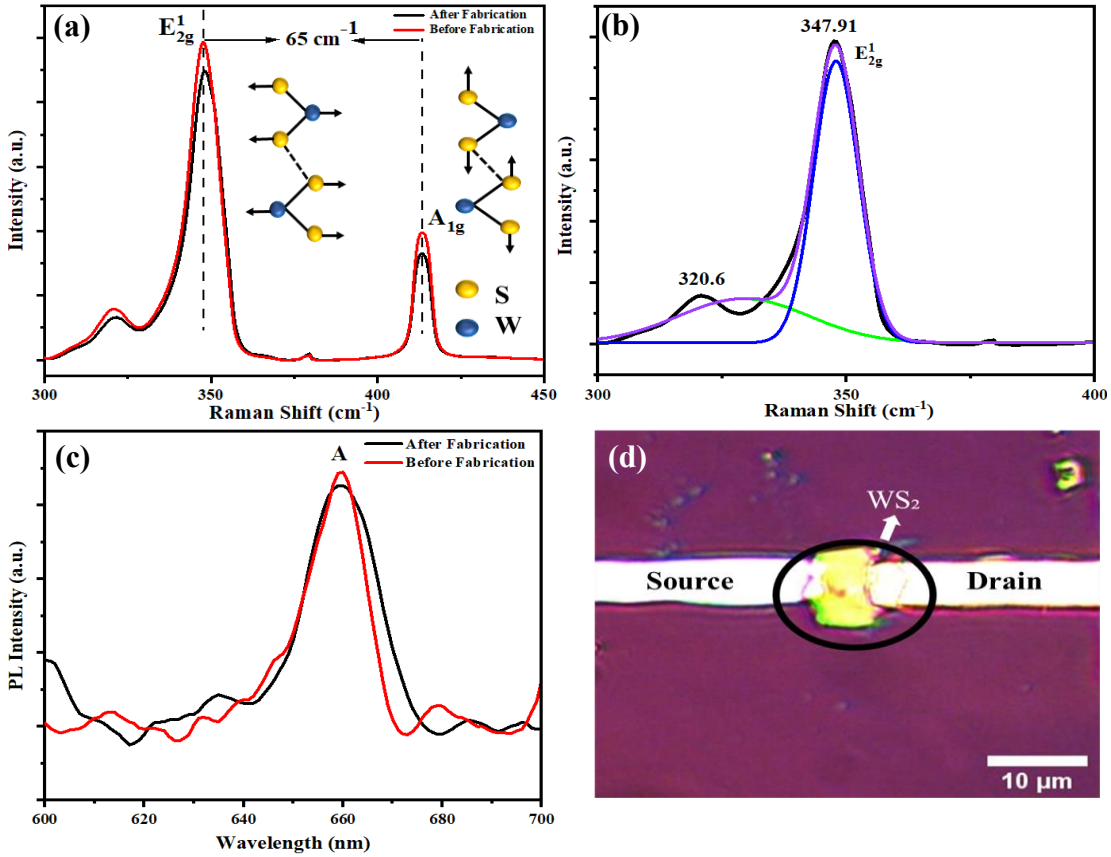

Fig. 5.3: (a) Raman Spectroscopy of the FL-WS_2 nanosheet before and after lithography-based fabrication (b) spectral fitting with Lorentzian curves for 2LM and E^1_{2g} and (c) PL Spectroscopy of the exfoliated WS_2 nanosheets and (d) Optical microscopic image of the photolithography patterned FL-WS_2 FET device

AFM measurement was conducted for the fabricated device using tapping mode under ambient conditions, as shown in Fig. 5.4. The detailed analysis of the surface roughness of WS_2 was made. The AFM images reveal that the WS_2 surface exhibits significant roughness, likely due to the presence of impurities or residues of photoresist during the fabrication process. The measured average thickness of the WS_2 layers was found to be less than 10 nm, suggesting that the thin WS_2 flakes consist of only a few

layers. Fig. 5.5(a) shows the FESEM image of the WS_2 device show that the metal electrode was is align perfectly with the same WS_2 flake. The precise alignment and spacing are very important for proper electrical contact with the metal electrode to function the device efficiently.

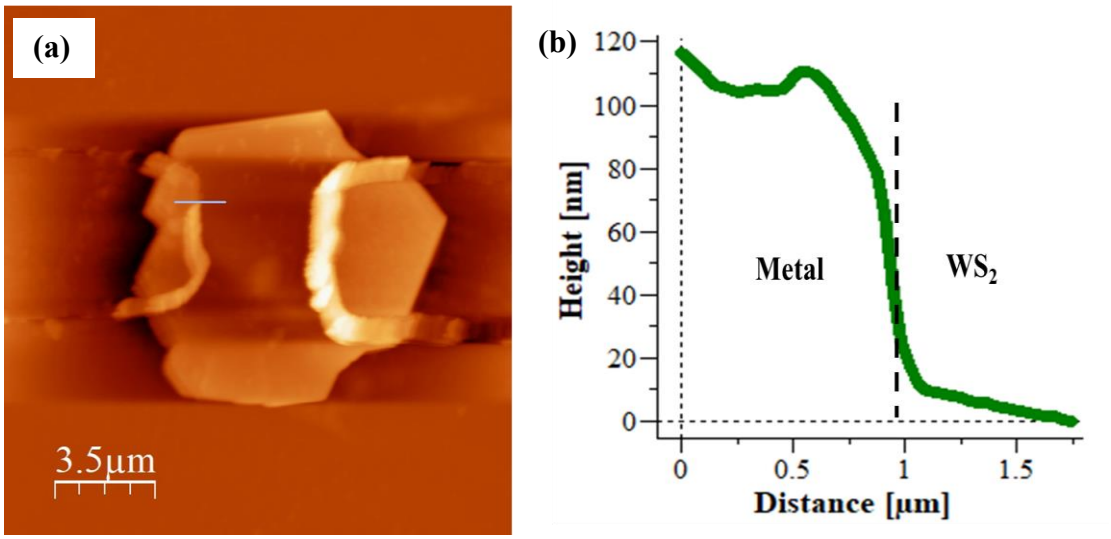

Fig. 5.4: (a) AFM image of the Fabricated FL-WS_2 device with <10 nm thick nanosheet and (b) corresponding height profiling of the Metal and WS_2 after the fabrication of the FET

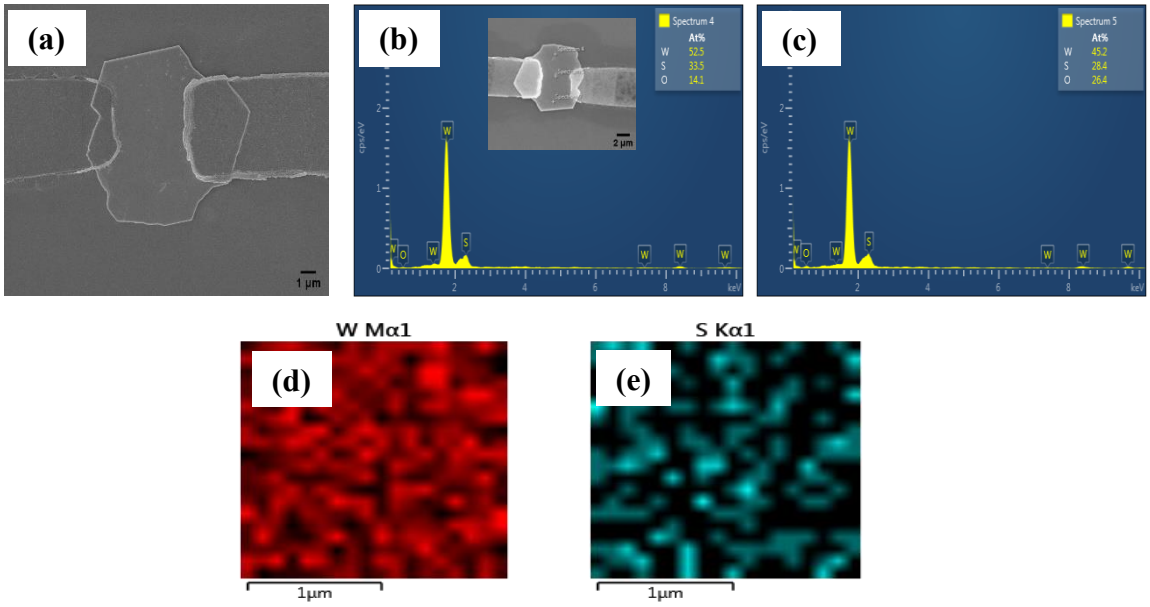

Fig. 5.5:(a) FESEM image of the Fabricated FL-WS_2 device, (b & c) EDX spectra of the FL-WS_2 flake captured from different regions of the nanosheet and (d-e) corresponding colour mapping of the W and S atoms in the WS_2 flake.

Fig. 5.5(b-e) shows the EDX analysis of WS_2 after the fabrication of the FET. The elemental mapping of WS_2 provides an intuitive visualization of the distribution of W and S elements across the examined region. These distributions were quantified in terms of their atomic percentages, as shown in the EDX spectra. The analysis revealed that the atomic percentage of S atom (~33% and ~28%) indicated in the Fig. 5.5 (b & c) which is significantly lower than that of W atom (~52% and ~55%). This discrepancy could be attributed to vacancies created in the atomic lattice during the exfoliation process [2]. However, the presence of O atoms in the WS_2 nanosheet is attributed to their ability to occupy the vacant sites of S atoms. Due to the presence of S vacancies in the WS_2 lattice, O atoms occupy these vacant positions during the exfoliation and device fabrication processes. In the previous chapter, we discussed that the presence of O atoms and S vacancies within the atomic lattice of WS_2 can lead to a reduction in the bandgap of WS_2. Moreover, the observed lower S atomic ratio and the presence of O atoms imply that S vacancies in WS_2 could significantly impact the electrical properties of WS_2-based FET devices. These vacancies could alter charge transport and influence device performance.

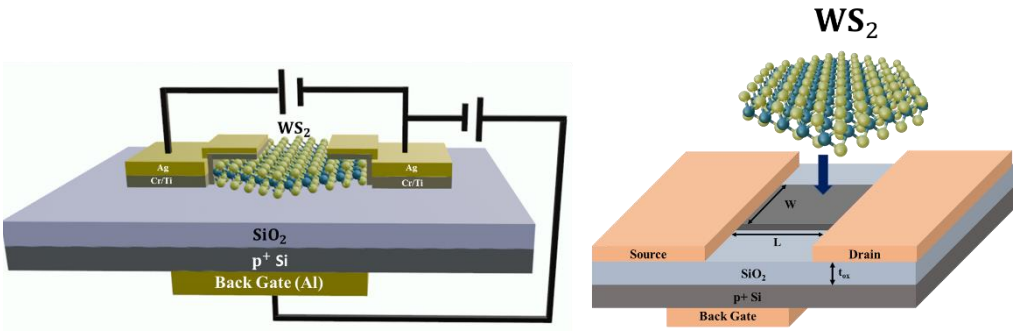

Fig. 5.6: Schematic depiction of the back gated WS_2-FET structure on SiO_2/Si substrate

5.3.2. Electrical Characterization of WS_2-FET:

To examine the operating performance of the fabricated WS_2-FET, the electrical measurement was performed using a Keithley SCS 4200 semiconductor parameter analyzer at room temperature. Key electrical properties such as contact type (ohmic or Schottky), R_C, V_{th}, μ_{FE}, etc of back-gated WS_2-FET were analyzed. The device structure and bias configuration to studying characteristics of FET is shown in Fig. 5.6. The output characteristics of the WS_2-FET, where drain current (I_{ds}) is plotted as a function of Drain-Source Voltages (V_{ds}) at a constant Gate-Source Voltage (V_{gs}). Ag is used as the metal contact. Two different metals Ti and Cr were used as adhesion layers for the FET

fabrication. Two FETs were fabricated on separate flakes, each with a thickness of less than ~10 nm. The FETs' L is approximately 2 μm, while the W is about 5 μm. The analysis of I_{ds}-V_{ds} measurements provides detailed insights into the nature of the metal contacts, whether ohmic or Schottky. A comparative study of different contact types and their impact on the FET's performance has been conducted in detail, highlighting their influence on key device characteristics.

Fig. 5.7(a & b) illustrates the schematic representation of a back gated WS_2-FET structure with Cr/Ag contact and Ti/Ag contact. The output characteristics of the WS_2-FET, as shown in Fig. 5.7(c), demonstrate non-ohmic behaviour. A non-ohmic contact often signifies the presence of a SBH at the M-S interface, the schematic energy band diagram is depicted in Fig. 5.7(d) [33]. The high barrier height is formed due to the mismatch between the χ_S and the Φ_M [34]. Reported findings indicate that few-layer WS_2 forms n-type contacts when interfaced with low-work function of metals ($\Phi_M<\Phi_{WS_2}$). In an ideal case, the barrier height is calculated as the difference between the χ_S and Φ_M. For WS_2, the electron affinity varies from ~4.7 eV for a monolayer and ~4.4 eV for multilayers. Comparatively, the work functions of Cr (Φ_{Cr}) is 4.5 eV and Ti (Φ_{Ti}) is 4.3 eV, respectively [6, 35]. However, the work function of Cr is approximately equal to or slightly higher than the electron affinity of few-layer WS_2 nanosheets [36]. This minimal difference can restrict efficient electron injection across the metal-WS_2 interface, potentially increasing the R_C and SBH. In addition, the layered structure of WS_2, along with the presence of numerous dangling bonds at the metal-WS_2 interface, makes it more prone to defect states compared to bulk materials. These defect states result in Fermi-level pinning, causing the SBH to deviate from the theoretical predictions of the Schottky-Mott rule [37]. These factors can adversely impact the performance of FETs by reducing current flow and degrading the overall device efficiency. Despite the presence of a SBH, electrons at the source contact, induced by the gate bias, can facilitate field emission, reducing the depletion layer and increasing the tunneling current. As a result, the drain current I_{ds} increase as the V_{gs} is raised [38].

The output characteristics of the corresponding FET device exhibit nearly ohmic behaviour, as shown in Fig. 5.7(e). The Ti metal in contact with WS_2 in FET device signifies a low barrier height at the metal-semiconductor junction due to a thinner depletion layer as depicted in Fig.5.7(f). The FET with Ti/Ag contacts exhibits greater

drain current I_{ds} compared to the Cr-contact-based FET, due to is low Schottky barrier and reduced contact resistance at the Ti/Ag interface.

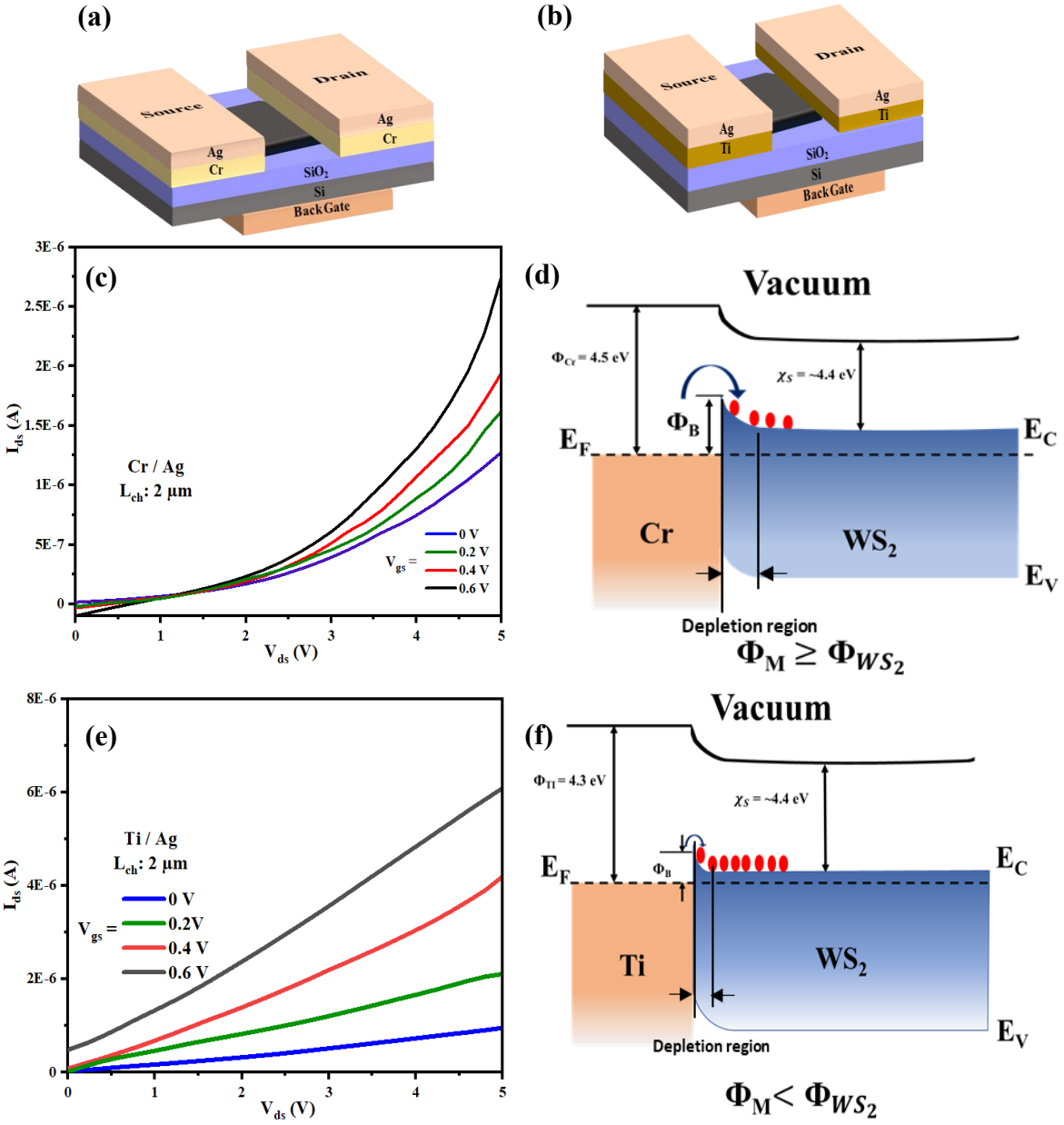

Fig. 5.7: Schematic depiction of WS_2-FET device structure with a channel length of ~2 µm: (a) Cr/Ag metal contact and (b) Ti/Ag metal contact-based FET, (c) output characteristics (I_{ds}-V_{ds}) of Cr/Ag contact based WS_2 FET and (d) corresponding energy band diagram of Cr-WS_2 interfaces (e) output characteristics I_{ds}-V_{ds} of the Ti/Ag contact based WS_2-FET (f) energy band diagram of Ti-WS_2 interfaces

To assess the comprehensive performance of the device and obtain key electrical metrics, it is crucial to study the transfer characteristics of the FET. This involves plotting

I_{ds} as a function of gate voltage V_{gs} while keeping V_{ds} constant, as shown in Fig. 5.8 (a & b) for Cr and Ti contact-based WS_2-FET. Important parameters like V_{th}, SS, and μ_{FE} can be estimated by examining the transfer characteristics of the fabricated FETs. These parameters offer an understanding of the device's electrical characteristics, such as its I_{ON}/I_{OFF} ratio, current modulation, and the effectiveness of charge carrier movement through the WS_2 channel [39]. The V_{th} of a transistor is generally defined as the point at which the drain current starts to diverge from its exponential behaviour in the subthreshold region as the gate-source voltage is increased [40]. The V_{th} is a key parameter of FET, as it defines the device's switching characteristics and operating mode [41]. It determines the point at which the transistor transitions from the off state to the on state, making it essential for controlling current flow. Furthermore, there is a consistent trend between the values of V_{th} and the observed on-currents, where a lower V_{th} typically correlates with a higher on-current, highlighting the influence of threshold voltage on the device's performance. A noticeable positive V_{th} on the positive side of the V_{gs} axis is observed for all the FETs. The V_{th} was derived through linear extrapolation of the device's transfer characteristics as demonstrated in Fig. 5.9(a & c) [42]. The extracted V_{th} of the WS_2-FETs is ~0.9 V for the Cr contact and ~0.2 V for the Ti contact. This indicates that the Ti-WS_2 contact exhibits a lower threshold voltage compared to the Cr contact. However, both the FET shows n-type FET characteristics.

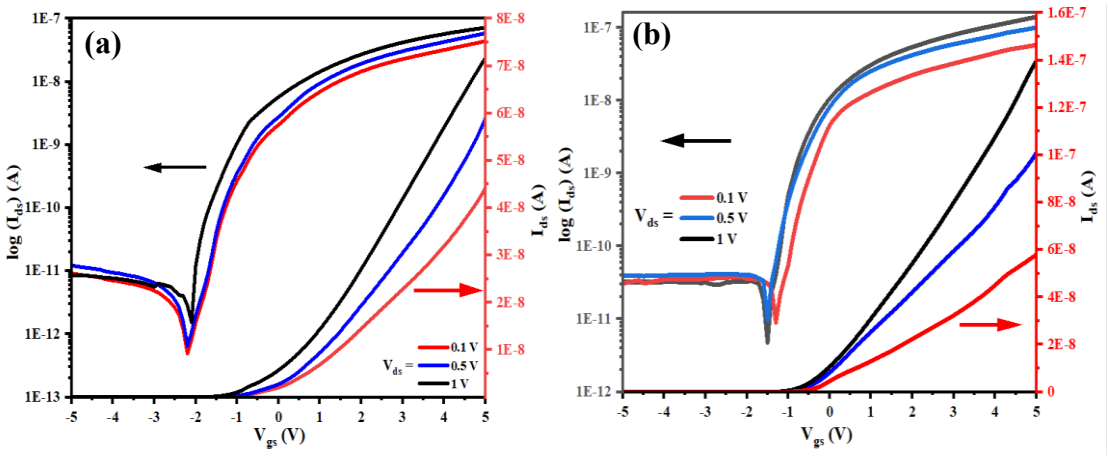

Fig. 5.8: Transfer characteristics I_{ds}-V_{gs} of the WS_2-FET for (a) Cr/Ag metal contact and (b) Ti/Ag metal contact for channel length of ~2 µm

Field-effect mobility is an essential parameter for FET that greatly influences the ON-state behaviour of the device. It assesses the velocity of charge carriers, such as electrons or holes travel through the transistor channel under an applied extremal bias

[43]. While intrinsic mobility is a fundamental material property determined by factors like crystal quality and scattering mechanisms, μ_{FE} is influenced by extrinsic effects, such as R_C at M-S interface [44]. High contact resistance can hinder charge injection, reducing the effective mobility and limiting device performance. The μ_{FE} represents a combination of the material's intrinsic properties and the device's practical constraints, highlighting the importance of optimizing both material quality and device design for improved performance. The μ_{FE} is extracted from the slope of the transfer curve of the FET and it can vary with V_{ds}. It is calculated using the following equation [45]_

$$\mu_{FE} = \frac{dI_{ds}}{dV_{gs}} \times \frac{L}{WV_{ds}C_{ox}} \quad (5.1)$$

Where, $\frac{dI_{ds}}{dV_{gs}}$ represents transconductance (g_m), L is the channel length and W is the channel width, and C_{ox} is the Oxide Capacitance of the SiO_2-coated Si substrate. Fig. 5.9(b & d) illustrates the extraction of transconductance g_m from the slope of the I_{ds}-V_{gs} plot in the linear scale. The calculated data demonstrate that the WS_2-FET device with a Cr metal contact exhibits a lower mobility of approximately 14 $cm^2/V{\cdot}s$ at room temperature. In contrast, employing a Ti contact in the WS_2-based FET enhances the mobility to around 25.03 $cm^2/V{\cdot}s$ for a channel length of ~2 μm, which is significantly higher compared to the Cr contact. The above findings clearly emphasize the significance of proper contact formation in optimizing the intrinsic properties of novel nanomaterials and demonstrate that the mobility value is improved by the use of Ti contacts.

The subthreshold slope is a fundamental metric for quantifying the switching efficiency and performance of FETs. For the fabricated WS_2-FET devices, the SS is determined from the log(I_{ds})-V_{gs} plot, by extracting the slope from the linear region of the transfer curve. This region corresponds to the exponential increase in I_{ds} with gate voltage V_{gs} when the device is transitioning from the off-state to the on-state. The estimated SS decreases from 0.6 V/dec for Cr contacts to 0.3 V/dec for Ti contacts. The SS is mathematically expressed by using the following equation [46]:

$$SS = \frac{d\,V_{gs}}{d\log I_{ds}}$$

$$= \ln 10 \frac{kT}{e}\left[1+\frac{C_{it}}{C_{ox}}\right] \quad (5.2)$$

Where k is the Boltzmann Constant, T is the operating temperature, e is the charge of an electron, and C_{it} is capacitance related to the Interface Trap Density (D_{it}) ~1.2 x 10^{11}

$eV^{-1}.cm^{-2}$ obtained by using the equation of ($D_{it} = \frac{C_{it}}{e}$). The presence of interface traps within the device can lead to an increased subthreshold swing, variability, and shift of the threshold voltage. A higher SS in the FET device requires a larger gate voltage to turn on the device.

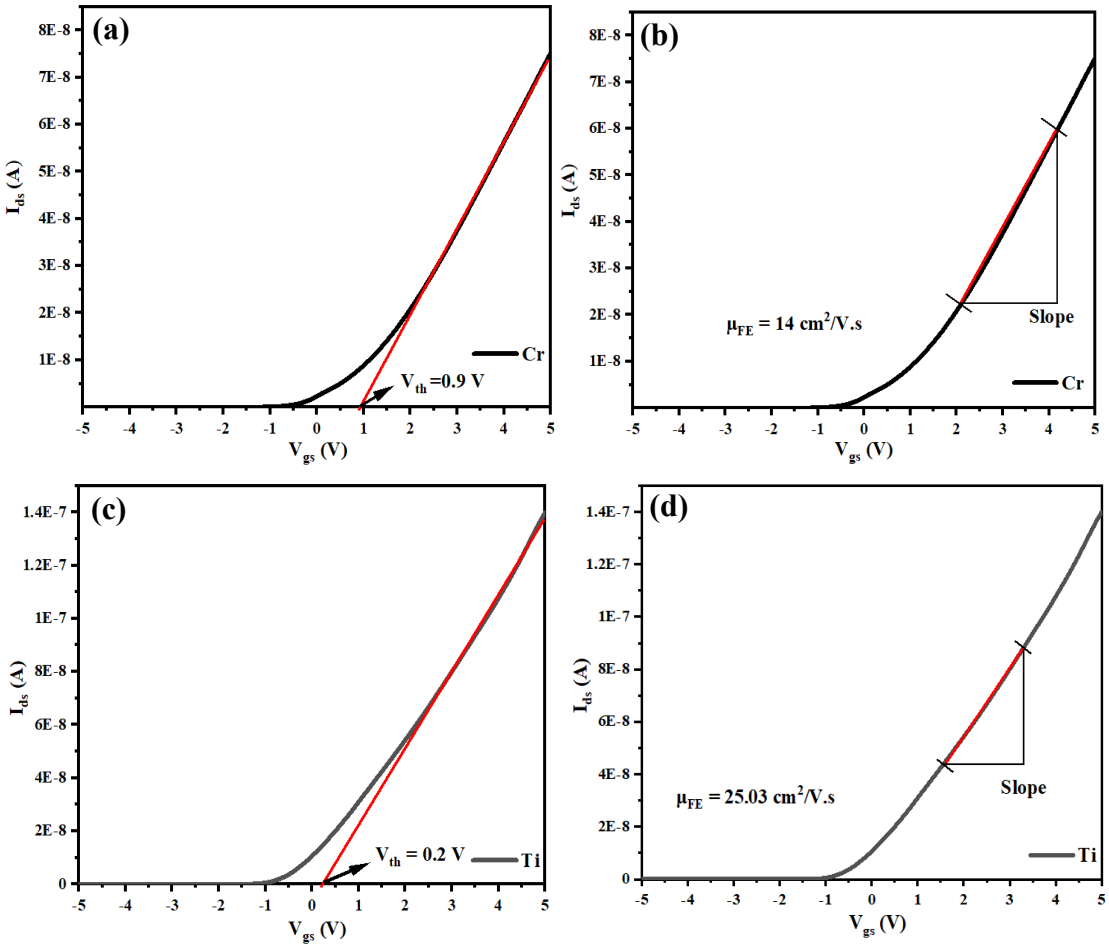

Fig. 5.9: Determination of V_{th} from the I_{ds}-V_{gs} plot of the WS_2-FETs and extraction of g_m from the slope ($g_m = \frac{dI_{ds}}{dV_{gs}}$) of the I_{ds}-V_{gs} plot in linear scale for (a & b) Cr contact-based WS_2-FET and (c & d) Ti contact-based WS_2-FET

Nevertheless, the Ti-WS_2 FET with a L_{ch} of ~2 demonstrated a higher value of I_{ON} current. The higher ON current is conversely correlated with the high drive current, low V_{th} and SS value, which allows for improving the channel conductance of the WS_2 -FET device. The I_{ON}/I_{OFF} ratio of the fabricated FL-WS_2 FET, obtained from the transfer characteristics of the device, is approximately ~10^4. This is determined by the ratio of the maximum current (I_{max}) at V_{ds} = 1 V to the minimum current (I_{min}) observed in the transfer

characteristics of the FET at room temperature and I_{min} is the lowest average value of the FET [47].

Compared to Cr contact-based WS_2-FETs, Ti contact-based devices exhibit superior performance characteristics, such as a lower threshold voltage, reduced subthreshold swing, and higher field-effect mobility. These results indicate that Ti-contact establishes a more efficient contact with WS_2 than Cr-contact, resulting in enhanced device performance. This improvement is primarily attributed to the lower work function of Ti compared to Cr [48]. The work function of a metal determines its ability to align the Fermi level at the metal-semiconductor interface. In the case of Ti, its lower work function places the Fermi level closer to the conduction band edge of WS_2, as illustrated in Fig. 5.7(f). This closer alignment reduces the Schottky barrier height for electron injection at the interface, thereby enhancing the efficiency of charge injection into the WS_2 channel. The improved alignment facilitates better electron transport, allowing the device to operate at lower threshold voltages and with higher conductivity.

5.3.3. Channel Length Variation of the WS_2 -FET:

The effect of channel length scaling on the electrical properties of WS_2-based FETs, including SS, V_{th}, On current (I_{on}), and μ_{FE}, was thoroughly examined. Fig.5.10 illustrates the output and transfer characteristics of WS_2-FETs for channel lengths of 3 μm and 4 μm. Furthermore, the variation of the resultant output current (I_{ds}) measured at a fixed V_{gs} and I_{on} current as a function of channel length is presented in Fig. 11(a & b) respectively. The I_{on} is extracted from their respective I_{ds}-V_{gs} plot of FET. A notable observation is that the I_{ds} and I_{on} current decreases significantly as the channel length increases, compared to shorter channel lengths. In these plots, the I_{on} current is specifically the maximum value of I_{ds} observed when the transistor is fully turned on, typically occurring in the saturation region of the I_{ds}-V_{gs} curve. The I_{on} current is a critical parameter that reflects the transistor's ability to conduct current when in the "on" state, which is directly linked to the device's switching performance and drive capabilities [39]. This trend highlights the critical role of channel length scaling in determining the device's electrical performance, which can be attributed to increased channel resistance and reduced charge carrier transport efficiency in longer channels.

In addition, V_{th}, SS and μ_{FE} of the FETs were analyzed, across different channel lengths. As represented in 5.11(c), V_{th} tends to increase with increasing channel length.

This increase can be attributed to the reduced influence of short-channel effects. With longer channel lengths, the gate's electrostatic control over the channel becomes less susceptible to interference from the drain, requiring a higher gate voltage to establish conduction.

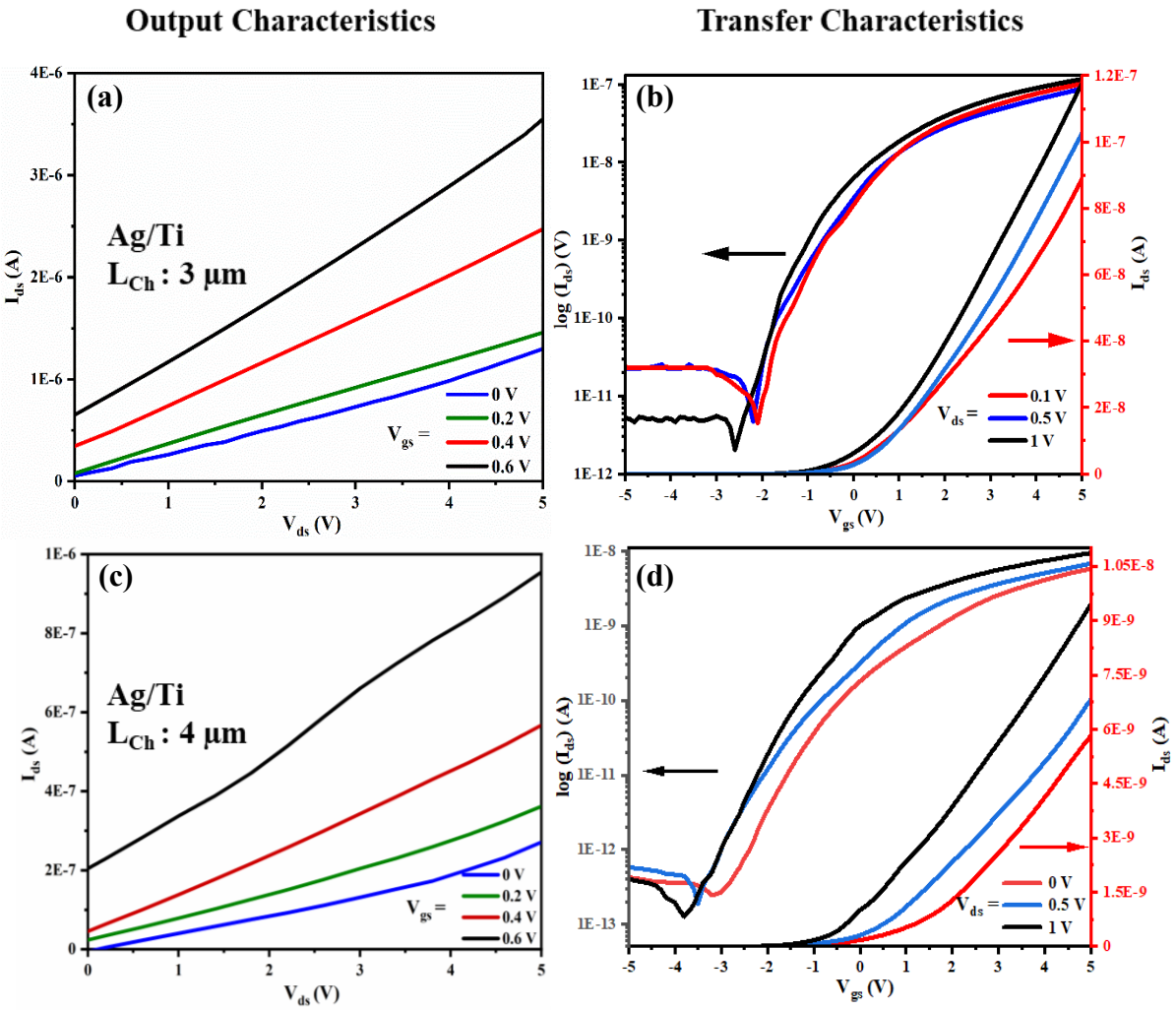

Fig. 5.10: I_{ds}-V_{ds} and I_{ds}-V_{gs} for the Ti contact based WS_2-FET for (a &b) 3 µm and (c & d) 4 µm channel length

The SS and μ_{FE} were also observed to vary with channel length. SS was found to increase with channel length, as illustrated in Fig. 5.11(d). A higher SS indicates a less efficient switching behaviour, demanding higher gate voltage to transition between states. This increase in SS with channel length can be attributed to the reduced ability of the gate to modulate the channel efficiently over longer distances. Similarly, the μ_{FE}, also increases with channel length, as shown in Fig. 5.11(d). In longer channels, the effects of carrier scattering, velocity saturation, and other short-channel effects are diminished,

allowing for more efficient charge transport [39]. While longer channels improve μ_{FE}, they also result in increased V_{th} and SS, which can negatively affect switching performance. These observations highlight the complex interplay between channel length and the electrical parameters, emphasizing the need to optimize channel dimensions for desired device performance [49].

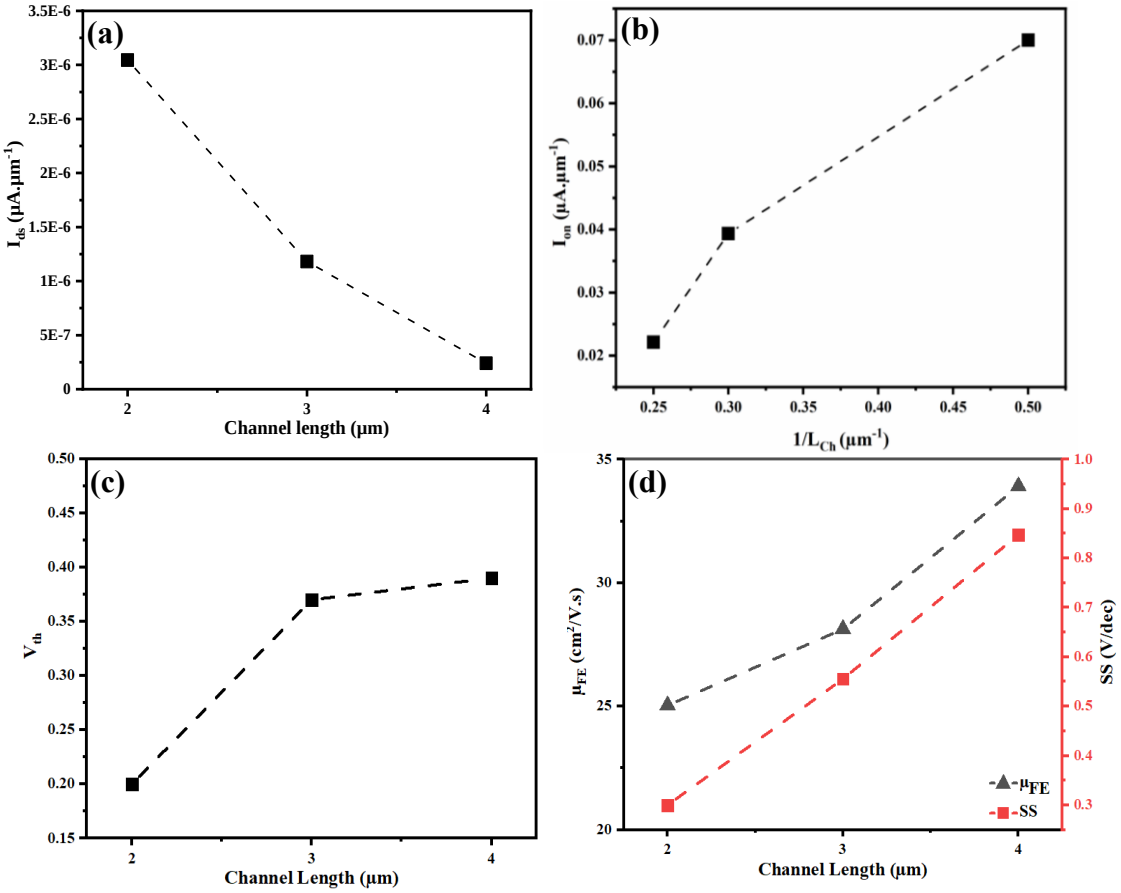

Fig. 5.11: (a) Variation of drain current I_{ds} from output characteristics of WS_2-FET with Ti contact (b) ON current of the FETs are plotted as a function of channel length (c) threshold voltage V_{th} extracted from the I_{ds}-V_{gs} plot (d) calculated field effect mobility μ_{FE} and subthreshold swing SS plotted as a function of channel length

5.3.4. Doping Effect in WS_2 FET:

After doping the WS_2 nanosheet with an n-type dopant material, a notable shift in the electrical characteristics of the WS_2-FET was observed, as illustrated in Fig. 5.12. The doping process was carried out on the WS_2 nanosheet surface through an absorption method, using chlorine (Cl) atoms as an n-type dopant. This n-type doping led to an increase in the drain current, which in turn enhanced the field-effect mobility. The dopant

atoms introduced interface defect states within the semiconductor, increasing the carrier concentration at the contact interface [50]. The detailed process of doping the WS_2 nanosheets is described in Chapter 4. This shift may have altered the Fermi level pinning position, leading to a reduction in the Schottky barrier height and contact resistance at the interface of Metal-Semiconductor [51].

In addition, key electrical parameters of the FET, such as field effect mobility, SS, and contact resistance, were calculated. After doping, the WS_2-FET with Cr/Ag contacts exhibited improved conductivity, with the mobility and SS enhanced from ~14 $cm^2/V{\cdot}s$ to ~102 $cm^2/V{\cdot}s$ and 0.6 V/dec to 0.24 V/dec, respectively. The extracted data demonstrate that the device's ON current also increased due to doping, which facilitated the improvement of the carrier concentration through electron injection [51].

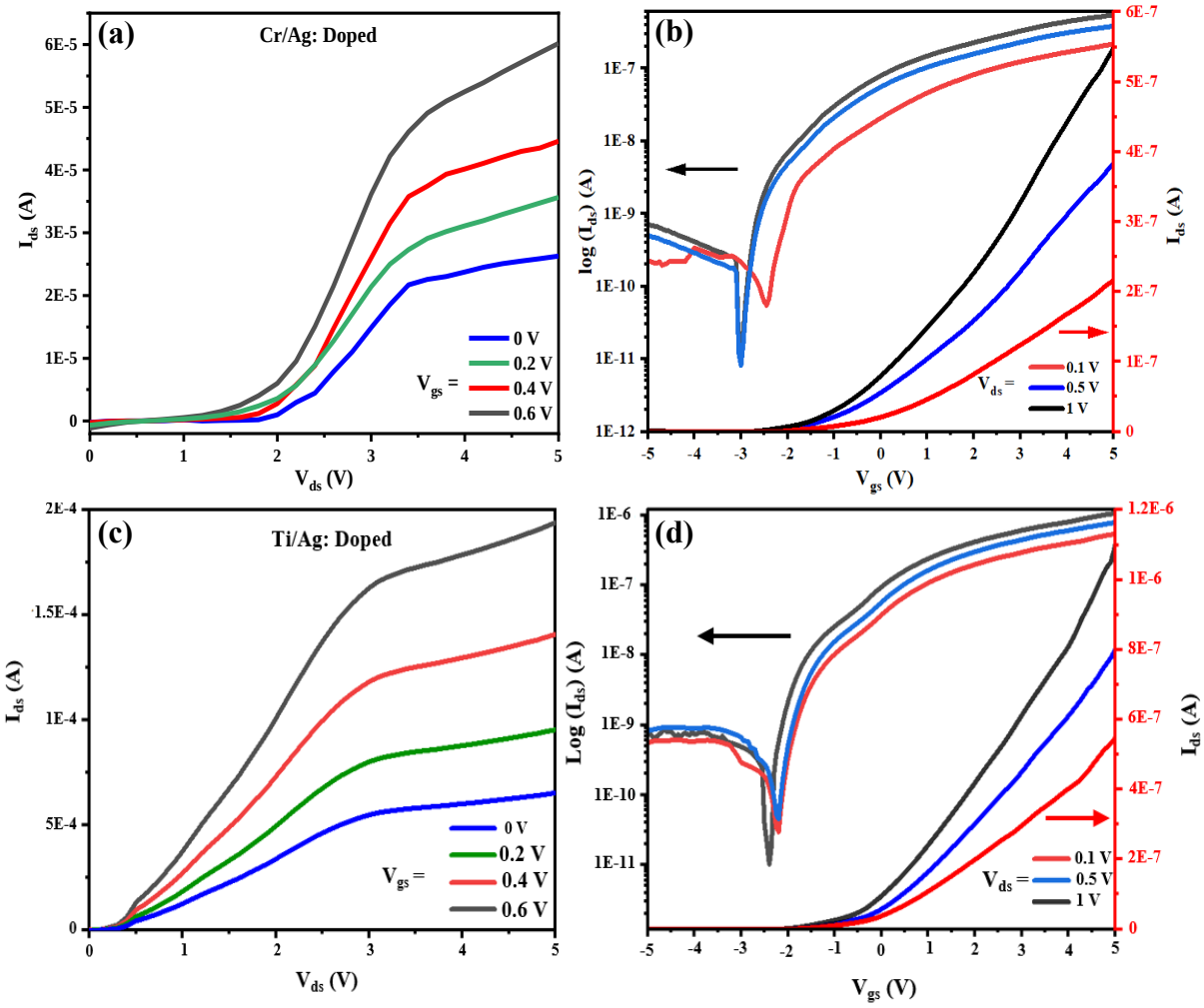

Fig. 5.12: I_{ds}-V_{ds} and I_{ds}-V_{gs} characteristics of the doped WS_2-FET for channel length of 2µm: (a & b) for Cr/Agr and (c & d) Ti/Ag contact

The extracted data reveal that doping significantly enhances the device's performance by increasing the ON current. This improvement is attributed to the increased carrier concentration facilitated through electron injection, as doping introduces additional charge carriers into the channel [52]. The doping process effectively modifies the material's electrical properties, enabling better current conduction when the transistor is in the "on" state. As shown in Fig. 5.13(a), the variations in μ_{FE} and I_{on} are plotted for doped and undoped devices using both Ti and Cr contacts, with a L_{Ch} of 2 µm. The results clearly demonstrate an increase in both μ_{FE} and I_{on} for doped devices, regardless of the contact material. This increase can be explained by the enhanced carrier transport efficiency due to higher carrier concentration. The presence of additional dopants reduces the scattering and trapping of charge carriers, thereby facilitating smoother charge transport and leading to an improvement in the device's electrical performance [33]. The enhancement is consistent across devices with Ti and Cr contacts, indicating that doping plays a dominant role in improving mobility and drive current. In addition, a notable reduction in the SS of the FETs is observed after doping as demonstrated in Fig. 5.13(b)

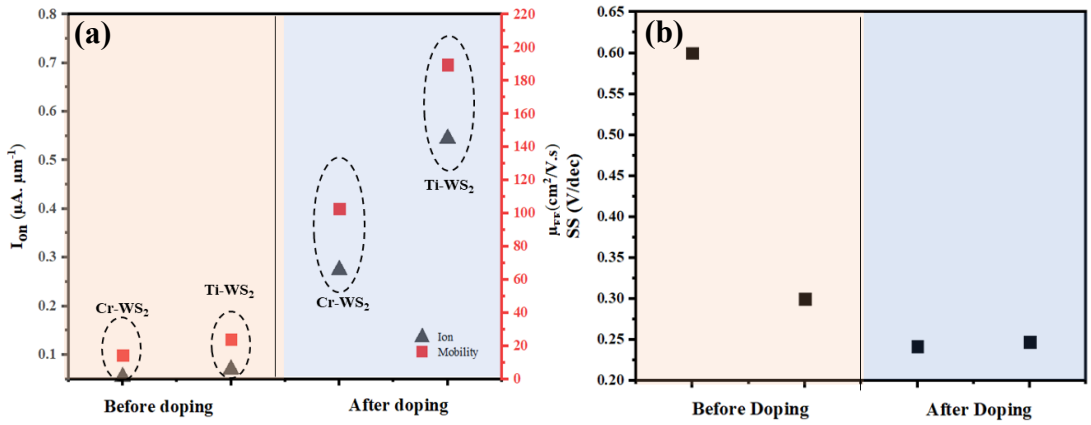

Fig. 5.13: (a) I_{on} and field-effect mobility μ_{FE} for undoped and doped WS_2-based FET and (b) SS for undoped and doped WS_2-based FET

5.3.5. Measurement of Threshold Voltage and Intrinsic Mobility Using Y-Function Method:

The primary obstacle in elucidating intrinsic charge transport properties in low-dimensional materials, such as 2D layered materials, is the considerable R_C typically present at M-S interface [53]. This contact resistance can hinder the material's true electrical properties, making accurate characterization difficult [54]. However, the Y-

function method provides a way to extract contact resistance, threshold voltage, and intrinsic mobility of FETs [55]. Initially, the Y-function proposed by Ghibaudo et.al., method is used for extracting Intrinsic Mobility (μ_0) and V_{th} in silicon-based transistor devices [56]. The Y-function method describes the transconductance or two-point conductance of field-effect devices, which is defined as $I_{ds}/\sqrt{g_m}$, where I_{ds} is the drain current and g_m is the transconductance of the FET extracted from the I_{ds}-V_{gs} characterization at a constant V_{ds} [57]. This approach is particularly useful for studying device physics, as it effectively isolates the intrinsic mobility by excluding the influence of contact resistance. Additionally, the Y-function analysis enables the simultaneous extraction of both the threshold voltage and the effective contact resistance of individual devices.

The Y-function method is a widely used approach for extracting key device parameters in field-effect transistors. It is based on the analysis of the I_{ds} in the linear region of the I_{ds}-V_{gs} characteristics at a constant V_{ds}. The drain current in this region can be described by the following equation [57]_

$$I_{ds} = \frac{W.C_{ox}.\mu_{FE}.(V_{gs}-V_{th}).V_{ds}}{L} = \left[\frac{W.C_{ox}.(V_{gs}-V_{th}).V_{ds}}{L}\right].\left[\frac{\mu_0}{1+\theta.(V_{gs}-V_{th})}\right] \quad (5.3)$$

Here, μ_0 denotes the intrinsic mobility, θ is mobility attenuation coefficient, incorporates the effects of carrier scattering and surface defects to better represent realistic device performance. Fig. 5.14 plots represent the Y-function method as a function of V_{gs} at constant V_{ds} is defined by [58]_

$$Y = \frac{I_{ds}}{\sqrt{g_m}} = \sqrt{I_{ds}}.\sqrt{(V_{gs}-V_{th}).\{1+\theta.(V_{gs}-V_{th})\}} = \sqrt{\frac{W.\mu_0.C_{ox}.V_{ds}}{L}}.(V_{gs}-V_{th}) \quad (5.4)$$

Where g_m is the transconductance defined as dI_{ds}/dV_{gs} is extracted from the slope of I_{ds}-V_{gs} plot in linear scale at constant V_{ds}. The presence of Schottky barriers at the source and drain contacts introduces a V_{gs} dependence in the R_C. This dependence is taken into account when calculating dI_{ds}/dV_{gs}. The μ_0 is extracted from the slope of the Y-function by extrapolating the $\frac{I_{ds}}{\sqrt{g_m}}$ vs. V_{gs} curve at a constant drain-source voltage (V_{ds} =

1 V), independent of the attenuating factors. This method ensures that the extracted μ_0 remains unaffected by attenuating factors such as variations in contact resistance or the presence of Schottky barriers, providing a more accurate characterization of the intrinsic device properties. The extracted threshold voltage $V_{th'lin}$ from the linear extrapolation of the I_{ds}-V_{gs} plot and the $V_{th'Y}$ obtained from the Y-function method are expected to be the same, as both aim to determine the point where the channel starts conducting as shown in Fig. 14(a-d). The devices are denoted by: D1 (Cr-contact WS_2-FET), D2 (Ti-contact WS_2-FET), D3 (Cr-contact Cl-doped WS_2-FET), and D4 (Ti-contact Cl-doped WS_2-FET).

The θ can be described by the following equation [58]

$$\theta = \theta_{Ch} + \frac{W.\mu_0.C_{ox}.R_C}{L} \tag{5.5}$$

Where θ_{Ch} is the mobility attenuation factor from the channel, which includes effects such as a surface roughness and phonon scattering assumed to be negligible [59].

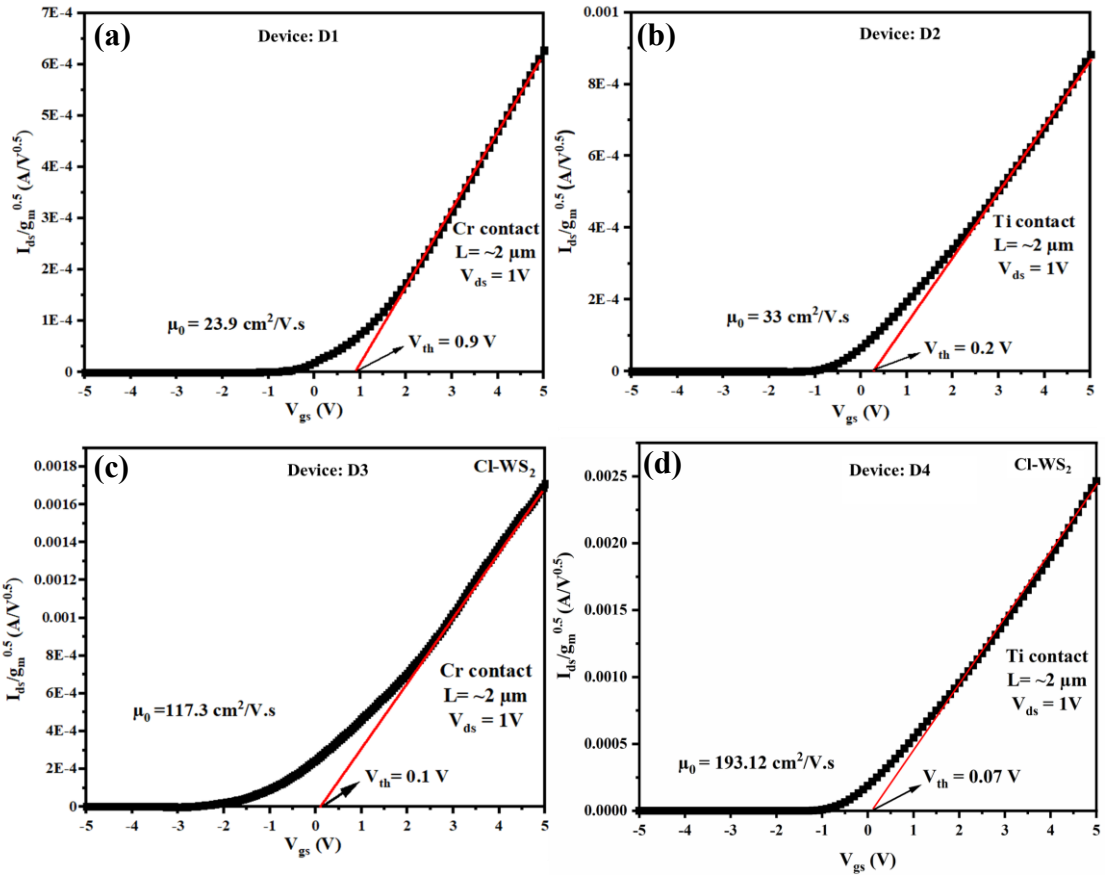

Fig. 5.14: Y-Function ($\frac{I_{ds}}{\sqrt{g_m}}$) plotted as a function of V_{gs} at constant V_{ds} for devices: (a) D1: Cr contact (b) D2: Ti contact and (c) D3- Cr contact with Doped WS_2 and (d) D4: Ti contact with Doped WS_2-FET and V_{th} is extracted from the x-axis intercept of the linear fit of the characteristics curve

Fig. 5.15 presents a comparative analysis of the mobility values obtained using two distinct extraction methods: μ_0, derived from the Y-function method, and μ_{FE}, extracted from the linear regime of the I_{ds}-V_{gs} characteristics at a constant V_{ds}. The results indicate that μ_o is consistently higher than the measured μ_{FE}, underscoring the differences between these two approaches in evaluating carrier transport efficiency within the device. Notably, the μ_o values for the Cr and Ti contact-based contacts have improved to 23.9 cm^2/V.s and 33.04 cm^2/V.s, respectively. These values are significantly higher than the corresponding μ_{FE} values of 14 cm^2/V.s and 25.03 cm^2/V.s, demonstrating that the Y-function method (μ_0) suggests a more efficient carrier transport compared to the linear regime-based method (μ_{FE}). This contrast highlights the influence of the measurement techniques on the assessment of device performance.

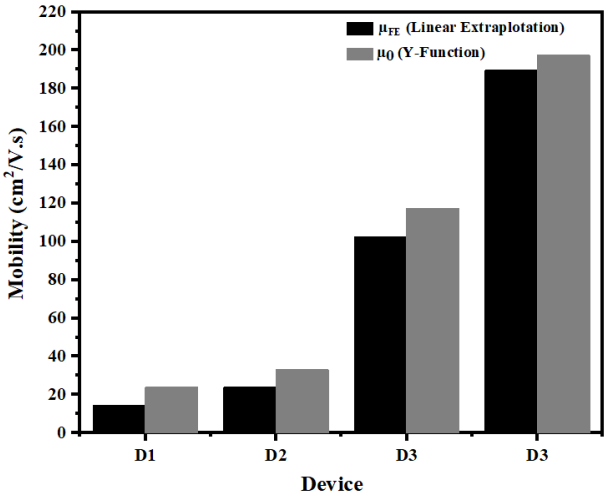

Fig. 15: Comparison of field-effect mobility (extracted from linear extrapolation of I_{ds}-V_{gs} and intrinsic mobility (calculated using the Y-function method) for doped and undoped WS_2-based FETs. Devices: D1 (Cr contact), D2 (Ti contact), D3 (Cr contact with doping), and D4 (Ti contact with doping).

5.3.6. Measurement of Contact Resistance at the Metal-WS_2 Interface:

The conduction mechanism through the Metal-Semiconductor junction of the back-gated 2D WS_2 FET has been studied. In the 2D-FET, the semiconductor thickness is typically smaller than the depletion width, leading to a different conduction mechanism compared to the traditional model. The current flow mechanism in the M-WS_2 junction for back-gated FET where the metal contact is made on the WS_2 thin film is schematically depicted in Fig. 5.16. The arrow represents the current flow through the junction of the M-

S interface where the electrostatically induced electron (e^-), is injected from the metal to WS_2.

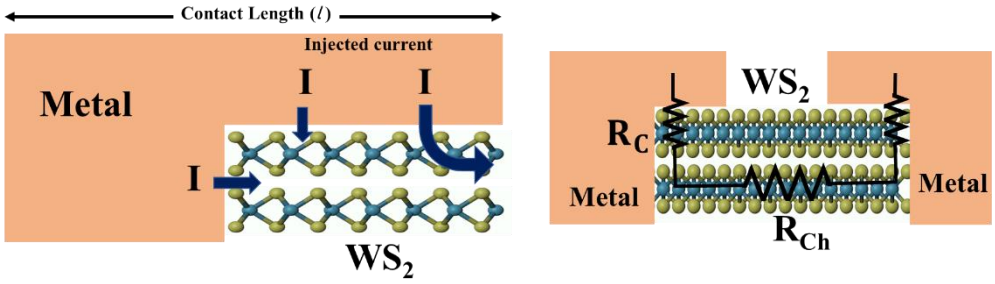

Fig. 5.16: The path of current flow from metal to WS_2 in the FET device is schematical illustrated

TLM, is a widely used technique for evaluating the contact resistance of FETs. However, its application can be challenging, as it requires multiple transistors with varying channel lengths and uniform contact properties to achieve accurate and reliable results. Additionally, local defects on the material's surface can introduce noticeable variations, leading to inconsistencies in the measurements. To address this limitation, the simple Series Resistance Extraction Methodology procedure was determined using the ratio of two I_{ds}-V_{gs} curves measured under two different drain bias conditions [60]. This method is simple and efficient, as it requires only two linear transfer curves from a single device. To examine the impact of the type of material usedas metal contact and doping in semiconductors, on R_C, the total resistance ($R_T = V_{ds}/I_{ds}$) of the device as a function of gate overdrive for the two drain biases (V_{ds} = 0.3 and 0.5 V) is determined in Fig. 5.17(a). The R_T represents the sum of the series resistance (R_{SD}) and Channel Resistance (R_{Ch}), where R_{SD} is equal to $2R_C$ can be extracted using two different channel resistance values at a high overdrive bias [61]. The calculated R_{SD} value is extrapolated as a function of $1/(V_{gs}-V_{th})$, and the R_C is obtained from the R_{SD} vs. $1/(V_{gs}-V_{th})$ curve, the R_C extraction is represented in Fig. 5.17(b) [62]. It was observed that a higher R_T correlates with lower I_{ds} and reduced channel conductivity. Results show that a ~2 µm channel length with Ti contacts yields the highest I_{ds}, effectively reducing R_C. Additionally, higher R_T values may be attributed to factors such as increased R_C at the Metal-WS_2 interface and reduced conductivity, both of which hinder charge transport in the device [63].

$$R_T = R_{SD} + R_{Ch} \quad [5.6]$$

$$R_{SD} = 2R_C$$

The extracted R_C for Ti and Cr are 63.04 kΩ.µm and 91.79 kΩ.µm respectively for ~2 µm channel length which is comparatively lower than Cr contact-based FET device. After doping the WS_2 surface for a Cr contact-based FET device, the R_C decreased significantly from 91.79 kΩ·µm to 44.82 kΩ·µm. This notable reduction in R_C indicates that the increased carrier concentration can enhance the operating performance of the FET and lower the barrier height at the M-S contact facilitating the narrow tunnel barrier [64]. The results demonstrated that the R_C, R_T and R_{Ch} is strongly depend on the carrier concentration (n_s) of the channel [38].

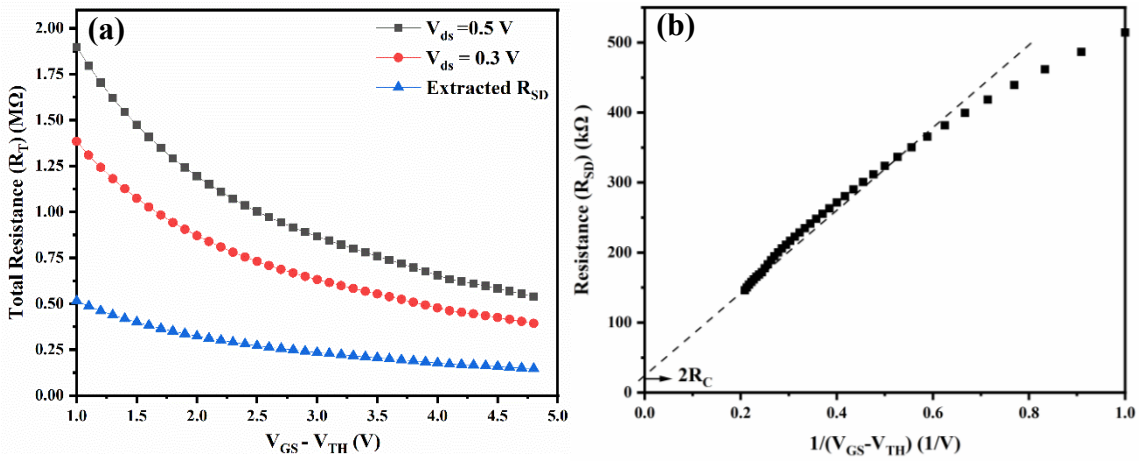

Fig. 5.17: (a) R_T at different V_{ds} for extraction of series resistance R_{SD} and (b) the distribution of the R_{SD} value plotted against 1/(V_{gs}-V_{th}) for the extraction of 2R_C

In addition, the carrier concentration (n_s) of the FETs was calculated for both doped and undoped WS_2-based FETs. The n_s was calculated using the following equation [65]_

$$n_s = \frac{(V_{gs}-V_{th}).C_{ox}}{q} \qquad [5.7]$$

The carrier concentration of the FET channel can be modulated by the applied gate voltage. The concentration of the charge carrier depends on various other factors such as channel conductivity and interface engineering of source-drain metal contacts which can strongly affect the operating performance of FET. It reduces the barrier width at the junction by applying a back-gate voltage, facilitating carrier tunnelling through the barrier and consequently decreasing the contact resistance R_C. In this case doping is studied to vary carrier concentration. The extracted value of R_C for all the FETs is plotted as a function of carrier concentration n_s is depicted in Fig. 5.18(a). The n_s of both the Cr- and Ti-contact-based FETs show 1.18 x 10^{10} cm^{-2} and 1.20 x 10^{10} cm^{-2}, which improve to

1.23 x 10^{10} cm^{-2} and 1.25 x 10^{10} cm^{-2} respectively. The increase in carrier concentration facilitates the decrease in contact resistance after doping. The obtained results demonstrate that the charge carrier concentration is inversely proportional to the contact resistance. As the carrier concentration increases, a corresponding decrease in contact resistance is observed after doping. A lower R_C at the M-S interface facilitates easier electron flow through the junction.

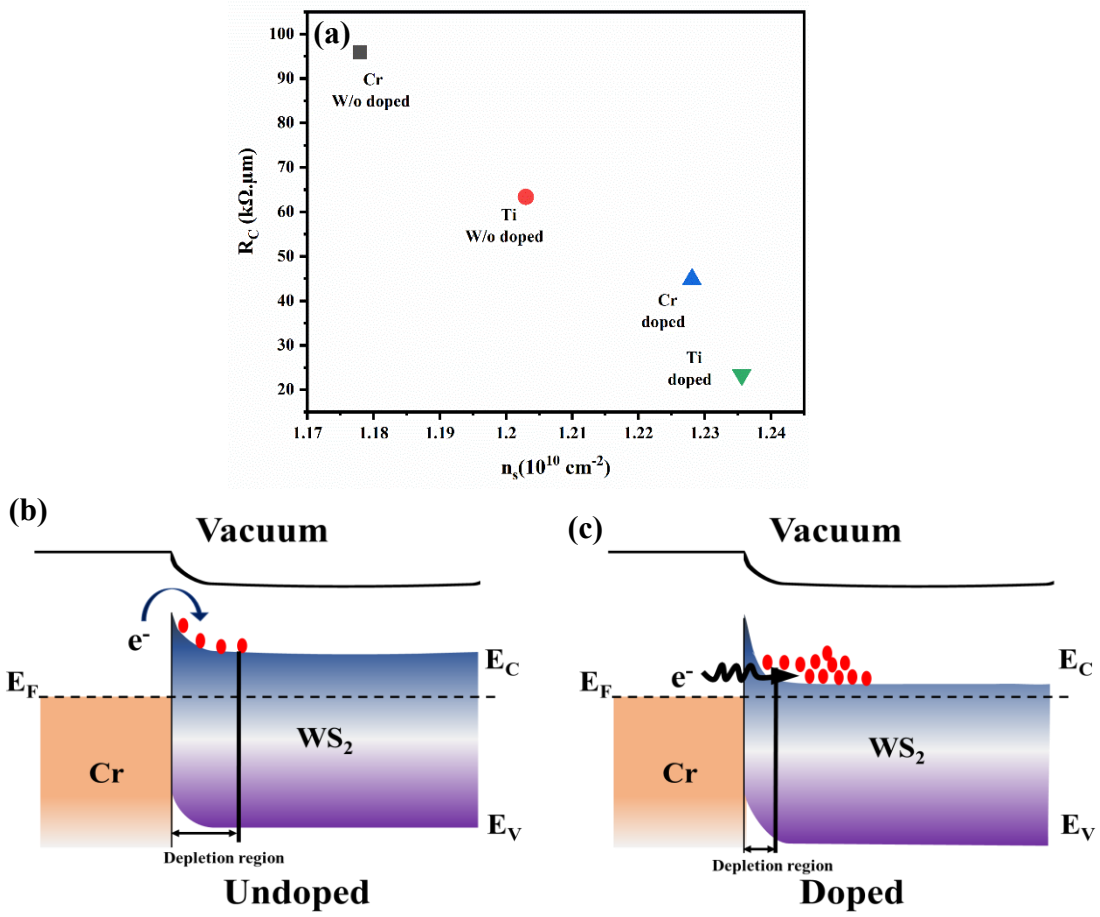

Fig. 5.18: (a) Variation of R_C with n_s for both doped and undoped WS_2-FETs and (b & c) energy band diagram of Metal-WS_2 interface for undoped and doped WS_2-based FET

Additionally, the data reveals that n-type doping significantly facilitates the flow of electrons through the junction of the FET [66]. By introducing charge carriers into the semiconductor, the doping process enhances the carrier concentration, making it easier for electrons to flow across the junction [51]. This increased carrier concentration also plays a crucial role in modulating the conduction band, causing it to move closer to the Fermi level as shown in Fig. 5.18(c). As a result, the material's electronic properties are altered, leading to improved conductivity. The enhanced electron flow is primarily

enabled by two mechanisms: tunnelling and Fermi-level pinning. Tunneling allows electrons to pass through potential barriers at the metal-semiconductor interface, even without overcoming the barrier's full energy requirement. This phenomenon effectively narrows the width of the depletion layer at the M-S interface. A narrower depletion layer allows for easier electron movement, improving the efficiency of carrier transport across the junction. These findings demonstrate that the reduction in depletion layer width through doping not only enhances the electron flow but also optimizes the performance of the FET by facilitating more efficient electron conduction [43,44]. The fabricated WS_2-FET exhibits promising electrical characteristics, including enhanced mobility, reduced R_C and other electrical parameters, through doping on WS_2 nanosheets and improved carrier transport facilitated by appropriate metal contacts. A key concern is the susceptibility of WS_2-FET to environmental factors such as humidity and temperature, which can lead to degradation of its electrical performance over time. The future work prioritizing this dimension to address the issue of environmental robustness, long-term stability, and scalability of WS_2-FET will pave the way for the commercial viability of the technology.

5.4. Summary:

The fabricated few layer-WS_2 back-gated FET device demonstrated stable electrical performance following a two-step lithography process, confirming that the fabrication steps did not significantly impact the crystalline structure of WS_2. However, the Cr metal contact with the WS_2 nanosheet displayed non-linear characteristics due to high contact resistance, arising from the mismatch between the metal's work function and the semiconductor's electron affinity. A comprehensive analysis of the electrical characteristics of the fabricated FL-WS_2 FETs was conducted. The study showed that factors like metal contacts (Cr and Ti), variations in channel length, and doping considerably influenced key electrical parameters of FL-WS_2 FETs, such as μ_{FE}, V_{th}, subthreshold swing, ON current, contact resistance, and overall device conductivity. Our findings indicate that the Cr-WS_2 FET exhibited a mobility of approximately 14.3 $cm^2/V{\cdot}s$, which improved to around 25.03 $cm^2/V{\cdot}s$ with Ti contacts for a channel length of about 2 µm. After doping, the mobility further increased significantly, reaching approximately 102.7 $cm^2/V{\cdot}s$ for Cr-contact-based WS_2 FETs and ~189.5 $cm^2/V{\cdot}s$ for Ti-contact-based WS_2 FETs, demonstrating the effectiveness of doping in enhancing carrier

transport properties. Additionally, the SS values for all FETs were higher than those for Ti-WS_2-FETs and doped WS_2 FETs, with a minimum value of 0.2 V/dec. However, all FETs show the I_{ON}/I_{OFF} ratio is ~10^4 with n-type FET characteristics. In addition, the Y-function method has proven to be an accurate and robust approach for extracting the intrinsic mobility of FETs, even when accounting for the gate-dependent variations commonly observed in semiconducting TMD transistor devices. The Y-function analysis mentioned in section 5.3.6 indicates that the μ_0 of the FET is higher compared to μ_{FE}. However, the threshold voltage of the FETs remains unchanged in the Y-function analysis. It was observed that the shorter channel lengths led to higher drain currents, facilitated by contact engineering with the low-work-function metal like Ti. The contact resistance of the Cr-contact-based WS_2 FET decreased from 91.7 kΩ·μm to 44.82 kΩ·μm with n-type doping, while the Ti-contact-based FET exhibited a reduction from 63.34 kΩ·μm to 23.39 kΩ·μm after doping. The highest carrier concentration (n_s) was 1.25 x 10^{10} cm^{-2}, and the V_{th} was approximately 0.07 V for the fabricated FET with Ti contact. These results indicate that 2D WS_2 is a promising material for FET applications.

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