Study of Multi-Channel Spread Spectrum Systems for Wireless Communication

A thesis submitted in partial fulfillment of the requirements for the Degree of Doctor of Philosophy

By

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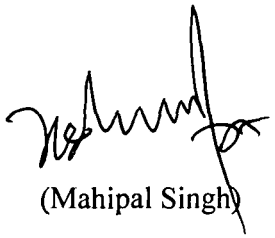
Dedicated to

The Almighty and My Family Members

AUTHOR'S DECLARATION

I hereby declare that the thesis entitled "**Study of Multi-Channel Spread Spectrum Systems for Wireless Communication**" is an outcome of my research carried out at the Department of Electronics & Communication Engineering, School of Engineering, Tezpur University, Assam, India. The work is original and has not been submitted in part or full, for any degree or diploma of any other University or Institute.



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Certificate

This is to certify that the thesis entitled "**Study of Multi-Channel Spread Spectrum Systems for Wireless Communication"** submitted to the Tezpur University in the Department of Electronics and Communication Engineering under the School of Engineering in partial fulfillment for the award of the degree of Doctor of Philosophy in Electronics and Communication Engineering is a record of research work carried out by Mr. Mahipal Singh under my supervision and guidance.

All help received by him/her from various sources have been duly acknowledged.

No part of this thesis has been submitted elsewhere for award of any other degree.

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This is to certify that the thesis entitled "**Study of Multi-Channel Spread Spectrum Systems for Wireless Communication**" submitted by Mr. Mahipal Singh to the Tezpur University in the Department of Electronics and Communication Engineering under the School of Engineering in partial fulfillment for the award of the degree of Doctor of Philosophy in Electronics and Communication Engineering has been examined by us and found to be satisfactory.

The committee recommends for the award of the degree of Doctor of Philosophy.

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Abstract

The advancement in the technology has flourished the communication sector in all directions and the concept of communication has changed from traditional wired telephone to wireless telephone. However, the resource that makes wireless communications possible is the spectrum which is scarce and limited. The growth in the number of wireless users and services has caused pressure on efficient use of available bandwidth (spectrum). To elucidate some of challenges of wireless communication the spread spectrum technique has emerged as a well-known technique. The spread spectrum based Code division multiple access (CDMA) techniques have been widely accepted for designing the next generation wireless systems with many advantages. This thesis, investigates multiplexing/multi-channeling of wireless systems using spread spectrum communication for efficient use of available spectrum by accommodating more number of users on a single channel. The proposed signal processing techniques are also studied to enhance the performance of existing systems.

Firstly, we investigate the CPSK technique for multiplexing/multi-Channing using DSSS and FHSS system. The designed and simulated systems accommodate more of number users on the same channel. The performance for BER was analyzed with a simulation model using software.

Secondly, we have proposed a binary phase shift keying (BPSK) demodulator for processing the signal in the receiver. This demodulator has been investigated for BER performance analytically and with simulation model.

Thirdly, the M-ary based CFHSS system has been designed and simulated for accommodating more users using band pass filters (BPF). The performance of the system is tested under different hop size. It shows that higher the hop size, lesser the BER and vice versa.

Lastly, we concentrate on the design of FHSS system for multi-channeling using proposed sinusoidal frequency to voltage converter (FVC) by replacing the BPF. The FVC also tested and analyzed for linearity and ripples. The FVC provides a higher frequency range of conversion with linear output.

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List of Abbreviations

ACA	adaptive channel allocation
AGC	automatic gain control
ASK	amplitude shift keying
AWGN	additive white Gaussian noise
BPF	band pass filter
BER	bit error rate
BPSK	binary phase shift keying
CSK	code shift keying
CMOS	complementary metal oxide semiconductor
CDMA	code division multiple access
CPSK	code phase shift keying
CMFHSS	code m-ary frequency hop spread spectrum
CDM	code division multiplexing
DAC	digital to analog converter
DSSS	direct sequence spread spectrum
D-BPSK	differential binary phase shift keying
FDM	frequency division multiplexing
FHSS	frequency hop spread spectrum
FVC	frequency to voltage converter
FCC	federal communications commission
FPGA	field programming gate array
FH	frequency hopping
FDMA	frequency division multiple access
GSM	global system for mobile
HPF	high pass filter
HCS	hierarchical cell structures
JSR	jamming to signal ratio
LEO	low earth orbit
LFSR	linear feedback shift register

List of Publications

Journal Papers

1. P.P. Sahu and **M. Singh,** "Multi channel frequency hopping spread spectrum signaling using code M-ary frequency shift keying." Computer and Electrical Engineering, (Elsevier), vol. 34, (2008), pp. 338-345.

2. **Singh Mahipal,** Sahu P. P. "Four channel transmitter and receiver using CPSK based direct sequence spread spectrum." International Journal HIT Transition on ECCN 2006: 1(1): 63-71.

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5. P. P. Sahu, **M. Singh,** and A. Baishya, " New low-voltage full wave rectification technique without a diode" IET Circuits Devices Syst., vol. 5, issue 1, pp. 33-36, 2011.

6. **M. Singh** and P.P. Sahu "A Wideband Linear Sinusoidal Frequency to Voltage Converter with Fast Response Time" Procedia Engineering (Elsevier) vol. 64, pp.26-35 2013.

LNA	low noise amplifier
LNA	low noise amplifier
MMSE	minimum mean square error
MIMO	multiple-input multiple-output
MLD	maximum likelihood decoding
MFSK	m-ary frequency shift keying
MSK	minimum shift keying
MSK	minimum shift keying
MAI	multiple access interference
PN	pseudo-noise
PG	processing gain
OTA	transconductance amplifier
QPSK	quadrature phase shift keying
SER	symbol error rate
SDMA	space division multiple access
SIPO	serial in parallel out
SSMA	spread spectrum multiple access
TDM	time division multiplexing
TDMA	time division multiple access
US DD	united states Digital Cellular
VLSI	very large scale integration
VCO	voltage control oscillator

Chapter 1

Introduction

1.1 Overview

Over last two and half decades, the success of cellular system has revolutionized the wireless industry [1]. But the tremendous growth of wireless users [2] has put forth many challenges for wireless communications [3]-[4]. These challenges include accommodation of more users, needing for more spectrum, immunity to interferences from simultaneous users [5]-[8] etc. Engineers and researchers are putting many efforts to bridge these demand and supply gaps. Available spectrum is limited [9] which have posed growing pressure on wireless industry for efficient utilization [10] of available spectrum. Adding spectrum is not one of the enduring solutions to the above challenges. Therefore either new technology is to be evolved or existing technology to be modified for spectral efficiency. In this direction spread spectrum technique has emerged as one of the most popular tools to mitigate many issues [11] of wireless communications.

Since 1950, the spread spectrum systems have been developed, and initially, its applications were restricted for military to hide the data from enemy as an anti-jamming tactical communications [12]. In this technique the signal occupies the bandwidth [13]-[14], which is greater than the minimum necessary, for sending the information. Two methods, namely, (i) direct sequence spread spectrum (DSSS) [15] -[22] and (ii) frequency hopping spread spectrum (FHSS) [23] -[31] are used for spread spectrum communication. In the DSSS, fast pseudorandom sequence causes phase transitions in the carrier using different modulation techniques. In the FHSS system, pseudorandom sequences cause the carrier to hop from one frequency to another frequency.

To enhance system capacity/spectral efficiency, by accommodating a number of users on a single channel, different multiplexing techniques [32], namely, (i) time division multiplexing (TDM), (ii) frequency division multiplexing (FDM), (iii) code division multiplexing (CDM) and space division multiplexing (SDM) are used. In TDM, [33] successive intervals of time are assigned to the different uses. During these intervals the bits of information from all channels are transmitted in rotation. At the receiving terminal the pulses are sorted out according to their time of arrival, and

diverted to their respective channel. In FDM [34], the total available bandwidth is divided into a series of non-overlapping sub bands, and each of them is dedicated to each user. As compared to TDM, FDM occupies more bandwidth; therefore it is not a bandwidth efficient system. CDM [35] is most bandwidth efficient technique and used for commercial applications by allowing several users to communicate simultaneously on common channel using pre-assigned code sequences. SDM [36]-[38] is more recently evolved technique for higher speed requirement of 4^{th} and 5^{th} generation. It utilizes the spatial separation of users. In these techniques all users are allowed to simultaneously share the common medium.

Further, the advancement in VLSI technology and signal processing [39]-[40] has played a dominating role to settle down some of the challenges of wireless communication by improving the quality of service, reduced power consumption, enhanced system capability and capacity [41]-[43]. Many signal processing techniques, such as filtering [44]-[45], equalization [46] -[49], detection [50] -[51], pulse shaping [52], demodulation [53] -[55], frequency to voltage converts (FVC) [56] -[58] etc., are evolved to enhance the performances of the communication devices.

This work discusses the design of multi-channeling (multiplexing) scheme using spread spectrum techniques for increasing channel capacity and performance evaluation of designed system. The proposed BPSK demodulation for demodulating has been studied for its performance. The sinusoidal FVC techniques have been studied for improving the performance of wireless FHSS communication systems and for wide band operation with very good linearity.

1.2 Multi-channel Communications

Since the origin of electronic communication there has been a requirement for providing simultaneous transmission of many messages using single transmission media [33] - [34]. Initially time division and frequency division multiplexing schemes were evolved

to increase the channel capacity [33]-[34]. The growth of users aggravated the capacity problem [59] and has caused an accelerating pressure on efficient use of bandwidth. The solution to the problem of efficient bandwidth utilization has emerged during 1950 and 1960, when researchers at Bell laboratories developed the cellular concept [60]. This concept exploits the fact that the power of transmitter signal fall off with distance therefore frequency reuse is possible at spatially separated location and hence more capacity. The founders of quality communication (QUALCOMM) developed CDMA technology for commercial cellular communications [1]-[61] to make even better use of the radio spectrum than other techniques for multiple accesses.

Code division multiple access (CDMA), is a spread spectrum technique in which each user is allocated signature code so that it can occupy same frequency spectrum simultaneously with the other users [15] -[16]. Therefore, CDMA systems can operate at much higher interference levels because of its interference resistance capability [61]. Along with this it provides multiple access capability with much higher capacity over other existing techniques like time division and frequency division multiplexing, high resistance to jamming, intentional interference therefore it is the most promising multiplexing technologies for current and future telecommunications services which has attracted it for future technology [35]-[36].

1.3 Open Issues in Multi-channel Wireless Communication

The resources those make wireless communications possible are limited. The one of the most important resource is bandwidth (spectrum). At the same time, the growth in the number of wireless users [2] has caused pressure on efficient use of available bandwidth [3]-[4]. The initially developed wireless systems for telephony have used 120 KHz of bandwidth and immediately the bandwidth was cut down to 60 KHz to accommodate more number of users by improving the technology [1]. It has doubled the channel capacity but there was a long waiting list of more users demanding to have wireless access capability. Seeing the growing number of users, in 1989 an additional

spectrum of 10MHz was released to address these waiting users. With the advancement in very large scale integration (VLSI) and digital technology, in late 1991, the first US Digital Cellular (USDD) has supported 3 users in 30 KHz bandwidth and improved the channel capacity by three times. But this improvement in channel capacity was insufficient to cater all users. A better solution for capacity enhancement was proposed by QUALCOMM using spread spectrum based CDMA [61]. The rise in the number of wireless users will continue in future also due to population growth and technological advancement for more services. These factors are enhancing the pressure on existing technology. Further, the mounting pressure is not alone due to the exponential growth in the number of users; it is further accelerated by demand for high data rate, better quality of service, degradation due to interference, noises etc.

Therefore, these issues were developed since the origin of communication system because of a gap in demand and supply. The technological advancement is continuously trying to fill the gap by advanced signal processing techniques and will continue in future also. The main issues of multichannel wireless communications are bandwidth efficiency, better channel capacity and improvement in signal to noise ratio.

1.4 Objectives

The main objectives of this dissertation are as follows:

- To design and simulate the proposed Code phase shift keying (CPSK) based DSSS transceiver for a multi - channel using Sallen-Key filter.
- To design and simulate the proposed CPSK based DSSS receiver for a multi-channel using a proposed demodulator for improvement of BER performance under noise and jamming in comparison to the CPSK based DSSS transceiver using Sallen-Key filter

- To design and simulate code M-ary frequency shift keying (CMFSK) based FHSS transceiver for multi-channel using BPF.
- To design and simulate the CMFSK based FHSS receiver for multi-channel using proposed sinusoidal FVC for improvement of BER performance under noise and jamming

1.5 Contributions

The conclusions of this research work along with key contributions are summarized as below:

1. Design and implementation of CPSK based DSSS transceiver for accommodating 4 users has been made. It has been found that without an increasing frequency band, numbers of users are increased by the same DSSS system and at the same time BER is less.
2. The proposed BPSK demodulator has been studied for DSSS system in order to reduce the BER further for DSSS.
3. Design and implementation of M-ary FSK based FHSS transceiver for accommodating 4 users has been studied and design along with performance evaluation.

4. R-C based FVC has been proposed for simplification of the FHSS circuit as the design of narrow band pass filter is critical requiring more order of the filter. It was also found that the proposed FVC provides linear frequency to voltage conversion over a wide range of frequency.

As a future prospect, one can try to implement the transceiver with the increase number of users (more than four) using CPSK based DSSS and M-ary FSK based FHSS systems. It is also seen that although a DSSS system requires less number frequency than that of FHSS system, the BER performance for later system is better than that for former system. So it is required to propose and develop a FHSS system with less

number of frequencies without degradation of BER performance. Another issue to be looked at the future is signal safety or security.

1.6 Thesis organization:

The structure of this thesis is as follows:

Chapter-2: *Overview of Spread Spectrum Signaling for Wireless Communications* – .This chapter reviews the PN sequences with properties and types. The basic theory of single user DSSS, CPSK based DSSS, FHSS, M-ary FHSS, Slow and fast FHSS are presented here. Previous work in multiplexing, M-ary keying and multiple accesses techniques along with AWGN and intentional noise (Jamming), are discussed briefly.

Chapter-3: *Review of Multiplexing and Multiple Access* Techniques *and their Evaluation for Wireless Communications* – In this chapter a literature review is presented that describes existing multiuser/multiplexing system for accommodating more number of users. Brief history of multiplexing techniques such as, TDMA, FDMA CDMA AND SDMA is discussed. We have also surveyed sinusoidal frequency to voltage converter (FVC) for wider band of frequencies and existing binary phase demodulator.

Chapter-4: *Design and Simulation of CPSK based Multi-Channel Direct Sequence Spread Spectrum System* – This chapter presents architecture and working principle of CPSK based transceiver for accommodating K-users. Further this chapter concentrates on the design and performance test of the proposed system for accommodation of four users to show the concept of using CPSK technique for bandwidth efficiency. The proposed technique for BPSK demodulation, using BPSK to ASK converter and peak to peak detector has been explained here.

Chapter-5: *Performance Evaluation of CPSK based DSSS System* – In this chapter the performance analysis of CPSK based DSSS transceiver is presented. Performance is

discussed under AWGN, jamming and due to phase mismatch. Performance analysis of designed system is carried out with the simulation setup using Microsim software.

Chapter-6: *Design and Simulation of Multi-Channel Frequency Hopping Spread Spectrum Spread Spectrum Communication System using coded M-ary Frequency Shift Keying* – It describes the architecture of transceivers for K-users using the CMFSK based FHSS technique. Further, this chapter describes the design and simulation of the system for accommodating 4-users. P-Spice simulated circuit using band pass filters (BPF) for transceiver has been presented the Chapter. Proposed wide band FVC has been discussed along with its performance for response time, linearity, and ripple calculation

Chapter-7: *Performance Evaluation of CMFSK based FHSS System* – This Chapter high lights analytical evaluation of symbol error rate (SER) and bit error rate (BER) s performance of the designed FHSS system under AWGN. Jamming and BER performance has been investigated with simulations. Chapter also presents the performance of designed device with proposed frequency to voltage converter (FVC) using P-Spice simulation model. Section Eye diagram analysis for noise margin and distortion also discussed. Finally, the experimental traces obtained from experimental measurement are presented.

Chapter-8: *Conclusion and future scope* – This chapter summarized the thesis conclusion with the future scope of this PhD research work.

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Chapter 2

Overview of Spread Spectrum Signaling for Wireless Communications

2.1 Introduction

The spread spectrum concept was first introduced by the US Army in 1950 in defense. Thereafter, the extensive work has been carried out on spread spectrum technology leading to different types of applications such as commercial wireless communications [1] -[3], mobile communications [4], underwater communications [5] -[6] etc. There are mainly two types of spread spectrum technology, direct sequence spread spectrum (DSSS) and frequency hopping spread spectrum (FHSS). The demand for wireless communication is rapidly growing and spread spectrum technology promises to be a key technique for future technology. Keeping the above in view, we have tried to provide fundamental concept of various spread spectrum systems. Additive White Gaussian Noise (AWGN) and jamming by various signals are the main concern for performance degradation of wireless systems. Therefore, different noises encountered in the system are also discussed in the chapter.

This chapter is organized as follows. Section 2.2 discusses PN sequences, their types and properties. Section 2.4 describes the basic principle of spread spectrum and discusses the spreading idea using PN sequences. The spread spectrum is basically of two types as DSSS and FHSS. In Section 2.5 and 2.6 we have tried to discuss concept used in DSSS and FHSS with block diagrams. Section 2.6 concentrates on noises encountered in communication systems with their types such as additive white Gaussian noise (AWGN) and jamming noise in spread spectrum communication. Performance evaluation of wireless system is very essential; therefore, Section 2.7 concentrates on the bit error rate (BER) of a digital system under AWGN. Finally, the conclusion is given in Section 2.8.

2.2 Pseudo-noise Sequences

Pseudo-noise (PN) sequences are the building blocks of any spread spectrum system communication system. It is a periodic binary sequence with a noise-like waveform which is usually generated by means of feedback shift register used for spreading the

signals [8]-[12]. These sequences provide protection against interference and enables the bandwidth tradeoff of processing gain for interfering signals. They also provide privacy by providing protection of signals from eavesdropping to the degree the code themselves is secured [9]. Following sub-sections briefly discuss the different types of PN sequences and their properties.

2.2.1 Maximum Length Sequences

The maximum length sequences (m-sequences) are generated using linear feedback shift register (LFSR) and exclusive OR-Gate. These sequences also called maximum sequences or maximum codes that can be generated by a shift register. An LFSR is said to be linear when the feedback logic consists entirely of modulo-2 adders. Certain outputs of the shift register are modulo-2 added and the adder output is fed back to the register. A PN sequence produced by such a linear feedback shift register with m flip-flops cannot exceed $2^m - 1$ [11]. When the period is exactly $2^m - 1$, the PN sequence is called a maximal-length-sequence. Figure 2.1 shows the block diagram of maximal length sequence generator for generating the m-sequences [11].

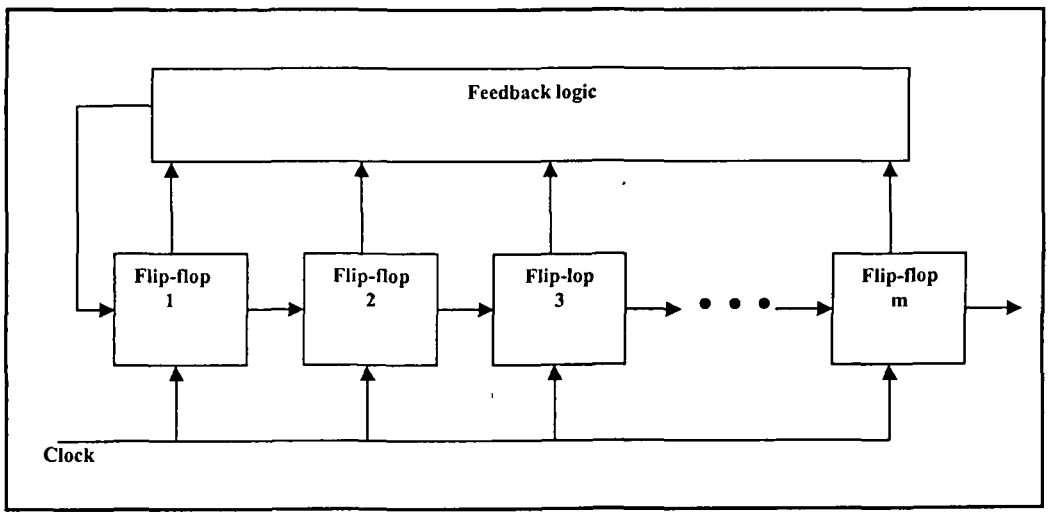

Fig.2.1: Block diagram of feedback shift register [11]

2.2.2 Gold Codes Sequences

Gold codes are named after Robert Gold and are constructed by summing "preferred pairs" of M-sequences, or maximal using these m-sequences [10]. Gold sequences have only three cross-correlation peaks, which tend to get less important as the length of the code increases. Gold sequence [10] is particularly popular for non-orthogonal CDMA systems. Gold codes have bounded small cross-correlations within a set, which is useful when multiple devices are broadcasting in the same frequency range. In a set of m-sequences some will have good cross-correlation properties. These sequences are called preferred m-sequences. A set of new PN sequences can then be generated from two preferred m-sequences by modulo-2 summing them in a specific manner. These new sequences will exhibit the same good cross-correlation properties as the original two preferred m-sequences used to generate them. These new sets of PN sequences are called Gold codes. Figure 2.2 shows the bock diagram Gold sequence generator [11].

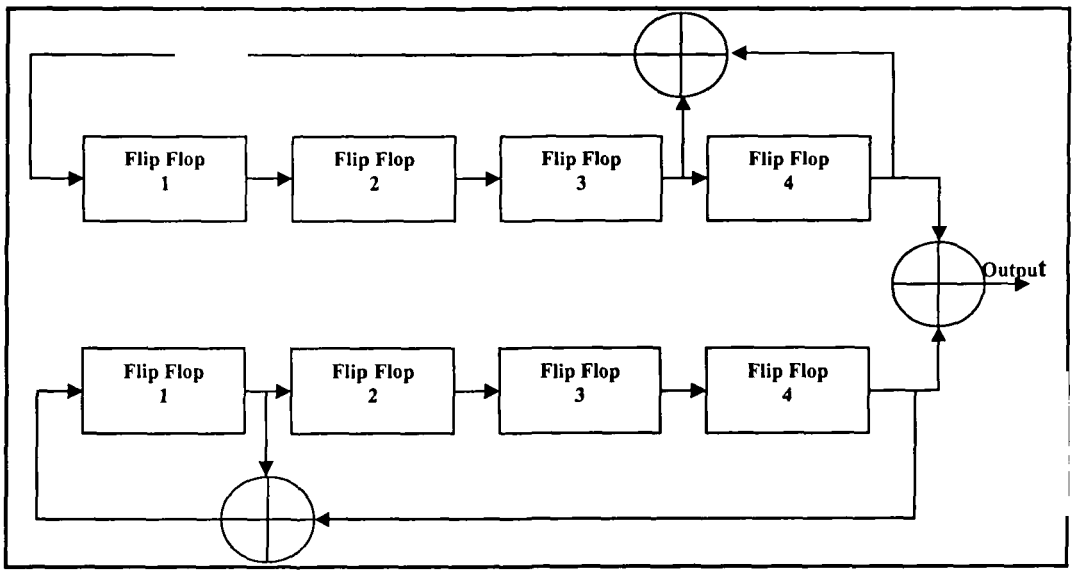

Fig.2.2: Generation of Gold code by combining two m-codes [11]

2.2.3 Barker Sequences

Barker sequences are short length codes and they were originally developed for radar applications [11]-[12]. Besides offering good correlation properties they have many advantages over other PN sequences. Different Barker codes come in lengths of two, three, four, five, seven, eleven and thirteen digits. These codes, which are subsets of PN sequences, are commonly used for frame synchronization in digital communication systems. The different known Barker codes are given in Table 2.1[12].

Table- 2.1 Different Barker Codes [12]

Length	Code
2	10, 01
3	110
4	1101, 1110
5	11101
7	1110010
11	11100010010
13	1111100110101

The conventional direct-sequence spread spectrum multiple-access system has its limitation and as the number of active user's increases. The bit error rate (BER) performance is degraded and even the gold like sequences also does not perform well. The BER performance of the of conventional DSSS systems employing Gold code-like sequences degrades with the increase of simultaneous users in the system. Thus the key to reduce multiple access interference is to acquire a set of PN spreads sequences which have the property of low odd and even periodic correlation magnitudes among all sequences [13]. Barker code produces a single peak and uniformly low side lobes when correlated against time shifted versions of it and thereby it rejects multi-path. This simply means that due to the non-repetitive behavior of the code, a matched filter correlator can easily identify the location of a Barker code in a sequence of bit. If one or

more chips in the bit are lost during transmission, statistical techniques embedded in the receiver can recover the original data without retransmission. The value of the autocorrelation function for the 11-bit Barker code is 1, -1, or 0 at all offsets except zero, where it is 11. The autocorrelation function of 11-bit Barker code is shown in Figure 2.3 [13].

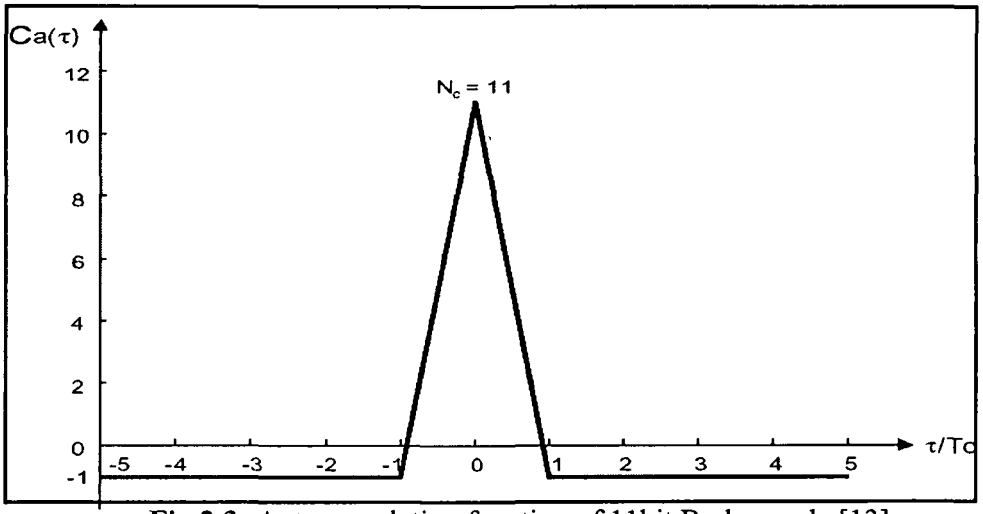

Fig.2.3: Auto correlation function of 11bit Barker code [13]

2.2.4 Properties of PN Sequences

An ideal PN sequence requires that its auto correlation function must be zero. But in actual practice due to several constraints the PN sequence will have an auto correlation function that is very small over the entire period. The following are the properties of PN sequence.

- **Balance Property**

In one period of a m-sequence, the number of 1's and that of 0' is nearly the same [11] -[12]. Since the period is an odd integer, they cannot be exactly the same, but differ only by one. This is called as a balance property.

- **Run Property**

A run is defined as a sequence of a single type of binary digit (s). The appearance of the alternate digit in a sequence starts a new run [11]. Between the runs of ones and zeros in each period, it is desirable that about one-half the runs of each type are of length 1, about one fourth are of length 2, one eighth are of length 3, and so on.

- **Correlation property**

If a period of one sequence is compared term by term with any cyclic shift of itself, it is best if the number of agreements differs from the number of disagreements by not more than one count [12].

2.3 Spread Spectrum Technique

Spread spectrum systems have been developed during the mid-1950 [1]-[4]. In the initial phase, its application was restricted for military to hide the data from enemy as an anti-jamming tactical communications. Since the last decade of the 20th century the spread spectrum systems have been increasingly used for commercial and industrial applications. Spread spectrum was first used for commercial purposes for multiple-access communications over synchronous satellite transponders in the 1980 [14]-[15]. In the late 1980s, the US Federal Communications Commission (FCC) opened up the industrial, scientific and medicine frequency bands for unlicensed spread-spectrum communications [14].

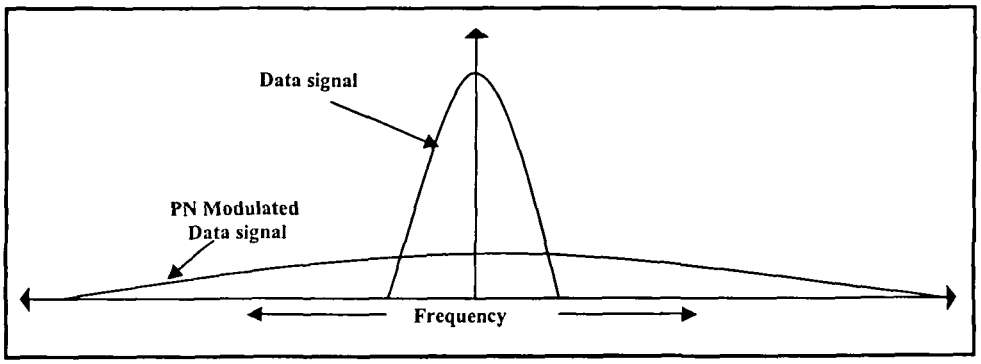

Fig.2.4: Data signal and modulated PN sequence in frequency domain [14]

Spread-spectrum techniques used to hide a signal by transmitting it at low power. By spreading the signal energy over the widest available bandwidth and using the minimum power needed, the signal can be hidden in the channel noise as shown in Figure 2.4. This means that any unauthorized interceptor will have a low probability of detecting the signal relative to the intended receiver. There are two methods for spread spectrum techniques, direct sequence spread spectrum and frequency hopping spread spectrum. These two methods are discussed in more details in the following sections.

2.4 Direct Sequence Spread Spectrum

In direct sequence spread spectrum system (DSSS), a code is used to spread the spectrum of a data-signal [14]-[22]. It is widely used for transmission of digital signals in wireless and military applications because they are very effective in suppressing interference. This interference can occur from several sources. One source could be an adversary deliberately jamming the communication channel.

The higher is the length of PN sequence, higher will be the bandwidth of a spread spectrum signal. After spreading the data, it is transmitted using suitable modulation scheme. At the receiver the demodulated data is multiplied with the same PN sequences as used at the transmitter end. This reverse process decodes the transmitted data. The operation of a DSSS system is described in more details in the following sub-subsection.

2.4.1 Basic DSSS Transmitter

In basic DSSS technique, the binary data is modulo-2 added with a pseudo-random spreading signal before being phase modulated [23-24]. A DSSS using binary phase shift keying (BPSK) is expressed by Equation (2.1).

$$s(t) = \sqrt{2P_s}\, g(t) d(t) Cos(\omega_c t) \qquad (2.1)$$

Where $g(t)$ is a pseudorandom noise sequence having values ± 1 and $d(t)$ is the modulating signal. The characteristics of g(t) are very interesting, it is generated in a deterministic manner and is repetitive. The sequence length before repetition is usually extremely long and to all intents and purposes, we can assume that the sequence is truly random. There is no correlation at all between the value of a particular bit and the value of any other bits. Furthermore, the bit rate of $g(t)$ is usually much greater than the bit rate f_b of $d(t)$. As a matter of fact, the rate of $g(t)$ is usually so much greater than f_b, we say that $g(t)$ chops the bits of data into chips, and we call the rate of $g(t)$ the chiprate f_c, retaining the words, bit rate, to represent f_b [23].

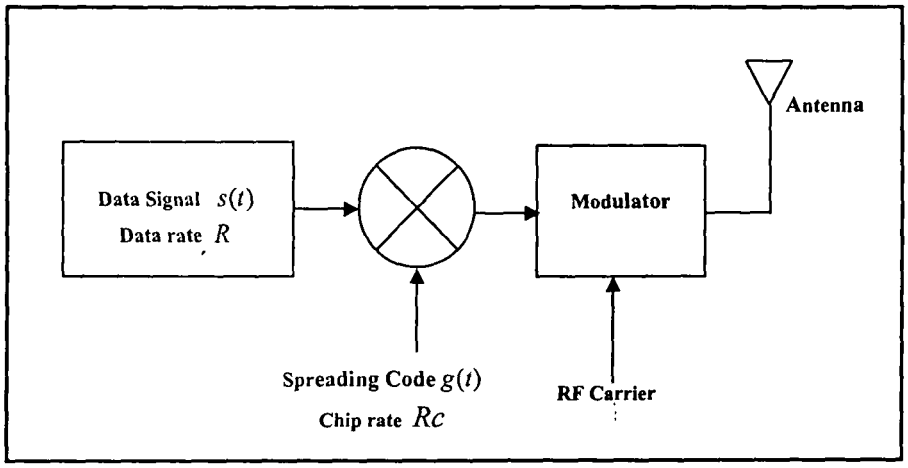

Fig.2.5: Block diagram of basic DSSS transmitter [23]

At transmitter the carrier signal is phase shifted according to spreading code. Generally, BPSK is used for modulating the carrier as it is easy to implement and have minimum bit error rate [23]-[24]. It is obtained by multiplying the carrier signal with the spreading code and Figure 2.5 shows the block diagram of the simple DSSS transmitter [23].

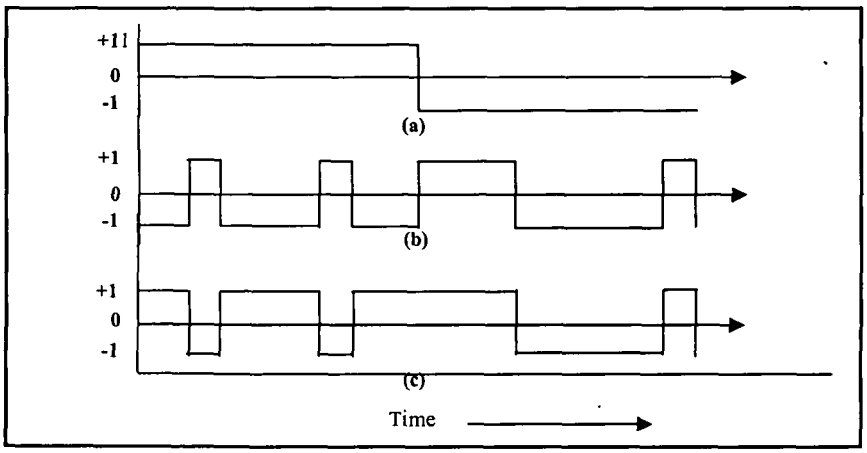

Fig.2.6: Data spreading in DSSS [23], (a) Input data, (b) PN sequence, (c) Data after spreading

For direct sequence, the amount of spreading is dependent upon the ratio of chips per bit of information. Figure 2.6 shows the DSSS spreading [23], (a)input data, (b) one chip, and (c) spreading code. If the data signal is narrowband compared to the spreading signal, the resulting product signal will have approximately the bandwidth of the spreading signal.

2.4.2 Processing gain in DSSS system

A fundamental issue in spread spectrum systems is how much protection spreading can provide against interfering signals with finite power. In DSSS communication the protection provided against the interfering signal is expressed in terms of processing gain. The higher the processing gain higher will be the data hiding and more is the protection. It is measured in decibels (dB) and simply measured by the ratio of number of chips per symbols to the number of bits encoded in one symbol [23]-[24].

For a DSSS system, binary data with a bit rate of R_b bits per sec (bps) is multiplied by a PN sequence at much higher rate and it provides the frequency spreading operation. This PN binary source outputs symbols called chips at a constant chip rate R_c chips per

sec (cps). The chip rate is always higher than the bit rate, and the ratio of the chip rate to the bit rate in dB is defined as the processing gain. The processing gain can be viewed as signal to jammer (interference) ratio at the receiver after the despreading operation (removal of PN). The larger the overall BW used, the higher the processing gain, assuming a constant data rate. A higher processing gain implies greater immunity against interference [24].

2.4.3 Basic DSSS Receiver

The DSSS receiver demodulated the received signals by multiplying with locally generated carrier signal $Cos(\omega_c t + \theta)$, then integrating over the chip duration. We assume perfect phase coherence and perfect timing synchronization between locally generated and received signals. The integrators and filter block remove the double or high frequency term generated by multiplication. The decision circuit compares the output of integrator with a preset value and translates the integrator output into digital data. These data are correlated with the local PN sequences which are replica of the PN sequences used at the transmitting end. Figure 2.7 shows the block diagram of the simple DSSS receiver [24].

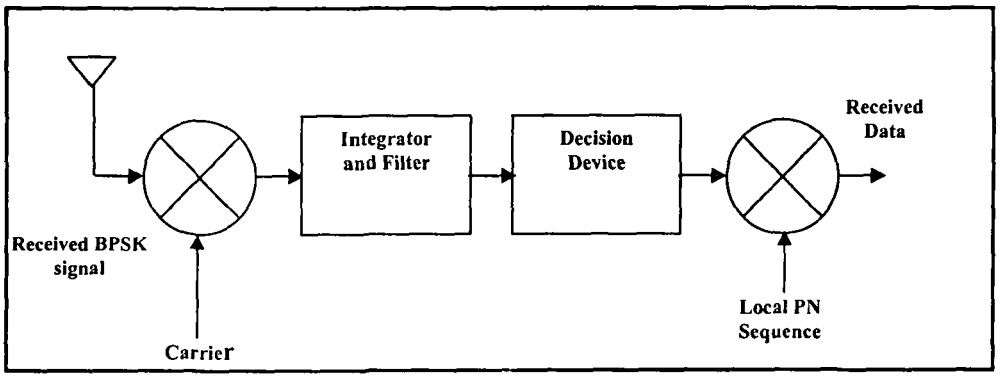

Fig.2.7: Block diagram of DSSS receiver [24]

This received coded PN sequence is multiplied with the locally generated and phase synchronized PN sequences using exclusive OR-gate. This process de-spreads the coded PN sequence and transmitted data is recovered as shown in Figure2.8 [24].

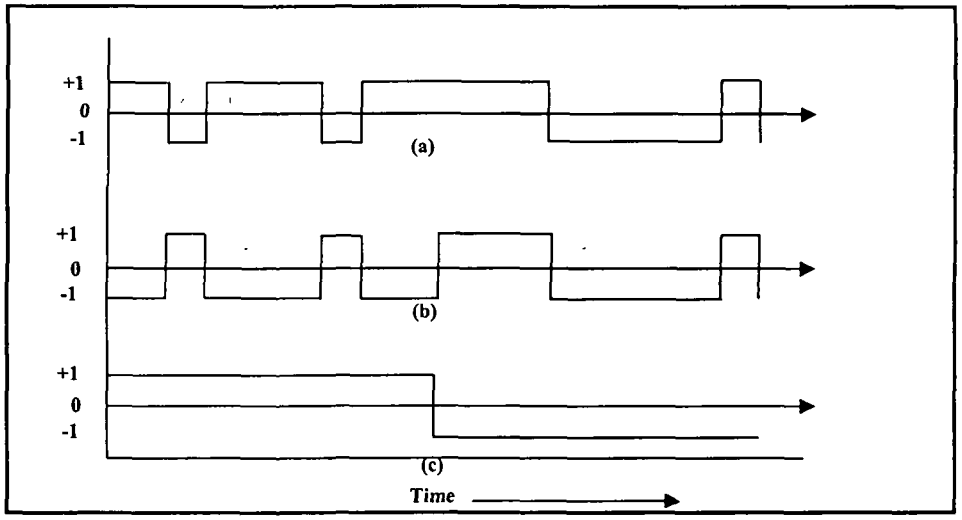

Fig.2.8: Data de-spreading in DSSS [24], (a) Received PN sequence, (b) Local PN sequence, (c) Decoded data

2.4.4 Code Phase Shift Keying Based DSSS Transmitter

Code-phase-shift keying (CPSK), is a M-ary DSSS modulation scheme proposed to increase the transmission efficiency of spread spectrum systems, and to overcome the spreading gain versus data rate limitation over a single channel [25]–[28]. Each of the signaling codes used to represent the input data symbols is obtained by cyclically shifting the same fundamental sequence, and is assumed to be a full period version of the fundamental sequence, i.e., the code period is equal to the symbol duration.

The CPSK transmitter groups the input data into K bit symbols with period T. The symbol value selects a signaling waveform from a M-ary alphabet ($M=2^K$). Each signaling waveform consists of a unique phase shift (by an integer number of code chips) of a single (maximal length) PN code sequence, $p(t)$, of length L and chip interval T_c.

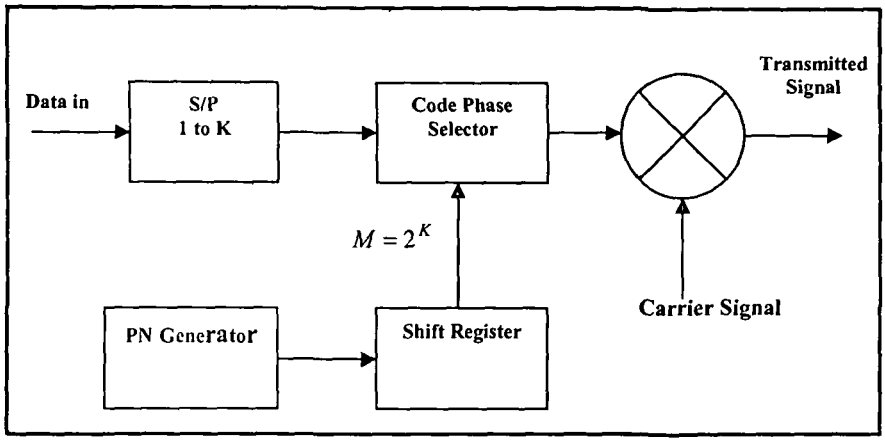

Fig.2.9: Block diagram of CPSK transmitter [25]

The selected waveform is modulated at carrier frequency ω radian/second. Suppose the value of the data symbol currently transmitted is $m(1 \le m \le M)$. The transmitter output is $s(t) = Ap_m(t)Cos(\omega t)$, where $p_m(t) = p(t - m_c T_c)$ is the m-th waveform in the signaling alphabet with phase shift (in the number of chips) $m_c = m\lfloor L/M \rfloor$. We assume that adjacent signaling waveforms in the alphabet are separated in phase by the same number of chips. The block diagram of CPSK based DSSS transmitter is shown in Fig-2.9 [25].

2.4.5 Code Phase Shift Keying Based DSSS Receiver

The block diagram of CPSK based DSSS receiver is shown in Fig (2.10). The received signal is multiplied with the carrier. The output of the demodulator is filtered and after passing through the wave shaping circuit applied to a bank of correlator. We assume that the receiver employs a bank of M correlators [27], as shown in Figure 2.10, or equivalently, a bank of M matched filters, each matched to the PN code with a specific phase shift as shown in Figure 2.9. Each filtered and processed PN sequence is processed in the correlator and integrator circuit before it is applied to decision device.

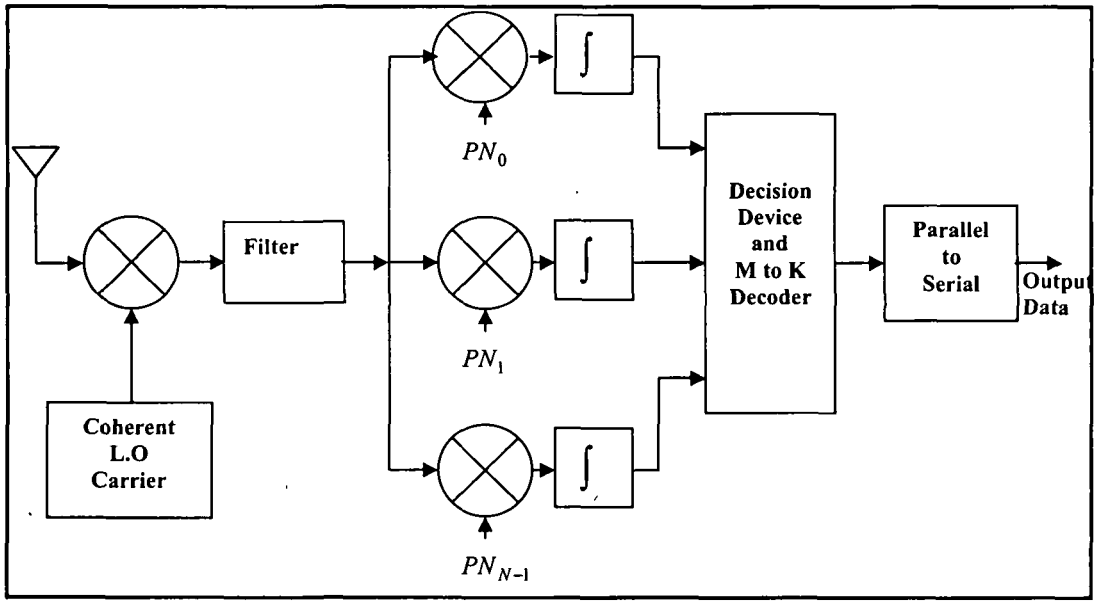

Fig.2:10: Block diagram of CPSK receiver [27]

The decision device determines the most likely phase shift of the received data stream in each symbol period and hence decodes the data symbol into K data bits. The correlators or matched filters require both chip and symbol interval synchronization for successful demodulation, both assumed to be perfect in the receiver. Decision device locates the correlator which gives the largest output and selects the corresponding symbol for parallel-to-serial decoding into the output data.

2.4.6 Code Division Multiple Access

In a code division multiple access (CDMA) system several users simultaneously transmit information over a common channel using pre-assigned code (Signature) waveforms [29]-[33]. The receiver has the knowledge of the signature codes of some or all users. It is then required to demodulate the information symbol sequences of these users upon reception of the sum of the transmitted signals of all the users in the presence of additive white Gaussian noise (AWGN).

In majority of the CDMA systems, each of the users transmits the information independently. Therefore, the transmitted signals of different users arrive asynchronously at the receiver. Since their relative time delays are arbitrary, it is inevitable that the cross correlations between signals of different users are nonzero. Low cross correlations among code waveforms for all relative time delays are obtained by the design of a set of complex code waveforms at the expense of an increased bandwidth. Since bandwidth is a valuable resource, the problem of interest is to accommodate as many users as can be reliably demodulated for a given bandwidth.

In CDMA transmitter each user transmits the signal using their own PN sequence code as simple DSSS signals [30]. This DSSS signal is obtained by modulating the carrier frequency with each code signal. The code signal consists of a number of code bits called "chips" that can be either +1 or -1. To obtain the desired spreading of the signal, the chip rate of the code signal must be much higher than the chip rate of the information signal. For the spreading modulation, various modulation techniques can be used, but usually some form of phase shift keying (PSK) like BPSK, differential binary phase shift keying (D-BPSK), quadrature phase shift keying (QPSK), or minimum shift keying (MSK) is employed.

The general approach to multiuser demodulation is to demodulate each user's signal as if it were the only one present. The receiver consists of a bank of correlators matched to each user's signal waveform in corresponding time and phase synchronism as shown in Figure 2.11 [29]. The K^{th} user's decision statistic consists of the desired signal component, AWGN and multiple access interference due to the cross correlation of the K^{th} user's signal with the signals from the other users. The receiver makes decisions by comparing the statistic signal with the signals from the other users. Thus, receiver makes decisions by comparing the statistic to a threshold and has the advantage of simplicity.

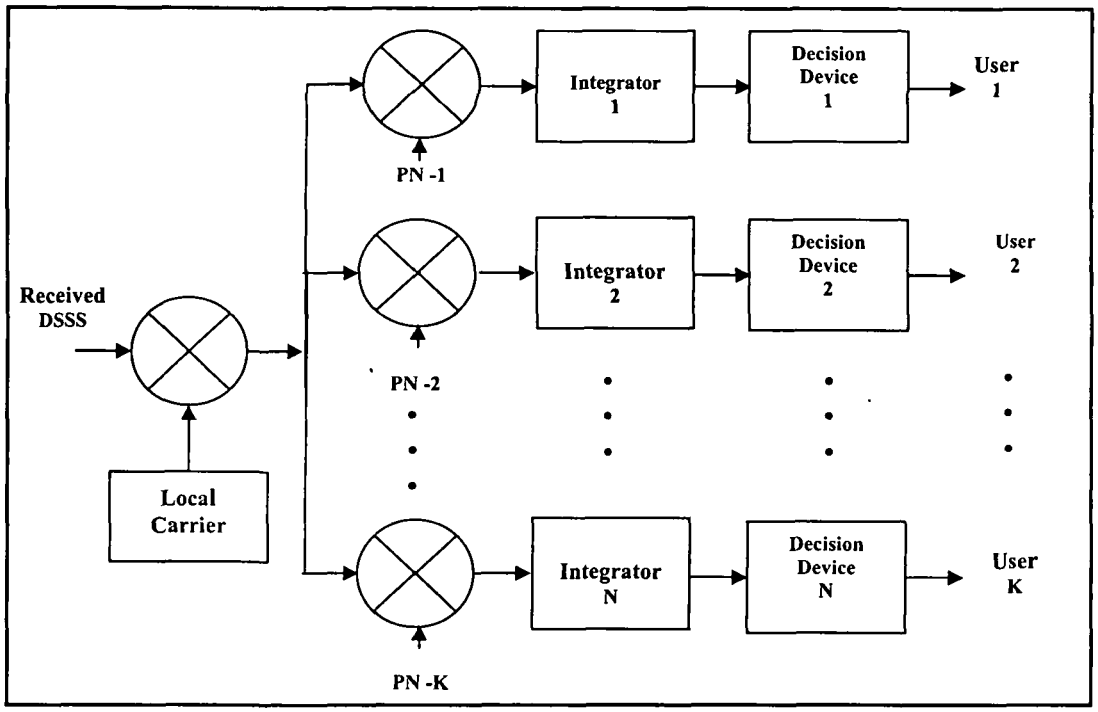

Fig.2.11: Block diagram of CDMA receiver system [29]

2.5 Frequency Hop Spread Spectrum

Frequency hopping (FH) [34]-[38] is a radio transmission technique where the signal is divided into multiple parts and then sent across the air in a random pattern of jumping or hopping, frequencies. When transmitting data, these multiple parts are data packets. The hopping pattern can be from several times per second to several thousand times per second. FH is the easiest spread spectrum modulation to use. Any radio with a digitally controlled frequency synthesizer can, theoretically, be converted to a FH radio. This conversion requires the addition of a PN code generator to select the frequencies for transmission or reception. Most hopping systems use uniform FH over a band of frequencies. An FH system can use analog or digital carrier modulation and can be designed using conventional narrow band radio techniques. De-hopping in the receiver is done by a synchronized PN code generator that drives the receiver's local oscillator

frequency synthesizer. FHSS splits the available frequency band into a series of small sub channels. A transmitter hops from sub channel to sub channel, transmitting short bursts of data on each channel for a predefined period, referred to as dwell time (the amount of time spent on each hop).

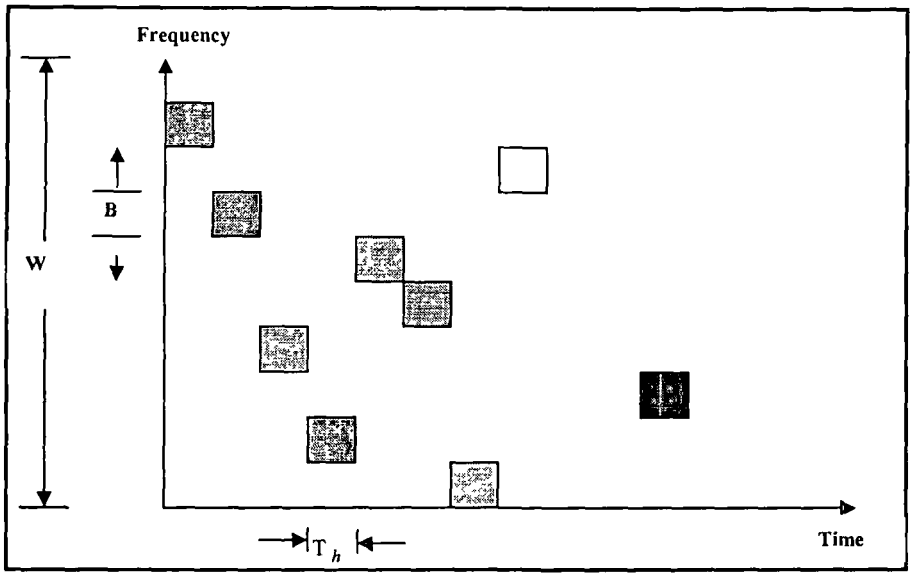

Fig.2.12: Basic concept of frequency hopping spread spectrum [35]

The hopping sequence is obviously synchronized between transmitter and receiver to enable communications to occur. In the FHSS a narrowband signal move or hops from one frequency to another using a PN to control hopping. This results in a signal's lingering at a predefined frequency for a short period of time, which limits the possibility of interference from another signal source generating radiated power at a specific hop frequency. Figure 2.12 shows the basic concept of FHSS transmitter [35].

2.5.1 Basic FHSS Transmitter

Figure 2.13 depicts the general form of a FH system [36]-[38]. The frequency synthesizers produce FH patterns determined by the time-varying multilevel sequence specified by the output bits of the code generators. In the transmitter, the data-

modulated signal is mixed with the synthesizer output pattern to produce the FH signal. An FH signal can be represented as:

$$S(t)=\sum_{i=-\infty}^{\infty} p(t-iT_c)Cos(2\pi f_i t+\phi_i) \tag{2.2}$$

where p(t) is the pulse shape used for the hopping waveform (typically assumed to be a square pulse), $f_i \in \{f_1, f_2, f_3 ..... f_N\}$ are the N hop frequencies, T_c is the hop period (also called the chip period), and ϕ_i's are the phases of each oscillator. Note that unlike in DSSS systems, the chip period (or hop period) does not impact the bandwidth expansion. Bandwidth expansion is completely determined by the number of hop frequencies.

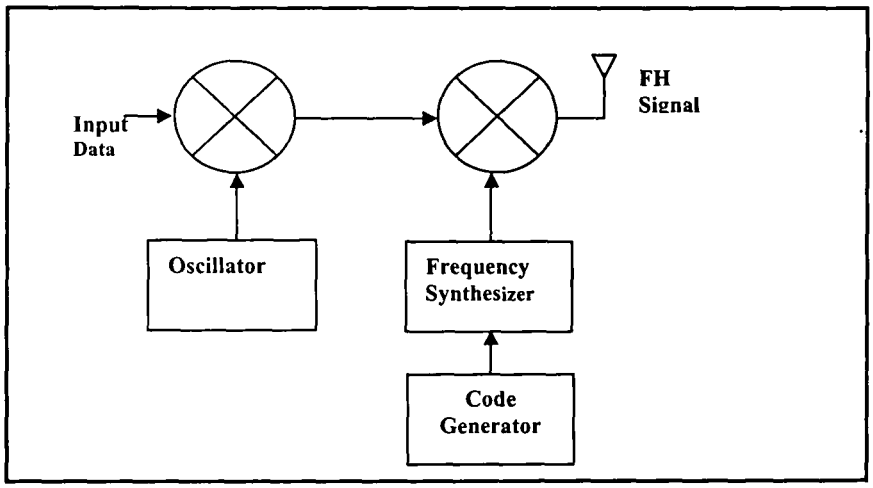

Fig.2.13: Block diagram of basic FHSS transmitter [36]

As discussed in the previous section, processing gain is a measure of shorthand description of the benefits which are provided by a particular spread spectrum system. As with DSSS we will formally define processing gain as the ratio of the bandwidth (W) to the bit rate (R_b) [39]:

$$\text{Processing Gain } (PG)=\frac{W}{R_b} \tag{2.3}$$

While we will define the number of non-overlapping frequency bands available for hopping as the bandwidth expansion factor N. However, it may be noted that in most cases of interest, the two will be equivalent and the processing gain will be equal to the common definition PG = N.

2.5.2 Basic FHSS Receiver

The receiver reverses the signal processing steps of the transmitter. The received signal is first de-hopped by mixing the output of synthesizer changing with the same spreading sequences as used at the transmitter side. The de-spread signal is demodulated by mixing the local carrier signal and original signal is recovered. The band pass filter after removing the harmonics and selecting the desired band of frequencies are applied to the demodulator stage (not shown in the block diagram). This stage process the output obtained from band pass filter and decodes the data as it was transmitted from the transmitter side. The performance of the receiver depends upon the amount of noise introduced in the channel. Block diagram of simple FHSS is shown in Figure 2.14 [36].

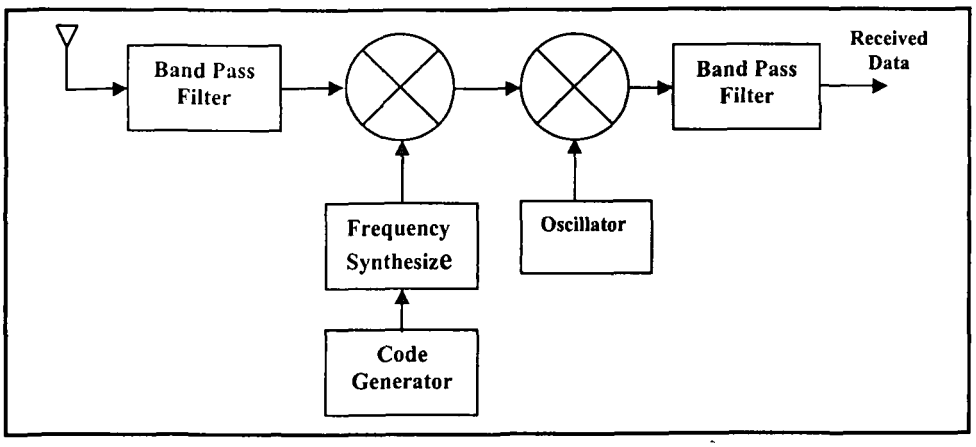

Fig.2.14: Block diagram of basic FHSS receiver [36]

2.5.3 M-ary FHSS Transmitter

In a FHSS, the frequency of the modulating signal shift by PN codes. The frequency shifting is performed by a frequency mixer (converter). The modulation most commonly

used with this technique is a M-ary frequency shift keying (MFSK) [36]-[39], where $K = Log_2 M$ information bits are used to determine which one of M frequencies is to be transmitted. The position of the M-ary signal set is shifted pseudorandomly by the frequency synthesizer over a hopping bandwidth. A typical FH/MFSK system block diagram is shown in Figure 2.15. In a conventional MFSK system, the data symbol modulates a fixed frequency carrier in an FH/MFSK the data symbol modulates a carrier whose frequency is pseudorandomly determined. In another case, a single tone is transmitted [38].

Generally, the FH system is a two-step modulation process in which both the data modulation and frequency hopping modulation are performed. However an FH system can be implemented as a single step whereby the frequency synthesizer produces a transmission tone based on the simultaneous the desired PN code and the data. At each frequency hop time, a PN generator feeds the frequency synthesizer a frequency word (as a sequence of chips), which selects one of symbol set positions. The frequency hopping bandwidths, and the minimum frequency spacing between hop positions, determine the minimum of chips necessary in the frequency word.

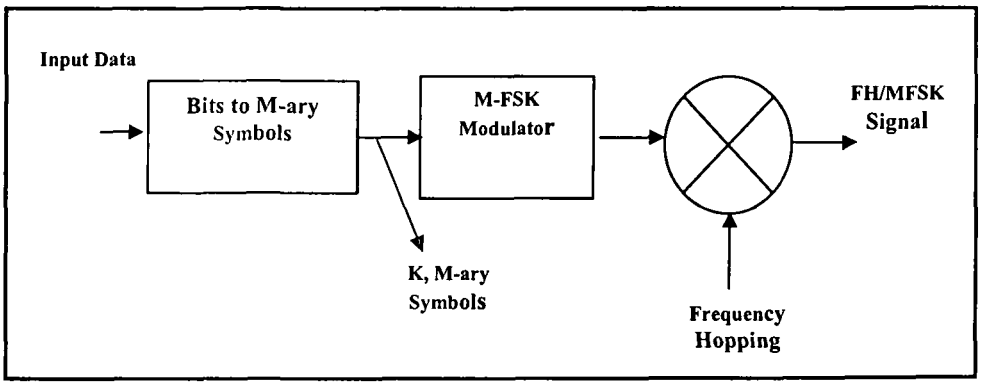

Fig.2.15: M-FSK spread spectrum transmitter [39]

2.5.4 M-ary FHSS Receiver

Figure 2.16 shows the block diagram of M- ary FSK receiver [36]-[39]. The received MFSK signal is filtered and passed to envelope detector. An envelope detector consists

of a rectifier and a low pass filter. The detectors are matched to the signal envelopes and not to the signals themselves. The phase of the carrier is of no importance in defining the envelope.

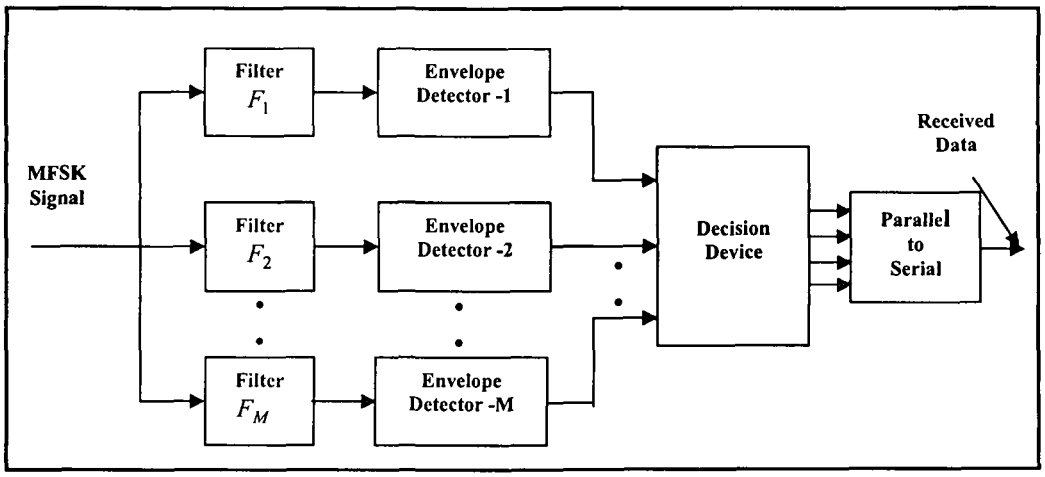

Fig.2.16: MFSK spread spectrum receiver [36]

2.5.5 Slow and Fast FHSS System

An FHSS system can be either fast hopping or slow hopping [40]-[45]. The system is said to be fast hopping if the frequency hop rate is larger than the symbol rate, i.e., if $1/T_h > 1/T_s$, where $1/T_s$ is the symbol rate [42]. Logically, a system is said to be slow hopping if $1/Th \leq 1/Ts$ [40]. We should here interpret $1/T_s$ as the rate of the possibly of coded symbols. For an un-coded system, the symbol rate is $\log2(M)/T_b$ where $1/T_b$ is the information bit rate, while for a system which employs a rate R_c error-control code, the symbol rate is $\log2(M)/(R_cT_b)$. For a slow hopping system, the frequency spacing between the signals alternatives must be a multiple of $1/Ts$ to allow for non coherent detection.

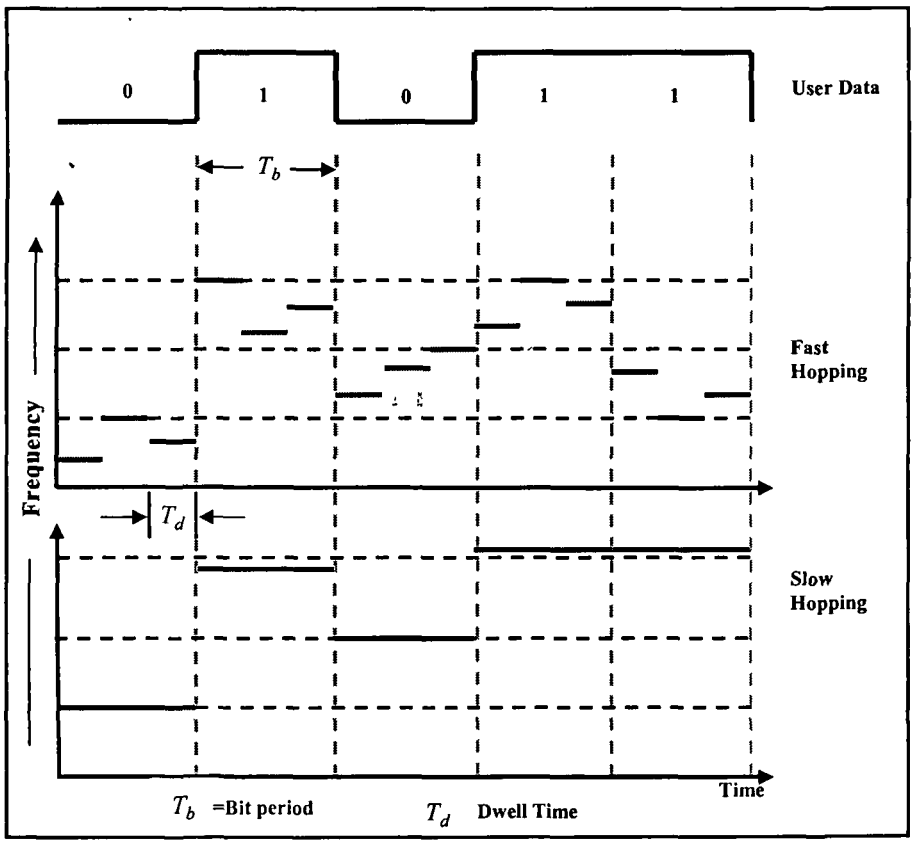

Fig.2.17: Time and hop relation in slow/fast hopping [42]

However, if the system is fast hopping, a symbol will span more than one hop, and we must ensure that the partial symbols within a hop are orthogonal (regardless of the carrier phase). Hence, the signal alternatives must be spaced by a multiple of $1/T_h$. To account for both fast and slow hopping systems, we define the chip rate as the maximum rate with which the transmitted signal can change frequency. Figure 2.17 plots the frequency occupancy versus time considering both the data modulation and frequency hopping.

2.5.6 Comparison between DSSS and FHSS

Table: 2.2 Comparison between DSSS and FHSS	
DSSS	**FHSS**
More complex and more efficient PSK modulation	Simple less complex FSK modulation
Avoids interference by spreading the energy over bands	Avoids interference source by hopping around it
Fast synchronization	Synchronization time is more
Transmission is Broad band continuously	At any instant the transmission is narrow band
Near far problem is dominant	Near far problem is less dominant
Bandwidth is low	Bandwidth is high
Low immunity to jamming/ Intentional interference	High Immunity to interference

Table:2.2 shows comparison between DSSS and FHSS systems. It is seen that although a DSSS system required less bandwidth than that of FHSS system, immunity to jamming noise/intentional interference of FHSS system is more than that of DSSS systems. Moreover DSSS system is more complex than that of FHSS, as the former used to spread of signal by spreading code and FHSS system is simple to implement by using frequency hopping. So both the spreading systems can be used as per requirement of applications. In this thesis, we have used both DSSS system and FHSS systems for providing multi services to multi users by introducing the multi-channel capability.

2.6 Noise in Communication Systems

When the signal is received from the channel and processed in the receiver, at the detector/demodulator stage the magnitude of the signal demodulated signal varies randomly. It is because the received signal accompanied/mixed with a voltage waveform which varies with time in an entirely unpredictable manner [23] -[24]. This unpredictable voltage waveform is the random process called noise. The signal

accompanied by noise is said to be contaminated or corrupted by noise. Noise is an unwanted electrical disturbance which gives rise to audible or visual disturbances in communication systems. The noise is picked from the channel and they are generated within the receiver also. The main sources of noise are as described in the following sub-section.

Undesired electrical signals which are introduced with a message signal during the transmission, and processing, are called noise. Noise, thus, is an unwanted signal that corrupts a desired message signal. In general, noise may be predictable, or unpredictable in nature. The predictable noise can be estimated, and eliminated, by proper design. Some examples of such noise are: power supply hum, spurious oscillation in feedback amplifiers, ignition radiation pick-up, fluorescent lighting. The predictable noise generally is man-made and can be eliminated.

Unpredictable noise varies randomly with time and, as such, we have no control over this noise. Identification of the message signal at the receiver depends upon the amount of noise accompanied by the message during the process of communication. In the absence of noise, identification of the message signal is perfect. The presence of noise complicates the systems of communication. The amount of noise power present in the received signal decides the minimum power level of the desired message signal at the transmitter. The term noise normally used to refer the unpredictable or random noise.

There are many sources of noise. The natural phenomena that give rise to noise are solar flares, electronic storms and radiation in space. The noise received by the receiving antenna from the natural sources can be reduced by repositioning the antenna. Noise originating from the sun and outer space is known as extraterrestrial noise. Noises are also generated within the electronic equipments. Such noises are categorized as thermal noise, shot noise, partition noise, flicker noise and transit noise. By proper design these noise can be kept to minimum magnitude. These cannot be eliminated completely. The noises and disturbances picked up from the channel are the main cause

of performance degradation. Such noises are additive white Gaussian noise (AWGN), jamming noise due to multiple access interference.

2.6.1 Additive White Gaussian Noise

White light contains all colour frequencies. In the same way, white noise too contains all frequencies in equal amount. The power density spectrum of a white noise is independent of frequency [46]-[51] which means it contains all the frequency components in equal amount. When the probability of occurrence of a white noise level is specified by a Gaussian distribution function, it is known as White Gaussian Noise. Shot noise and thermal noise are considered as white Gaussian noise for all practical purposes. The power density of white noise is given in Figure (2.18).

$$S_w(\omega) = \frac{N_o}{2} \qquad (2.5)$$

This equation shows that the power spectral density of white noise is independent of frequency. As N_o is constant, the power spectral density (psd) is uniform over the entire frequency range including the positive as well as the negative frequencies. N_o in equation (2.7) is defined as:

$$N_o = KT_e \qquad (2.6)$$

Where, K =Boltzmann's constant and

T_e = Equivalent noise temperature of the system.

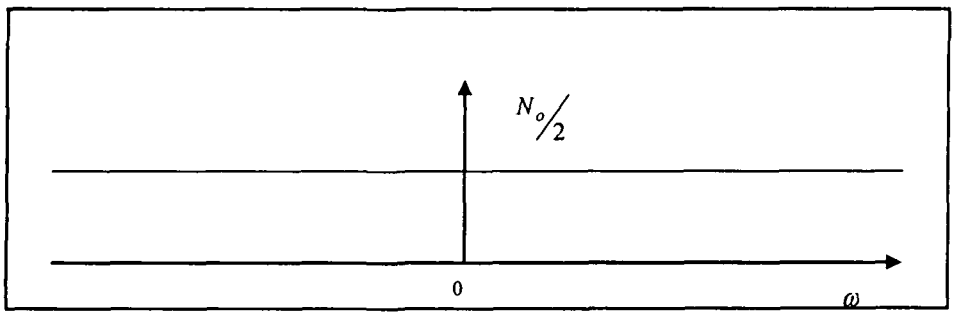

Fig.2.18: Power density of additive white Gaussian noise [46]

2.6.2 Jamming Noise

In wireless networks, a principal necessity is the ability to securely and effectively communicate with intended receivers. Due to the broadcast nature of the wireless medium, however, a jamming adversary can send interfering signals to efficiently stop valid communication. The goals of a jammer are to deny reliable communication to his adversary and to accomplish this at a minimum cost [46]. Extensive research has shown that mounting a jamming attack can be an effective denial of service attack, with many proposed techniques available. She can jam messages by transmitting high power signals that cause the original signal to become unreadable by the receiver. The fraction of the message that the attacker has to interfere with to successfully jam depends on the used coding scheme. She can modify messages by either flipping single message bits or by entirely overshadowing original messages. In the former, the attacker superimposes a signal on the radio channel that converts one or several bits in the original message from zero to one or vice versa. In the latter, the attacker's signal is of such high power that it entirely covers the original signal at the receiver. As a result, the original signal is reduced to noise in the attacker's signal and the original message is replaced by the attacker's message.

2.6.3 Jamming to Signal Ratio

The source of interference is assumed to be wideband Gaussian noise power from a jammer in addition to thermal noise. Therefore, the SNR of interest is $E_b/(N_o + J_O)$, where J_o is the noise power spectral, assumed equal to density due to the jammer. Unless otherwise specified, J_o is assumed equal to J/W_{ss}, where J is the average received jammer power and W_{ss} is the spread-spectrum bandwidth. Since the jammer power is generally much greater than the thermal noise power, the SNR of interest is a jammed environment usually taken to be E_b/J_o. Therefore we define $\left(E_b/J_o\right)_{reqd}$ as the

bit energy per jammer noise power spectral density required for maintaining a specified error probability [51]. The parameter E_b can be written as:

$$E_b = ST_b = \frac{S}{R} \tag{2.7}$$

where S is the received signal power, T_b the bit duration, and R the data rate in bits/s.

Then we can express $\left(E_b/J_o\right)_{reqd}$ as:

$$\left(\frac{E_b}{J_o}\right)_{reqd} = \left(\frac{S/R}{J/W_{ss}}\right)_{reqd} = \frac{W_{ss}/R}{(J/S)_{reqd}} = \frac{G_p}{(J/S)_{reqd}} \tag{2.8}$$

Where $G_p = W_{ss}/R$ representsand canocessing gain, and $\left(E_b/J_o\right)_{reqd}$ can be written as:

$$\left(\frac{J}{S}\right)_{reqd} = \frac{G_p}{\left(E_b/J_o\right)_{reqd}} \tag{2.9}$$

The radio $\left(E_b/J_o\right)_{reqd}$ is a figure of merit that provides a measure of system invulnerable to interference. The larger the $\left(E_b/J_o\right)_{reqd}$, the greater is the system's noise rejection capability, since the figure of merit describes how much noise power relative to signal power is required in order to degrade the system's specified error performance.

2.7 Bit Error Rate

The performance of digital communication system is the measure of bit error rate (BER) and it also quantifies the reliability of the entire radio system [46] -[47]. From simple definition it is expressed as:

$$BER = \frac{Error}{Total\ \ Number\ \ of\ \ bits} \tag{2.10}$$

Noise is the main enemy of BER performance and it is a random process, defined in terms of statistics. The noise introduced by the circuitry is described by a Gaussian probability density function, while the signal path is usually described by a Rayleigh probability density function. A Rayleigh, or fading, the signal path is not noise in the intuitive sense of the familiar hissing sound of white noise, but it is a random process that is analyzed in the same manner as Gaussian noise. One way to lower the spectral noise density is to reduce the bandwidth, but we are limited by the bandwidth required to transmit the desired bit rate. We can also increase the energy per bit by using higher power transmission, but interference with other systems can limit that option.

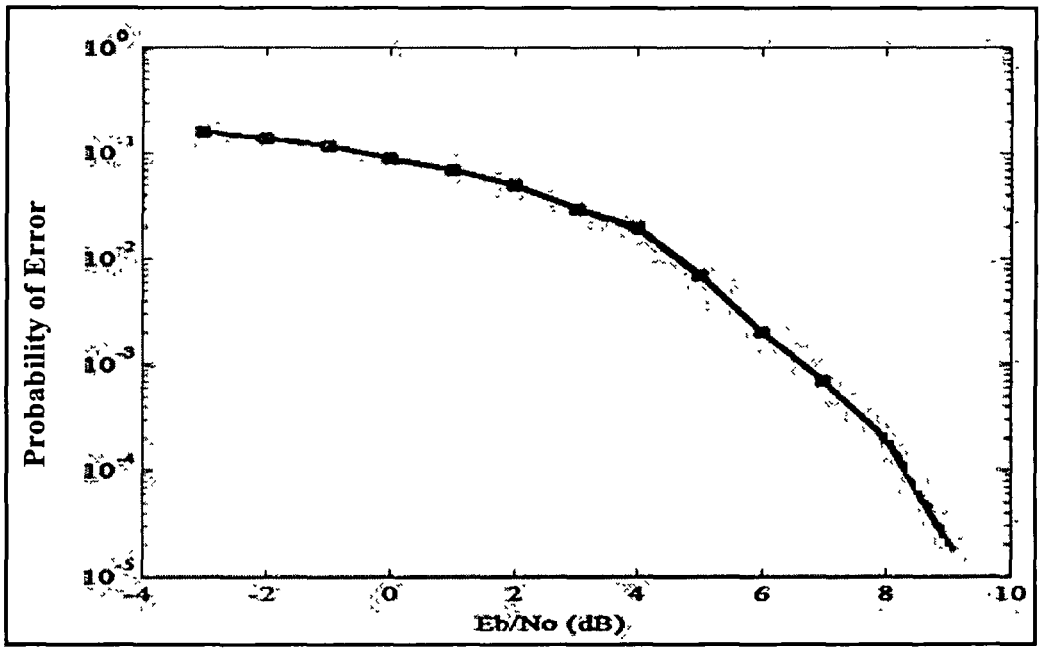

Fig.2.19: BER Performance of a BPSK system under AWGN [47]

A lower bit rate increases the energy per bit, but we lose capacity. Ultimately, optimizing E_b/N_o is a balancing act among these factors. BER rate also depends upon the modulation methods and among all modulation techniques, the BPSK has the least

value of BER [6]. The theoretical value of bit error probability for BPSK is given by Equation (2.9) and plotted in Figure (2.19) [40].

$$P_b = Q\left(\sqrt{2\frac{E_b}{N_o}}\right) \tag{2.11}$$

In our works, we have studied BER performances taking AWGN and jamming noise for our proposed DSSS and FHSS systems which are discussed in Chapter 5 and 7 respectively.

2.8 Conclusion

This chapter presents an overview of spread spectrum for wireless communications. PN sequences are very essential elements of spread spectrum technology. Different PN sequences with their types and properties are discussed briefly. DSSS and FHSS techniques are the two techniques for spread spectrum; these are described by the block diagram for single user communications. Recently, an M-ary keying technique has been introduced with the spread spectrum to increase the processing gain of the spread spectrum system for single user. It has been focused with block diagram and principle of operation. From the comparison shown between DSSS and FHSS, it is projected that although DSSS requires less bandwidth than that of FHSS system, immunity to intentional interference/jamming of FHSS system is more than that of DSSS. The near/far problem is serious in DSSS (CDMA) and tight power control with attendant complexity, is needed to combat it For performance evaluation of a wireless system, noises specially AWGN and jamming noise are very essential. These are discussed with the BER performance of a wireless system.

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Chapter 3

Review of Multiplexing and Multiple Access Techniques and their Evaluation for Wireless Communications

3.1 Introduction

This chapter enumerates the basic concepts of the different multiplexing and multiple accesses techniques and related previous works. The multiplexing and multiple access techniques are based mainly on three techniques: time division, frequency division and code division. Apart from these, space division multiplexing is also used to transfer the data at higher rate by using multiple antennas. Keeping in view the above mentioned multiplexing and multiple access techniques this chapter is organized as follows.

Section 3.2 introduces multiplexing and multiple access techniques, such as, time division, frequency division code division and space division. These techniques are reviewed since their evolution and contribution of some authors in this field is described. The advancement in design and fabrication of VLSI technology has played a dominating role in addressing the challenges of wireless communication. Further, this has improved the quality, reliability and capacity of systems using different signal processing techniques. Section 3.3 and 3.4 discuss different demodulators used for demodulation of binary phase shift keying signal and sinusoidal frequency to voltage conversion techniques. Section 3.5 discusses the growth of wireless users. The exponential growth of users from wired communication to wireless has motivated to enhance the efficient use of existing spectrum. Finally, the conclusion is given in section in section 3.6.

3.2 Multiplexing

In multiplexing techniques various communication systems/channels are connected together those shares a common channel [1] -[2]. Fig-3.1 shows the basic principle of multiplexing for sharing a common channel by K-number of users. The frequency division, time division, code division and spatial division are the most common techniques for multi-channel signaling with a single channel. We will discuss them briefly with their history.

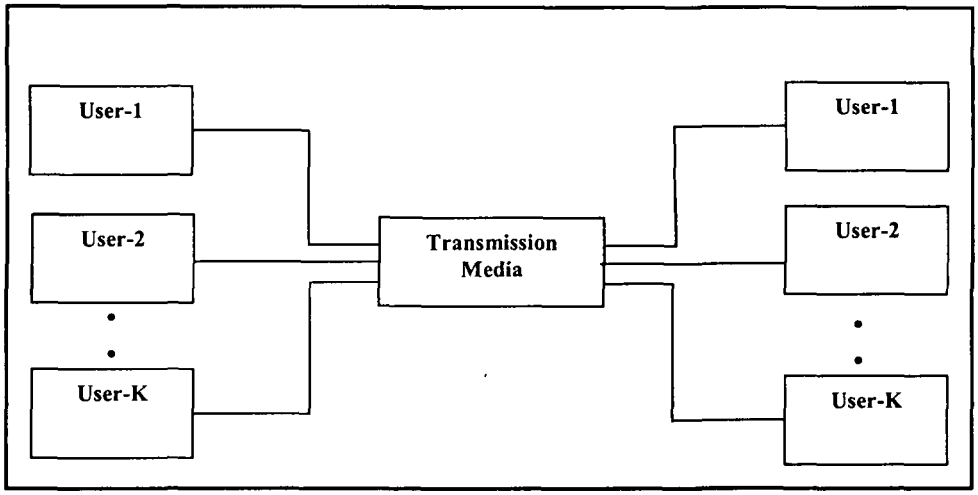

Fig.3.1 Principle of multiplexing [2]

3.2.1 Time Division Multiplexing and Time Division Multiple Accesses

Immediately after the commercial success of the telegraph in 1840, using telegraphic codes (dots and dashes) on physical lines, the necessity of simultaneous transmission of many users' signals over a single channel was realized to increase the capacity. Many methods were proposed by F. C. Bakewell, A. V. Newton and M. B. Farmer for implementing TDM using synchronously driven rotating commutators [3]. Theoretically and Technically improved methods were then developed by B. Meyer, J. M. E. Baudot, as well as P. Lacour and P. B. Delany. Willard M. Miner has invented the TDM system based on fast rotating commutators, Figure3.2 and Figure 3.3. Sampling theorem was not developed at that time therefore it was revealed from this experiment that as the speed of commutator goes near the upper frequency components of speech, the best result was obtained.

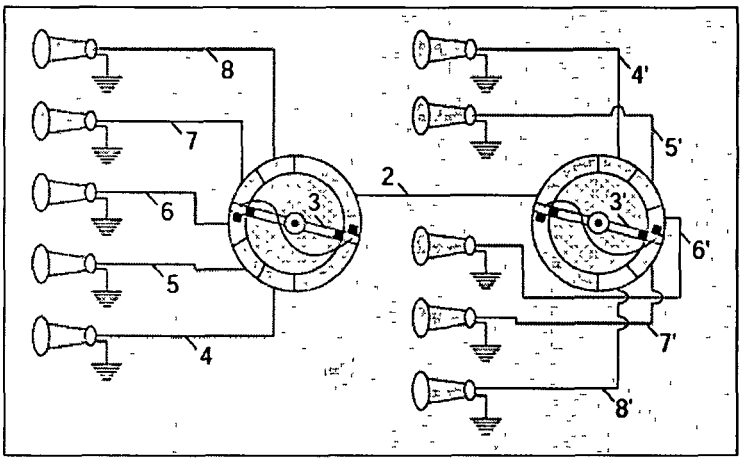

Fig.3.2: Block diagram of commutator based TDM system [3]

As telephony became increasingly more widespread, a new opportunity for multiplex signal transmission arose. The problem of time-division multiplex in telephony is in fact closely related to a sampling problem. Till now it was not clear whether the samples can be instantaneous or have nonzero duration. Early work on the multiplexing of telephony signals, such as that done by Willard Miner [4] was experimental and the sampling frequency was determined by trial and error. Raabe's [5] thesis published in 1939 goes further than mere experimentation. The author has described and analyzed a TDM system for telephony. He also has demonstrated a thorough understanding of sampling, including sampling with pulses of finite duration and sampling of low-pass, band-pass signals. Raabe showed that a number of channels carrying telephony signals could be multiplexed and reconstructed with arbitrarily small error, provided that a certain condition is met The condition was known as 'Raabe's condition' state that the sampling frequency must exceed twice the maximum frequency of the multiplexed signal.

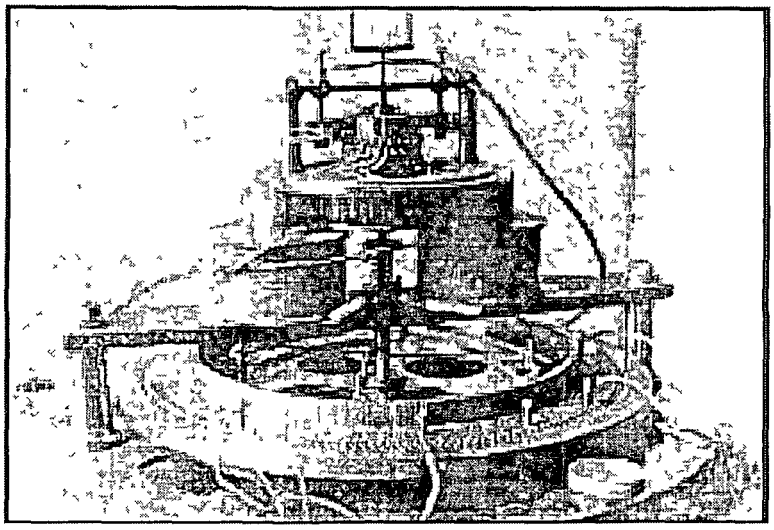

Fig.3.3: Pattern distributor (Sampling machine) [3]

Pulse code modulation (PCM) for telephony was invented in 1937 by Alec. H. Reeves while working for line-of sight microwave links [6]. Further, during the World War II, the PCM was further developed under the guidance of Harold S for designing a practical system for the U.S. Army Signal Corps. Because of unavailability of suitable, cheap, long-life components it took long time and could not be justified suitable for civilian applications.

Further, Godaal [7] described an experiment for TDM system using PCM to transmit sampled amplitude of PAM signal by groups of ON/OFF pulses and experimental equipment for coding the PAM pulses at the transmitter and decoding the PCM pulses at the receiver. The experimental results have shown the necessity of a three unit code for a minimum grade of circuit and suggested a six or seven unit code to provide good quality. .

PCM technology has been further improved with the development of integrated circuit technology and processor controlled switching systems. Gallagher [8] has described a non-blocking processor-controlled digital TDM switching system for six,

24-channel digital TDM trunk groups and 48 analog lines. This system used integrated circuit technology and stored program processor to for capacity improvement.

Davis & Reilly [9] discussed the T1 carrier evolution. In 1962, engineers from Bell Labs developed the first T1 Channel Banks, which combined 24 digitized used TDM. Further this 24 channel system was extended to 48-channel system to offer the advantage of more efficient cable utilization. But due to growing demand from new users, there was a capacity saturation problem.

With the launch of satellite communication, the technique of time division multiple accesses (TDMA), has got considerable interest for wireless communication [10]-[11]. Multiple accesses may be considered as a special kind of multiplexing, in which two or more signals, each from a different location, are sent by radio to a single transponder. Figure 3.4 shows the basic principle of TDMA for accommodating N-channels.

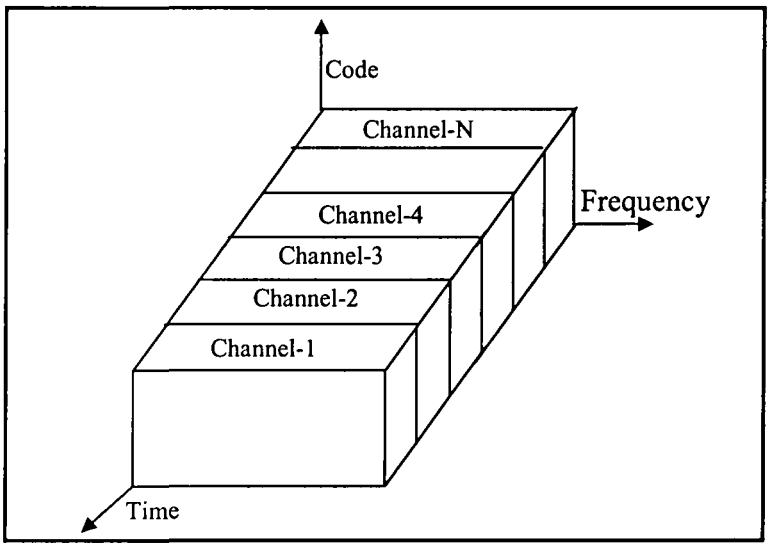

Fig.3.4: Principle of TDMA [40]

To evaluate the multiple access capability with the TDMA technique [12], Sekimoto *et al.* [12] had carried out field test using INTELSAT I (Early Bird) to evaluate the multiple access capability with TDMA technique. The information obtained during this

experiment is being used to design a high-capacity 600-channel, 50-Mbps TDMA system that allowed up to 30 accesses.

In [13], Mohanti has studied multi access capability of TDMA and spread spectrum techniques for satellite communication. He found that the combination of TDMA and SSMA can be used for asynchronous and reliable transmission of digital or analog signals.

Suguri *et al.* [14] showed that TDMA is a practical system for communications with satellites and communication rate up to 13 Mbit/s, 4 phases, and 27 Mbit/s, 2 phases were feasible. The system information capacity is about 480 voice channels with a 7-bit quantization code at these bit rates

Using satellite communication, the techniques of TDMA/FDMA were studied in by Krister Raith *et al.* [15] for capacity issue. The authors have shown that there was an improvement in the capacity by 10 times using analog FDMA. In the long range, microcellular technology combined with adaptive channel allocation (ACA) will move this into the personal communication capacity range. ACA also eliminates the need to plan frequencies for cell.

Riaz Ahmad [16] has pointed out that TDMA is the only technology to offer an efficient utilization of hierarchical cell structures (HCSs) offering pico, micro, and macrocells. By using this approach, system capacities of more than 40-times can be achieved in a cost-efficient way. Because of its inherent compatibility with FDMA analog systems, TDMA allows service compatibility with the use of dual-mode handsets.

Krishnamurthy *et al.* [17] have studied the TDM approach within an integrated receiver to reduce the power, area and cost of multiple antennas. Authors have developed simple closed form noise figure relations in terms of the number of multiplex channels and the anti-alias filter rejection. These simple relations provides a quick method of determining the expected noise figure of such systems. A four-antenna 2.4 GHz LNA array circuit in CMOS is designed in a 0.18 μm technology. The results

obtained show close agreement with the developed model of the TDM-based multi antenna receiver system.

3.2.2 Frequency Division Multiplexing and Frequency Division Multiple Access

There are many reported works on the history of evolution of frequency division multiplexing (FDM) techniques. In these papers authors highlighted that the FDM technique was evolved by Alexander Graham Bell, while experimenting with a telegraph multiplexing system Figure 3.5. Alexander Graham Bell had recognized the possibility of transmitting the voice itself as an analog signal and Bell called it harmonic telegraph (carrier multiplexing) system in 1876 [18]-[19]. But there were not adequate electrical components and technology to make this carrier multiplexing concept possible at that time.

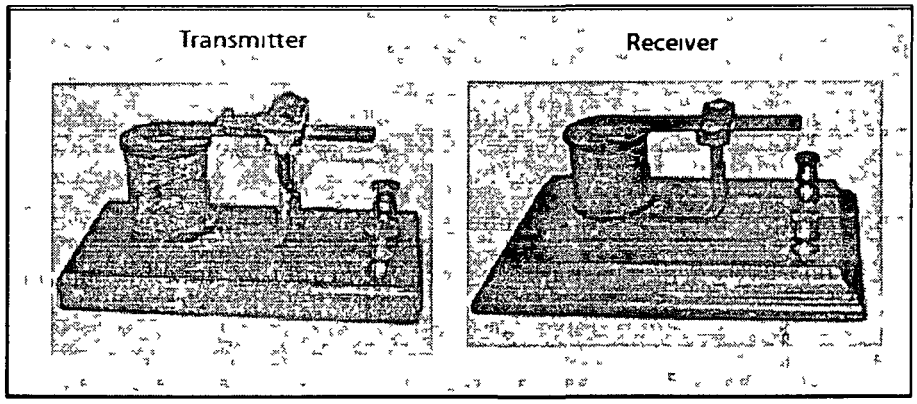

Fig.3.5: Bell's harmonic telegraph system [18]

Schwartz [20] described the first demonstration of a carrier multiplexed system that was carried out by then Major George Owen Squier of the U. S. Army Signal Corps on September 18, 1910 in Washington, DC. In this demonstration Squier transmitted two

simultaneous analog voice signals. One signal was that of a normal telephone circuit conversation and other signal was a modulated high-frequency signal, with the high-frequency carrier used in the experiments varying in frequency from 20 KHz to 100 KHz. Since the high-frequency signal used wireless techniques, Squier coined the term "wired wireless" to represent his method of carrier multiplexing. But this work was assessed as of no great commercial use since the high-frequency attenuation of signals over telephone lines would be so great as to require enormous power for transmission.

With the development of wireless communication and technology, the multiplexing technique using carrier (FDM) had waited till 1918 when first commercial implementation of carrier multiplexing for telephony was introduced by AT&T in the United States. This system enabled five simultaneous conversations to be carried over a single pair of wires, thus improving telephone communications capability significantly. FDM became the main multiplexing mechanism for telephone carrier systems. Bandwidth and dispersion were not serious problems with the relatively modest spacing of repeaters, and 8 kHz sub channel spacing was provided for 4 kHz voice signals. This N2 carrier system of the mid-1960s used double sideband amplitude modulation and transmitted up to 200 miles Figure 3.6. With the introduction of digital telephony, FDM carrier systems with individual sub channels for voice signals began in the 1970.

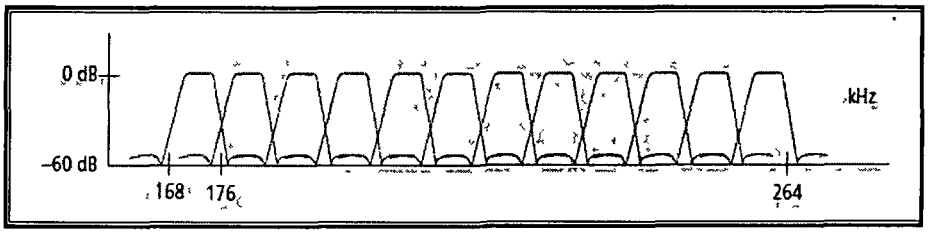

Fig.3.6: N2 Carrier system for FDM [18]

Just like TDMA, FDMA also got its recognition after the launch of commercial application of satellite communication and cellular service in 1970 and 1980 respectively [21] -[22]. A geostationary satellite using an earth coverage antenna can see

approximately one-third of the earth's surface. The satellite can see any point within its viewing area and works as a means of multiple accesses. Figure 3.7 shows the block diagram of FDMA [40].

FDMA was the first multiple access technique used in satellite communication systems. When satellite communications began in the 1960s, most of the traffic carried by satellites was telephony. All signals were analog, and analog multiplexing was used at earth stations to combine large numbers of telephone channels into a single baseband signal that could be modulated onto a single radio frequency (RF) carrier. Individual telephone channels can be shifted in frequency from baseband to a higher frequency so that they can be stacked into a group of channels using FDMA.

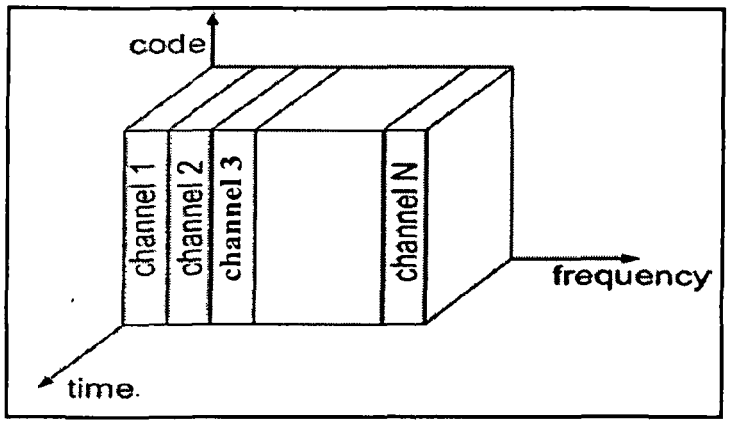

Fig.3.7: Principle of FDMA [40]

The following paragraph surveys the work carried out by some authors on FDMA briefly.

Vitalice *et al.* [23] have presented framed and burst acquisition in a satellite communication network and results showed that when the false alarm rate was low the probability of detection also low, and the acquisition time was long. The effect of timing errors on these results is to shift down lowering detection probabilities and shift the

curves for increasing the acquisition time. What was also observed was that as the length N of the unique word was increased, the performance got better.

To address the problem of Gaussian multiple-access channel with inter symbol interference Yu *et al.* [24] proposed a numerical method for characterizing the rate region achievable with FDMA. The proposed algorithm is based on the observation that the optimal frequency partition has a two-band structure when the signal-to-noise ratio is high. The FDMA-capacity algorithm is used to devise the optimal frequency-division duplex plan for very-high-speed digital subscriber lines.

To support different type of user with different data rate and with spectral efficiency, Poonam *et al.* [25] proposed a novel access scheme using with TDMA, FDMA and CDMA. It exploits the advantage given by the combination of spread spectrum with multi-carrier modulation and as well as TDMA.

In [26], Kim *et al.* presented efficient radio interference technology for a B3G satellite system. In order to maximize the efficiency, the authors have introduced techniques which have the maximum compatibility to those of the terrestrial system specifications, adopting FDM. The proposed satellite specific technique is different from that of the terrestrial system in order to reflect the characteristics of the satellite systems. A few simulation results demonstrate that the proposed scheme can be effectively utilized in order to provide efficient B3G satellite.

3.2.3 Code Division Multiplexing and Code Division Multiple Access

The introduction of frequency reuse concept in cellular technology greatly expanded the efficiency and capacity. The first cellular service in the world was introduced in the year 1980 using analog radio transmission as advanced mobile phone system (AMPS) [10]. Within a few years, cellular systems began to face the challenge of capacity saturation as more and more users started demanding mobile service. To solve this problem and to accommodate more number of users a new set of digital wireless technology called

TDMA and GSM (Global system for mobile) was developed [16]. But just as TDMA was being standardized, an even better solution was found in CDMA. Fig-3.8 shows the basic principle of CDMA.

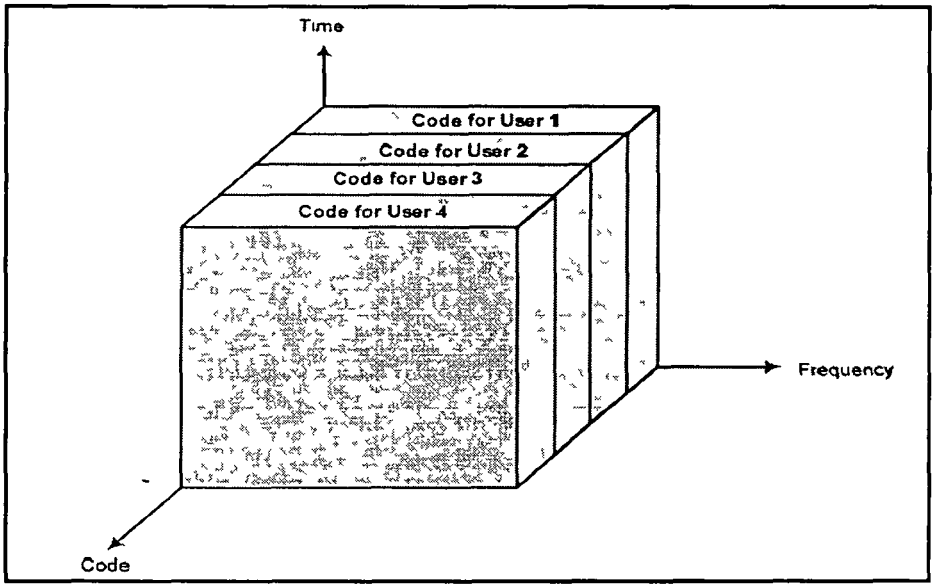

Fig.3.8: Concept of CDMA [40]

The founders of quality communication (QUALCOMM) realized that CDMA technology could be used in commercial cellular communications to make even better use of the radio spectrum than other technologies [40]. They developed the key advances that made CDMA suitable for cellular, then demonstrated a working prototype and began to license the technology to telecom equipment manufacturers. The first CDMA networks were commercially launched in 1995, and provided roughly 10 times more capacity than analog networks - far more than TDMA or GSM. Since then, CDMA has become the fastest-growing multiple access technique of all wireless technologies [30]-[31].

In CDMA systems all users transmit in the same bandwidth simultaneously and this concept leads to spread spectrum systems [30]. In this transmission technique, the

frequency spectrum of a data-signal is spread using a code uncorrelated with that signal. As a result the bandwidth occupancy is much higher than required as shown in Figure 3.9. The PN codes used for spreading have low cross-correlation values and are unique to every user. This is the reason that a receiver which has knowledge about the code of the intended transmitter is capable of selecting the desired signal.

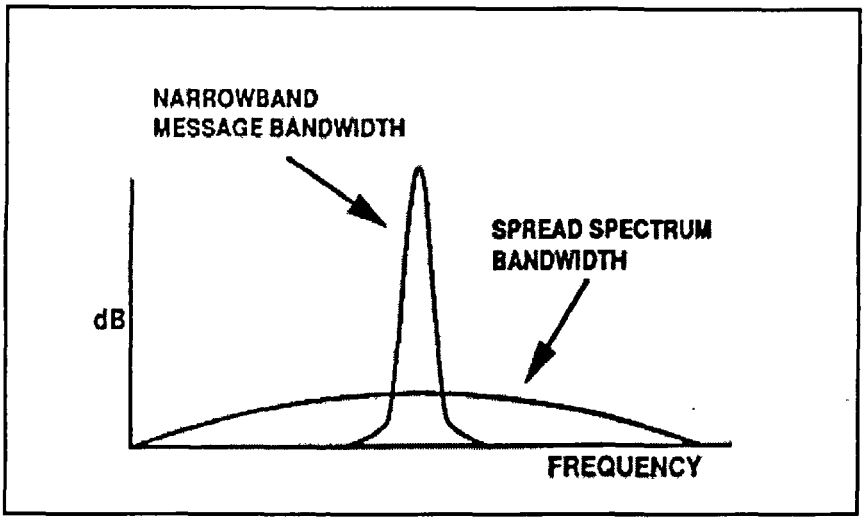

Fig.3.9: Bandwidth of signal before and after spreading [30]

CDMA system has a number of advantages as:

- Low power spectral density. As the signal is spread over a large frequency-band, the Power level is low.
- Spectral Density is getting very small, so other communications systems do not suffer from this kind of communications. However the Gaussian Noise level is increasing.
- Interference limited operation. In all situations the whole frequency-spectrum is used.

- Privacy due to unknown random codes. The applied codes are - in principle - unknown to a hostile user. This means that it is hardly possible to detect the message of another user.
- Applying spread spectrum implies the reduction of multi-path effects.
- Good anti-jam performance.

Figure 3.10 give the block diagram presentations of transmitter system.

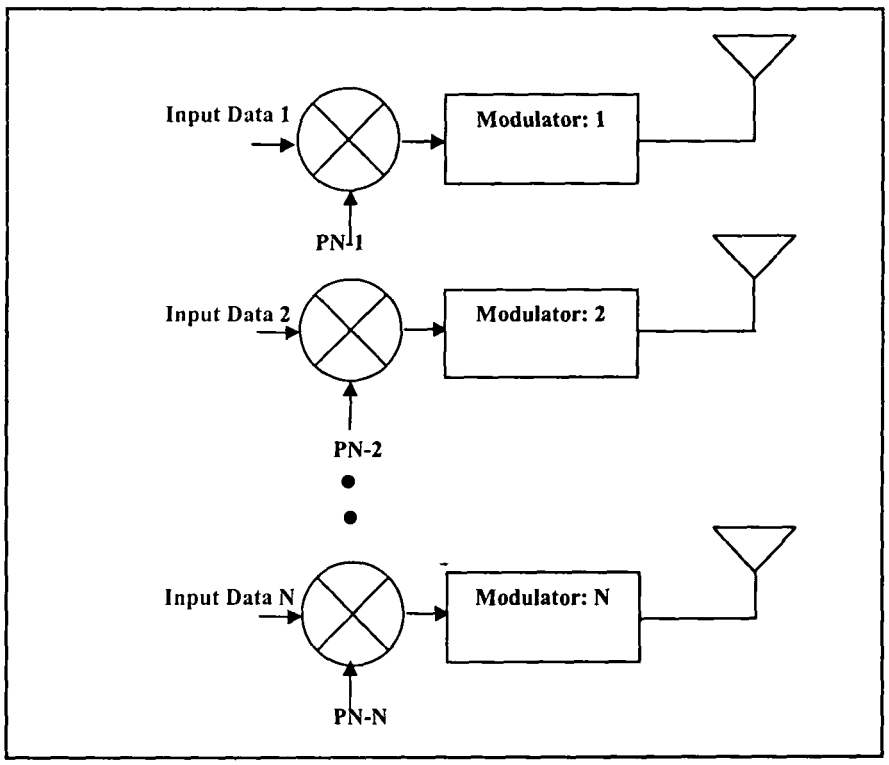

Fig.3.10: Block diagram N-channel CDMA transmitter [40]

Figure 3.11 gives the block diagram presentation of receiver for CDMA system.

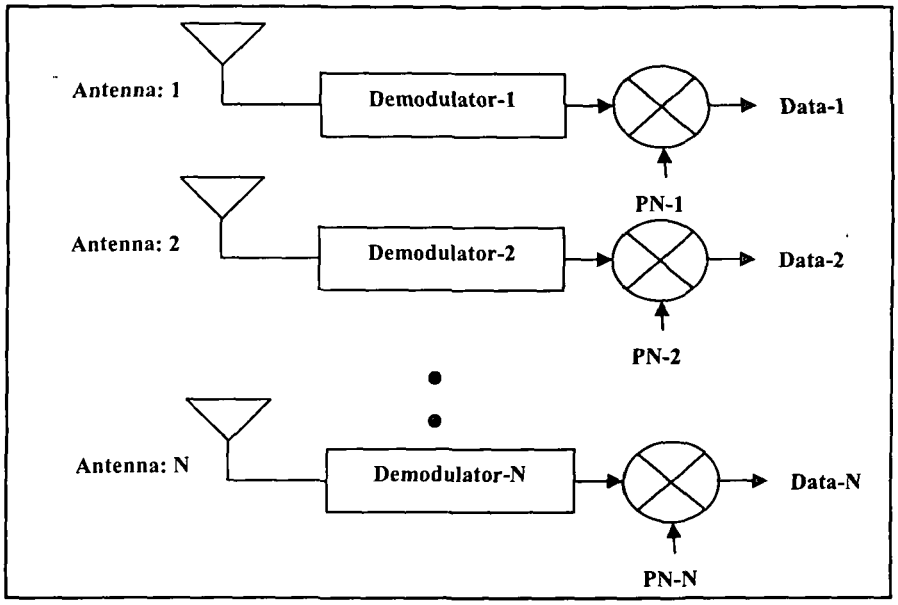

Fig.3.11: Block diagram N-channel CDMA receiver [40]

The following section reviews the works carried out by previous authors using spread spectrum technique briefly.

In [32], Stiglitz has briefly described common techniques for permitting many active subscribers to access a common channel as FDMA, TDMA, spread spectrum multiple access (SSMA) and SDMA in practice. In this paper author has addressed some issues concerning the design of a satellite system for aircraft surveillance and for air traffic control.

Kochevar [33] has investigated the spread spectrum technique for its maximum random capability experimentally. The operational characteristics were investigated with the use of two ground stations and the satellite to determine the maximum number of simultaneous users that can access a spacecraft and provide a minimum SNR of 27 dB in a 3 kHz audio channel. The result obtained from experiments have shown the feasibility of simultaneous transmission of a spread spectrum and a TV signal with acceptable quality of both signals when the spread spectrum signal is a minimum of 10 dB below that of the TV signal level.

Jung *et al.* [34] unified theoretical method for the calculation of the radio capacity of multiple access schemes of FDMA, TDMA, and CDMA for AWGN channels. Authors have highlighted that in multipath fading environment applications, the performance of CDMA is better and it has advantages over FDMA and TDMA.

Fu *et al.* [35] have determined and compared the system capacity of multi beam low earth orbit (LEO) system with CDMA and FDMA/TDMA. By considering the various parameters such as, channel fading, channel shadowing, power control, spot beam antenna gains and imperfect equalization, it was found that the capacity of CDMA is significantly reduced because of imperfect power control. They also found that because of multiple access, interference is much more severe and the CDMA system capacity is comparable to FDM/TDMA.

Cho *et al.* [36] proposed a frequency hop spread spectrum multiple access network employing M-ary orthogonal Walsh sequence keying with non coherent demodulation. The performance of proposed technique was analyzed for synchronous and asynchronous hopping under non fading and Rayleigh fading channels. The results show significant improvement in the performance with the same bandwidth as that of M-ary FSK.

Yang *et al.* [37] proposed a multiple access spread spectrum communication system using binary frequency shift keying. The bit error probability of DS-SFH SSMA using 8-ary FSK, was calculated and the results shows that the MFSK tones optimally overlapped achieves a lower BER than the conventional SSMA using non overlapping tones. Also the bit error performance improvement depends mainly on the DS spreading. The optimum frequency overlap was also determined. The approach can be used for direct sequence spread-spectrum systems with MFSK modulation to minimize the partial band jamming by optimizing the frequency tones' overlap, and the work can be extended to the analysis of multi-carrier CDMA systems, which use overlapping frequency bands.

Wang and Chao [38] considered frequency hopped spread spectrum multiple access communications employing M-ary modulation and error correction coding. In this paper major concerns were multiple access interference and network capacity in terms of number of users that can transmit simultaneously for a given level of error probability. In this author have considered FH system employing M-ary modulation. In order to mitigate the multiple access interference and increase the system capacity, error correcting codes are used such as BCH codes, RS codes. In their analysis, it was found that the larger number of users, the better the BCH code performs.

Alexantra *et al.* [39] have investigated the different detectors to increase the capacity of CDMA for multi-user applications. In that authors have focused on the optimal detectors for multi-user application and pointed out that the theoretical bases of optimal multiuser detection are well understood. Given the prohibitive complexity of optimum multiuser detectors, attention has been focused on suboptimal detectors, and the properties of these detectors are well understood by now. The next stages of investigation, involving implementation and robustness issues, are accelerating now and will lead to a determination of the practical and economic feasibility of the multiuser detector.

Kavita & Shikha [40] studied the DS-CDMA system for multi-user applications. They focused on linear multi-user detection schemes used for data demodulation with Simulation results the performance was studied in -conventional detector, de-correlating detector and MMSE (Minimum Mean Square Error) detector. It was concluded that the performance of these detectors depends on the number of paths and the length of a Gold code used.

Sandhu & Berber [41] proposed a multi-user chaotic based detector and presented results for proposed chaotic phase shift keying from simulation under AWGN. The analysis shows an improvement in the BER performance which matched with the theoretical analysis and for a BER of 10^{-3}, the improvement, compared to CSK, in Eb/No ratio is about 3.5 dB.

In [42] Wong & Leung presented the code phase multiplexed direct sequence spread spectrum signaling system, which employs parallel transmissions of several data streams modulated by different phase shifts of the same pseudo-noise code. The techniques improve the processing gain of single users and simulation results presented for performance under AWGN and single tone jammers.

3.2.4 Space Division Multiplexing and Space Division Multiple Access

Space division multiple access (SDMA) utilizes the spatial separation of the users in order to optimize the bandwidth efficiency and performance under noise. In this the radiated power of each user is controlled by space division multiplexing (SDM) using a spot beam antenna. These areas may be served by the same frequency or different frequencies. Fig-3.12 shows the basic block diagram of SDM system. However, for limited co-channel interference it is required that the cells are sufficiently separated. When using multiple antennas at the receiver as well as at transmitter, these different data streams, that are mixed-up in the air, can be recovered by SDM. The multiple-input multiple-output (MIMO) technology is a method of SDM in wireless communication system design. It uses the spatial dimension provided by the multiple antennas at the transmitter and the receiver to combat the multipath fading effect. Figure 3.13 shows the SDM system [43].

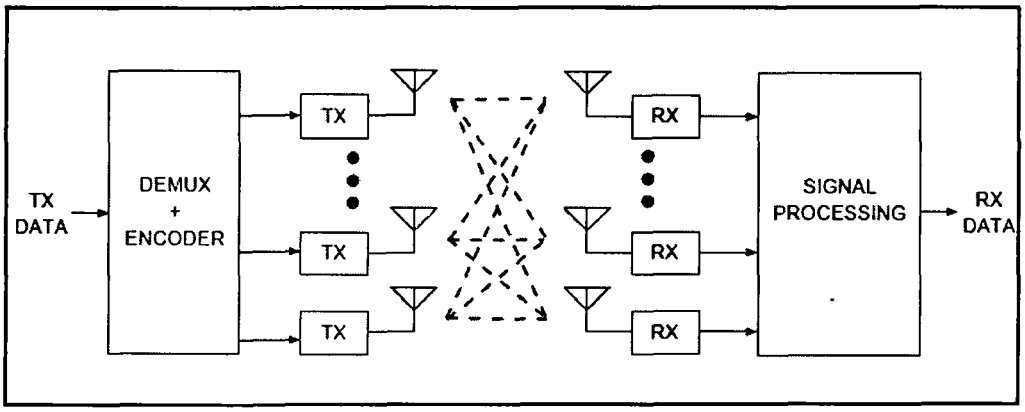

Fig.2.12: Block diagram or SDMA System [43]

SDMA utilizes the spatial separation of the users in order to optimize the use of the frequency spectrum. A primitive form of SDMA is when the same frequency is reused in different cells in a cellular wireless network. The radiated power of each user is controlled by SDMA. SDMA serves different users by using a spot beam antenna. These areas may be served by the same frequency or different frequencies. However for limited co-channel interference it is required that the cells are sufficiently separated. This limits the number of cells in a region can be divided into and hence limits the frequency re-use factor. A more advanced approach can further increase the capacity of the network. This technique would enable frequency re-use within the cell. In a practical cellular environment it is improbable to have just one transmitter fall within the receiver beam width. Therefore it becomes imperative to use other multiple access techniques in conjunction with SDMA.

The earliest idea about MIMO communication systems go back to work by A.R. Kaye and D.A. George [43] and W. van Etten [44]. Pauraj and Kailath [45] also proposed the technique of multiplexing using MIMO and US Patent was issued in 1994 with No. 5,345,599 in year 1994. In this Patent the authors have highlighted the use of proposed multiplexing technique by mitigating effect of multipath fading for wireless application with improved efficiency.

Foschini *et al.* [46] examined the exploitation of spatial dimension to improve capacities in wireless applications. In their investigation, it was concluded that there is high possibility of the capacity improvement with multi element array (MEA) technology. Further they found, the capacity scales with increasing SNR number of antenna elements at both transmitter and receiver.

Erceg *et al.* [47] presented the capacity, envelope correlation coefficient obtained from MIMO fixed wireless channel using dual polarized antennas. Experimental data indicate good channel quality and the other supporting result confirms that high capacity gains can be achieved in spatially multiplexed MIMO systems.

Dong *et al.* [48] have shown the improvement in channel capacity using antenna pattern diversity. However, the capacity is limited by the correlation of sub channels in non-ideal scattering enrolments. In this paper, the authors have investigated MIMO systems that use antennas with a dissimilar radiation pattern to introduce decorrelation hence increasing channel capacity. Further the proposed MIMO system that exploits antenna pattern diversity shows improvement over dual-polarized antenna systems. The increment in the capacity of such MIMO systems depends on the characteristics of the scattering environment.

Choi *et al.* [49] carried out the investigations lost in cellular MIMO systems and have shown that the advantage of MIMO can be lost unless extra diversity is provided. In this work the outage probability and capacity of cellular MIMO-CDMA system with spatial multiplexing has been derived. The basic reason for this loss in capacity is that linear MIMO receivers are forced to enhance some of the interference, which hurts the capacity more than multiple sub streams help it. From this analysis, the developed analytical model can be used for evaluating the performance of cell interference (OCI) reduction techniques in practical cellular MIMO systems.

Artigue *et al.* [50] have investigated the performance of downlink MIMO-CDMA receivers based on a chip rate equalizer followed by dispreading. The behavior of the SINR provided by the receiver is first studied when the spreading factor and the number of users per antenna converge to $+\infty$ at the same rate. It was shown that the SINR converges towards a simple expression depending on the particular realization of the frequency selective channel between the base station and the mobile of interest. In order to get more insights on the long term performance, the ergodic sum-capacity delivered by the system was evaluated in the large number of antennas regime in the case the impulse response taps of the channel are Gaussian random matrices. A simple expression is obtained. It appears to be quite reliable for realistic number of antennas, and is discussed in order to get some insights on the overall performance.

Zelst *et al.* [51] have proposed new maximum likelihood decoding (MLD) technique. This MLD technique provides superior SNR performance compared to other SDM techniques. Further to improve the efficiency and capacity with more robust against inter symbol error (ISI) the system is applied to the OFDM.

Akhilesh *et al.* [52] have analyzed the channel capacity improvement with MIMO. In this paper the authors have emphasized on fine compromise between rate maximization and diversity solution, including the ability to adapt to the time changing nature of the wireless channel using some form of feedback.

Muhammad Farooq *et al.* [53] have presented the study of some future generations which are under research like 5G, 6G, and 7G. Authors have discussed the existing and future wireless mobile communication generations. Edge will contribute to a bright future for 3G and onwards generations, a vision shared by major analyst and industry groups. Satellite network will be used from 6G mobile communication systems and onwards.

Jayesh Dabi & Kamlesh Gupta [54] have designed multiple–antenna wireless systems that exploit the space modulation (SM) concept and analyzed Orthogonal Space–Time Block Codes (OSTBC). It provides advantage of SM-OSTBC technologies to design transmit–diversity and high–rate modulation schemes by providing high multiplexing gain.

Marco Di Renzo *et al.* [55] have summarized recent research achievements and open research issues of a novel transmission technology named SM. SM combines digital modulation, coding, and multiple–antenna transmission in a unique fashion, and exploits the location–specific property of the wireless channel for communication. This enables the position of each transmit–antenna in the antenna–array to be used as an additional dimension for conveying information. Recent results have indicated that SM can be a promising candidate for low–complexity MIMO implementations. However,

SM is still a young–born research field and several issues need to be addressed to fully understand its potential and limitations in practical and realistic propagation environments.

3.2.5 Comparison between TDM, FDM, CDM and SDM

Since the origin of electronic communication many multiplexing techniques are evolved to transfer data of many users on a single channel. Each technique has its advantage and limitations. Table 3.1shows the comparison between them.

Table: 3.1 Performance Comparison of Multiplexing Techniques

Quantity	TDM	FDM	CDM	SDM
Bandwidth	Low	High	Very High	Very High
Channel Capacity	Low	Low	Very High	Very High
Spectral Efficiency	Low	Low	Very High	Very High
Data Transfer Rate	Medium	Medium	Medium but with CPSK it is high	High
Implementation	Simple	Simple	Complex	Very Complex
Multiuser on same Frequency band	Not possible	Not possible	Possible	Possible
Noise Immunity	Not free	Not free	Better but degraded for more users due to MAI	Noise immunity is poor

Table: 3.2 previous works on Multiple-excess Techniques

Author	Multiple access Technique	No of Channel/ users	Modulation	BER / SER/ Noise Margin /ISI performance	Applications
Yang et.al [37]	SSMA	10-100	MFSK	BER for SNR ~ 15 dB and no of user =10 is 10^{-3} BER for SNR ~ 9 dB dB and No of user =100 is 10^{-1}	Spread spectrum wireless communication
Goodall [7]	PCM	Single	PAM	--	4KHz Speech Coding
Suguri *et al.* [14]	TDMA/PCM	244	BPSK	BER for SNR ~ 10 dB is 10^{-5}	Satellite communication 6/4GHz
Krister raith *etal.* [15]	TDMA	833 with Analog FM, 1000 with GSM	Digital	BER ~ 0.015 for C/I 18dB	Analog FM/GSM mobile applications.
Vitalice et al. [23]	TDMA	---	Digital QPSK	SER ~ 10^{-5}	Satellite communication for TDMA.
Wang, *et al.*[38]	FHMA	10	4-FSK	----	Satellite phone, Multiple Access Communication
Yu. W *et al.* [24]	FDMA	32	QAM	----	FDMA-capacity region problem for a Gaussian MAC with ISI.
Choi W. *et al.* [49]	MIMO CDMA	---	Digital	Higher processing gain of 786 as compare to SISO gain of 64	Outage probability and capacity of cellular MIMO-CDMA systems with spatial multiplexing. and linear receivers has been derived.
Artigue *et al.* [50]	MIMO CDMA	----	Digital	Ergodic-Sum-Capacity increases transmit antennas	MIMO systems are studied to improve the performance and capacity of CDMA systems.

Akhilesh *et al.* [52]	MIMO/CDMA	---	Digital	At SNR 50 the capacity improved from 7.5 Bits/Hz with MIMO as compared 5.5 Bits/Hz with SISO.	Channel Capacity Enhancement of Wireless Communication using MIMO Technology.
Alexandra *et al.* [39]	Multi-user CDMA	--	Digital	With processing gain of 31 and 16 users, the users interference cancellation scheme provides a improvement in the BER from 0.075 to $0.5x10^{-2}$	CDMA for mobile communication.
Kavita *et al* . [40]	Multi-user CDMA	15	Digital	With Decorrelating detector BER is improved 0.01 in compare to conventional detector at 10 dB SNR	Commercial Application
Sandhu *et al* [41]	Multi-user CDMA	--	Digital	CPSK system provides better BER by 10^{-3} at 3.5dB SNR BER in compare to CSK system	Personal communications services.
Wong *et al.* [42]	Single user CDMA	4	M-ary DSSS	At 10 dB SNR provides $0.5x10^{-3}$ BER for single tone jammer ISR 50dB	Commercial applications

Table-3.2 shows previously reported works [15], [23], [24], [37], [38], [39], [41], [49], [52] related to multiple access wireless communication with no of channels BER/ SER / Noise margin performances. Most of the works on multiple accesses are based on TDMA, FDMA or CDMA. It is seen that BER performance with AWGN is greater than 10^{-3} for most of the work [40], [15], [39], [42]. To improve the spectral efficiency to accommodate more number of users the CDMA multiplexing technique has been reported which is the back bone of present and future wireless communication. But conventional CDMA also has its limitation. As the number of users increases, they interfere with each other and add to the channel interference. Therefore, it is seen that

CDMA technique does not perform well on multi user/Jamming/Intentional interference. However, for data communications application, BER is required to be less than and equal to 10^{-4}. So it is needed to use the techniques for multiple accesses which can perform well under jamming/AWGN/intentional interference for wireless communication applications. It is also seen from the table that for most of the work on direst sequence spread spectrum (DSSS) and frequency hopping spread spectrum (FHSS) are based on single channel as those techniques are not perform well in wireless communication with a number of channel/users are more than one. So it's required to use DSSS and FHSS for multi user services. In this thesis we have studied both DSSS and FHSS techniques for multi channel/ multi user applications

3.3 Binary Phase Shift Keying Demodulator

Phase shift keying (PSK) is a digital modulation scheme that conveys data by changing the phase of the carrier wave. PSK uses a finite number of phases; each of them conveying a unique pattern of binary bits. Binary phase shift keying (BPSK) is the simplest form of PSK which uses two phases that are separated by 180°. It is one of the simplest techniques for digital modulation and provides the best performance in terms of BER. The demodulator demodulates the modulated carrier and recovers the transmitted data. In literature many techniques are proposed for demodulation of BPSK signal. The succeeding section surveys some works presented by previous authors on BPSK demodulation.

In [56], Riter has realized and discussed an optimum receiver structure for estimating a phase reference from the PSK signal itself. It is shown that at low signal-to-noise ratios, the optimum detector can be realized with a Costas loop. Since a Costas loop and squaring loop exhibit identical performance, it follows that either of these simple devices give optimum performance for low-input SNR.

Villegas *et al.* [57] have presented a new method for conversion of BPSK signals into amplitude shift keying signals. The basic principles of the conversion method are the

super harmonic injection and locking of oscillator circuits, and interference phenomena. The first one is used to synchronize the oscillators, while the second is used to generate an amplitude interference pattern that reproduces the original phase modulation. When combined with an envelope detector, the proposed converter circuit allows the coherent demodulation of BPSK signals without the need of any explicit carrier recovery system.

Wu *et al.* [58] have proposed new low power BPSK demodulator for internal module of a wireless implantable neural recording system. The proposed circuit was verified by the measurement results obtained from the circuit board comprises of RC phase shift, Shimite-Trigger XOR gate. The measured results demonstrate that the proposed circuit can demodulate the input signal correctly.

Asgarian *et al.* [59] have presented non coherent BPSK demodulator for wirelessly powered biomedical implants. The circuit is very simple and consumes ultra low power. It can detect the high rate signal as data rate to carrier frequency ratio of 100%. The circuit is designed and simulated in a 0.18μm CMOS technology and tested experimentally.

An ultra-low power BPSK demodulator based on injection locked oscillators was demonstrated by Zhu *et al.* [60]. The BPSK is first converted to ASK signal, which is then demodulated by an envelope detector. The prototype chip is fabricated in a 65 NM CMOS technology and consumes 228μwatt power. Theoretically calculated BER performance verified with the measured results and found to be very close to the predicted value.

Young *et al.* [61] have proposed BPSK demodulation technique using CMOS. The method compares absolute values of in-phase and quadrature-phase signals to select the larger one to be converted to a digital value. A simple double-balanced mixer and an efficient absolute current comparison block are proposed and implemented with 0.18 μm CMOS technology. The generation of quadrature signal from the VCO output is not discussed when the input frequency is changing. This limits the performance of this demodulator.

Zheng & Saavedra [62] has presented a novel anti-parallel loop carrier synchronization method for BPSK demodulation. In the proposed circuit D.C. offsets are introduced using two voltage summers and they play important role for the operation of this anti-parallel loop. Moreover, there are two switches at the VCO input and a control circuit: a comparator and an inverter. The switches and D.C. off sets limits speed and further complicates the circuit. This results in poor bit error rate (BER) performance.

3.4 Sinusoidal Frequency to Voltage Converter

Kiranon *et al.* [63] have presented an FVC with theoretically zero output ripples. It has a simpler structure and four times faster response than an earlier system reported. Moreover, it may easily be modified to a switched-capacitor version, if so desired can be adjusted by the capacitance ratio together with a reference voltage.

Cohen *et al.* [64] has described an FVC that can be used in a voltage-controlled oscillator with a 100-kHz central frequency, varying within an octave on either side. Accuracy of 0.01 percent and better is secured by determining the pulse width by an exact digital system and determining the pulse height by switching an exact current source. The FVC was tested in the frequency range of 50 KHz to 200KHz and provide a linear output of 1 volt to 4 volt and response time of 200 μ Seconds.

Surakampontorn *et al.* [65] have introduced a sinusoidal FVC based on the nonlinear analog circuits. The realization is composed of a differentiator, an integrator, and a translinear divider and square rooter circuit. The proposed F/V converter can accurately and linearly convert a sinusoidal signal frequency into an output voltage, with fast response and low error, over more than two decades of frequency range. The performance of the FVC for the frequency range from 50 Hz to 5 kHz has been tested experimentally.

Das *et al.*[66] have investigated transconductance amplifier (OTA) based sinusoidal FVC. The proposed FVC can linearly convert low voltage signals which are not

possible with commercial converter ICs such as LM2917. This converter is based on an OTA based differentiator and an OTA based half wave rectifier. The circuit provides linear output for input frequency of 200 Hz to 10 KHz.

Lorsawatsiri *et al.* [67] have presented a new method of sinusoidal FVC using differentiator, RMS-DC converters and divider. The performance of the circuit is evaluated by computer simulation and results obtained are in a good match with the theoretical values. The simulations were carried out from a frequency of 100 Hz to 10 KHz.

Apart from the surveyed literature, there are many commercially available sinusoidal FVCs in the form of ready to use integrated circuits. Some of such devices are discussed here. Integrated circuit LM2907/2917 from Texas Instruments [68] provides FVC conversion with a high gain operational amplifier designed to operate a relay, lamp or other load. The output voltage from the converter is obtained from the expression as:

$$V_{out} = f_{in} \times V_{cc} \times R_1 \times C_1 \qquad (3.1)$$

There are some limitations on the choice of R_1 and C_1 which should be considered for optimum performance. The timing capacitor also provides internal compensation for the charge pump and should be kept larger than 500pF for very accurate operation. Similarly, several considerations must be met when choosing R_1. If R_1 is too large, it can become a significant fraction of the output impedance and it will degrade linearity. It provides linear output from 1 KHz to 10 KHz only.

Integrated circuit VFC32 also provides FVC function. It operates on a principle of charge balance [68]. R_1 sets the input voltage range and for a full scale input, a 40 KΩ input resistor is recommended. Other input voltage ranges can be achieved by changing the value of R_1 as follows [68]:

$$R_1 = \frac{V_{FS}}{0.25mAmps} \qquad (3.2)$$

R_1 should be a metal film type for good stability and manufacturing tolerances can produce approximately ± 10% variation in the output. In the circuit if C_2 value is made too low, the integrator output voltage can exceed its linear output swing, resulting in a nonlinear response. This integrated circuit provides linear output from 1 KHz to 200 KHz only.

Integrated circuit AD/650 [68] also provides high frequency FVC operation with low non- linearity in comparison to other commercially available circuits [63]. Also above 500 KHz frequency an additional 3.6 KΩ pull down resistor from Pin 1 to –Vs is required. The additional current drawn through the pull-down resistor reduces the operational amplifier output impedance and improves its transient response. However, its higher operating range is limited to 1 MHz only and above this frequency of operation non linearity is resulted in the output voltage.

Integrated circuit TC9400/9401/9402 [68] also provides both VFC and FVC function. These devices are low cost and utilize low power CMOS technology [65]. But their range of operation is very low and provides linear output from 10 KHz to 100 KHz only.

Table: 3.3 Comparison of different FVC

Quantity	[59]	[60]	[61]	[62]
Maximum Operating frequency	100KHz	5KHz	10KHz	10KHz
Linearity	Good	Good	Good	Good
Response Time	High	Low	Low	Low
Ripple	Medium	Low	Low	High
Bandwidth	Low	Low	Low	Low

Table 3.3 gives the comparative analysis of work reported by authors on FVC. It is seen from the table and surveyed commercial integrated circuits that the most of the work on sinusoidal FVC has a lower frequency range of conversion (maximum up to 100 kHz),

higher response time and lower linearity of conversion. These approaches fail to work when operating in frequency more than 100 kHz due to limitation of noises of integrator/differentiator of these FVC circuits. These reported FVC are unsuitable for signal processing in communication systems where bandwidth is in MHz range.

3.5 Growth of Wireless Users

The last few years have witnessed a phenomenal growth in the wireless industry, both in terms of mobile technology and its subscribers [69]-[70]. There has been a clear shift from fixed to mobile cellular telephony, since the last decade of the century as depicted in Figure 3.13, in Japan. By the end of 2010, there were over four times more mobile cellular subscriptions than fixed telephone lines [69].

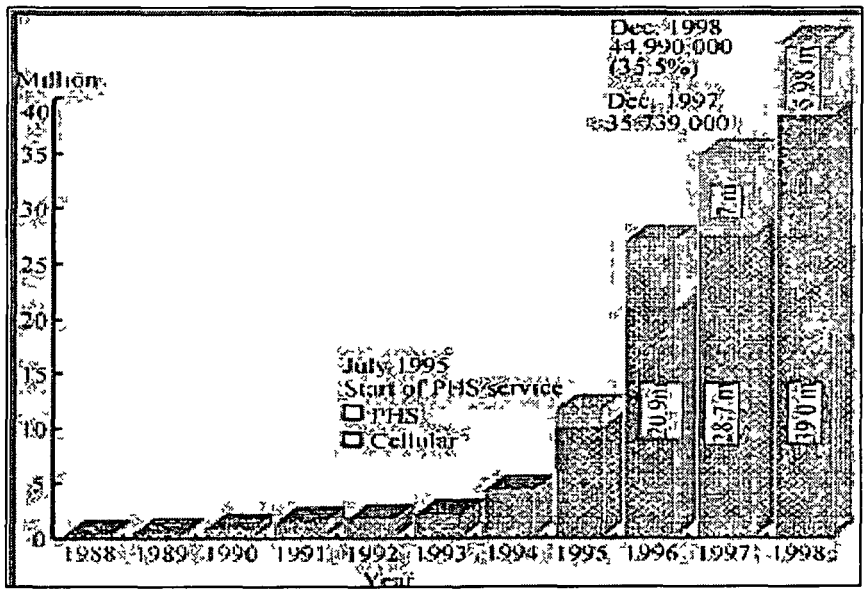

Fig.3.13: Growth of mobile users in Japan [64]

Similar rapid growth rates in mobile users are evident all over the world wide. People want to communicate with people not with the place. Both the mobile network

operators and vendors have felt the importance of efficient networks with equally efficient design.

Service providers are experiencing growing demand for access bandwidth as standard definition broadcasting continues to evolve to high definition, more people are online at once and internet becomes preferred delivery mechanism for entertainment and a full multimedia experience. Market expectation for fixed access bandwidth growth is almost doubling every 2-3 years but customers are resistant to expected cost increases. Services revenue growth requires in addition to continued infrastructure cost savings to balance forecast demand. The demand for wireless communications is rapidly growing and CDMA technology promises to be a key technique for achieving the high data capacity and spectral efficiency requirements for wireless communication systems of the near future [71]. During the last few decades, mobile communication has developed rapidly. The increasing dependency of people on telecommunication resources is pushing even more current technological developments in the mobile world [72]-[74].

3.6 Conclusion

In this chapter, an overview of the existing works related to multiplexing and signals processing using BPSK demodulator and sinusoidal FVC related to the problem addressed has been provided. The capacity and spectral efficiency of initially developed systems were low. Poor technology was the main hindrance. Later with the development of integrated circuit technology and processor controlled digital switching system, the efficiency and capacity [10]-[12], [17] of TDMA was improved. FDMA is implemented with narrow band but each band (channel) is shared by each user separately. In search of high speed, fast data rate capacity and good quality of service, the evolution of mobile generation reached to 3rd generation mobile communication system. Further, as the numbers of users increases, the bandwidth increases. This has further demanded improvement in the channel capacity and performance of the existing systems. Both, TDMA and FDMA are used in mobile/satellite communications [12]-[16], [23]-[26]

efficiently. It also suffers from the adjacent channel interference. In contrast to TDMA/FDMA, CDMA provides better bandwidth efficiency and channel capacity [35]-[42]. They have hard limits on the user capacity while the performance of CDMA systems degrade gradually as the number of users increases due to multiple access interference (MAI) and jamming. The SDMA can be integrated with CDMA/TDMA/FDMA to increase data speed but with single users [46]-[50].

The tremendous growth in wireless users and huge increment in the mobile subscription has made the attention of researchers and industries to move to the next generation of mobile wireless technology. The main aim of next generation mobile technology is to provide high speed, high quality, high capacity and low cost services. The slogan to be connected from anywhere to anywhere have further, attracted the attention of researchers. The main aim of next generation technology is to provide high speed, high quality, high capacity and low cost services for example voice, multimedia and internet. The growth of wireless users over the wired users and type of service has worried the service provider for more bandwidth and technological advancement.

In technological advancement, the signal processing has played very crucial role in the design of various systems high speed and improved system. There is at present a worldwide effort to develop next-generation wireless communication systems. It is envisioned that many of the future wireless systems will incorporate considerable signal-processing intelligence in order to provide advanced services such as multimedia transmission. In general, wireless channels can be very hostile media through which to communicate, due to substantial physical impediments, primarily radio- frequency interference and time-varying nature of the channel. The need of providing universal wireless access at high data-rate presents a major technical challenge, and meeting this challenge necessitates the development of advanced signal processing techniques for multiple-access communications in non-stationary interference-rich environments.

Therefore, this research aims at developing multiplexing technique using DSSS and FHSS spread spectrum for channel capacity/spectral efficiency improvement of the

existing capacity. We have also tried to improve the performance under AWGN/jamming using proposed signal processing techniques.

Chapters 4, 5, 6 and 7 are concentrated on the design of proposed multi-channel DSSS and FHSS systems for a multiplexing number of users on a single channel and the proposed signal processing techniques to improve the performance of designed systems.

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Chapter 4

Design and Simulation of CPSK based Multi-Channel Direct Sequence Spread Spectrum System

4.1 Introduction

As seen in Chapter-2 and 3, the spread spectrum has tackled many issues of wireless communication such as communication privacy, jamming for defense application, intentional interference due to multi users, multipath fading etc [1]-[3]. Code Division Multiple Access (CDMA) [4-5], a direct sequence spread spectrum (DSSS) technique, has emerged as an alternative to the global system for mobile (GSM) cellular architecture. Though it has an interference suppression capability, as number of user increases, the multiple access interference generated results in performance degradation. Recently, the code phase shift keying (CPSK) based DSSS technique [6]–[9] has gained popularity for high data rate transfer capability providing services to a single user with signal security and privacy. To improve further capacity and spectral efficiency of DSSS by coding many users with single pseudorandom noise (PN) sequence, a multiplexing technique with DSSS has been proposed. This chapter discusses the design and simulation of multi-channel DSSS system for accommodating more number of users.

This chapter is structured as follows. Section 4.2 describes the architecture of proposed multi-channel transceiver based on CPSK/DSSS. The design and simulation of the transmitter and receiver are introduced in Section 4.3 and Section 4.4. The BPSK demodulator provides very good noise immunity and frequently used for better bit error performance. Section 4.4.2 shows the design of the proposed BPSK demodulator. Finally, Section 4.5 provides conclusion of the chapter.

4.2 Architecture of Proposed CPSK based Multi-channel Direct Sequence Spread Spectrum System

In this section the architecture of proposed CPSK based transceiver has been discussed for multi-channel communications. Section 4.2.1 explains the working principle of proposed DSSS transmitter for a multiplexing K number of channels for a K number of users.

4.2.1 CPSK Based DSSS Transmitter

The CPSK based DSSS transmitter consists of a PN sequence coder with PN sequence generator, bi-level shifter, and multiplier and power amplifier. Figure 4.1 shows the architecture of the proposed CPSK based DSSS transmitter.

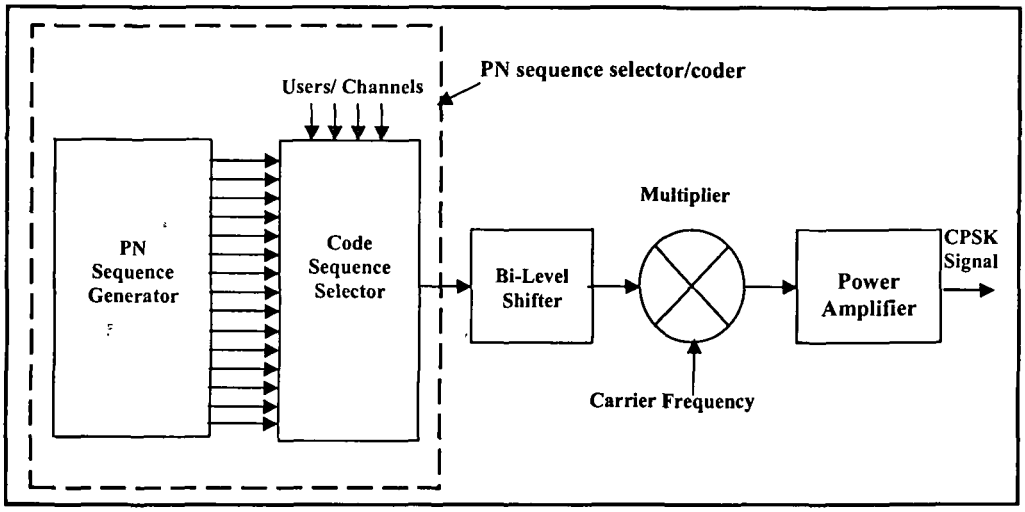


Fig.4.1: Architecture of CPSK based DSSS transmitter

The CPSK module groups the input data into K bit data word ($K = Log_2 M$), and represented by an integer m, $0 < m < M-1$. This K-bit data is composed by taking one bit from each user and have total 2^K symbols. Each symbol selects one of $M = 2^K$ PN code, each with duration T generated by a PN generating circuit. A PN waveform with length N (N is the spreading factor, and N>>K) chips is selected from signaling waveform 2^K sets. If chip duration is T_C, then symbol duration is expressed as: $T = N \times T_C$ [10]-[17]. These selected PN sequences represent the coded PN signaling waveforms which modulate the carrier signal with BPSK modulation scheme and generates CPSK, DSSS signal as expressed by Equation (4.1) [18]-[22].

$$s_m(t) = \sqrt{\frac{2E_s}{T}} p_m(t) Sin(2\pi f_c t) \qquad (4.1)$$

Where m=1, 2, 3.....M. $M = 2^K$ and K=total number of channels for CPSK DSSS system; $p_m(t) = p(t - m_c T_c)$; $m_c = {m(L+1)}/{M}$; T_C=chip duration; L= length of PN sequence; T=symbol period and E_s = signal power.

In this fashion, out of 2^K PN sequences, one PN code is selected by multiplexing (coding) K users with it.

4.2.2 CPSK based DSSS Receiver

Figure 4.2: shows the block diagram of K-channel CPSK based DSSS receiver, which consists of binary phase shift keying (BPSK) demodulator, PN sequence generator, correlator, integrator, dump, comparator and decoder [18].

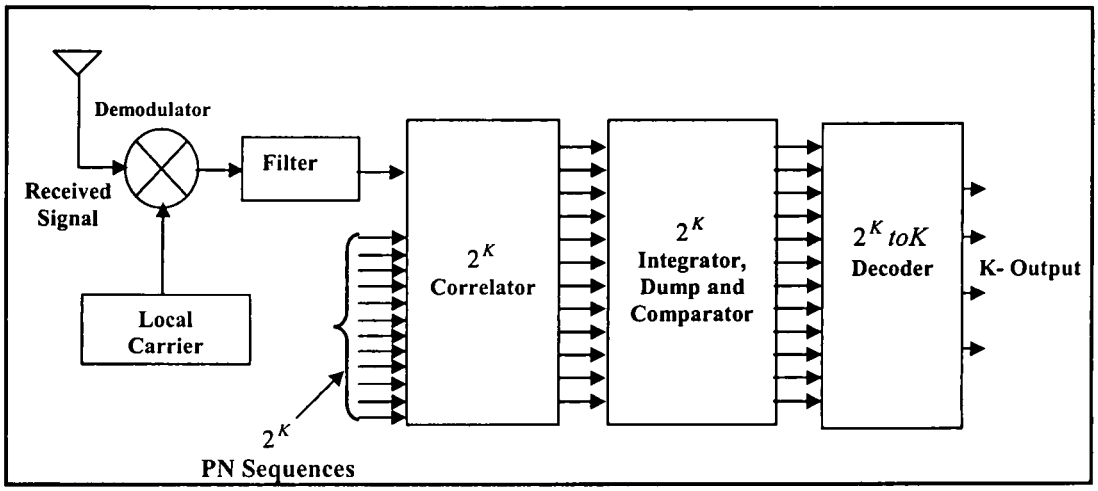


Fig.4.2: Architecture of CPSK based DSSS receiver

The received signal is first demodulated using coherent demodulator and then filtered with a low pass filter (LPF). Now, the receiver's task is to identify which PN sequence, out of 2^K PN sequences, is received. It is accomplished using two input EX-NOR gate working as a correlator circuit. Therefore, the received PN sequence is correlated with 2^K EX-OR gates. The output of 2^K EX-OR gates, only one gate will give high output for one PN duration. The outputs of all 2^K correlators are applied to integrate and dump circuits. Integrate and dump circuits integrate the output signal of each correlator and

dump to zero before the next PN sequence is received. Only one integrator circuit will have high output in compare to other circuits. The output of each integrator is compared in comparator circuit with fixed reference level. At a time one comparator will give high output which matches with the local PN sequence completely. The output of the comparator is applied to 2^K to K decoders. Finally, 2^K outputs obtained form comparators are decoded into K bits word as transmitted by the CPSK based DSSS transmitter for multiplexing K users.

4.3 CPSK based DSSS Transmitter Design

As discussed above the proposed CPSK based DSSS system has been discussed for multi-channeling. K-users are multiplexed on single frequency using 2^K PN sequences. To show the proof of technique and keeping in view the complexity of circuit, we have designed the proposed system for 4 users (K= 4), only. Further, this Chapter concentrates on the design and simulation of proposed CPSK based transmitter for 4-users only. The different stages of the transmitter are studied with block diagram, circuit diagram and simulated waveforms. The waveforms obtained from simulation are presented here.

4.3.1 Pseudorandom Noise Sequence Generator

Pseudorandom Noise, sequences is the essential component of a spread spectrum system. Spread spectrum communication has two characteristics first one is the bandwidth of the signal transmission is much larger than the bandwidth of the original information signal and the second is that the transmission signal bandwidth is decided by the spreading codes [16] (PN sequences). In this design, we have used, LFSR to generate required PN sequences [23].

In LFSR contents of the each registers are shifted right by one position with each clock cycle. The feedback from predetermined registers or taps to the left most registers are XOR-rd together and fed back to the first shift register as shown in Figure 4.3. A n-bit shift registers which pseudo-randomly scrolls between 2^N-1 values and once it

reaches its final state, it will traverse the sequence exactly as before. A maximum length sequence (L) for an LFSR shift register of length N is referred to as m-sequence [12]-[17] and is defined as: $L = 2^N - 1$.

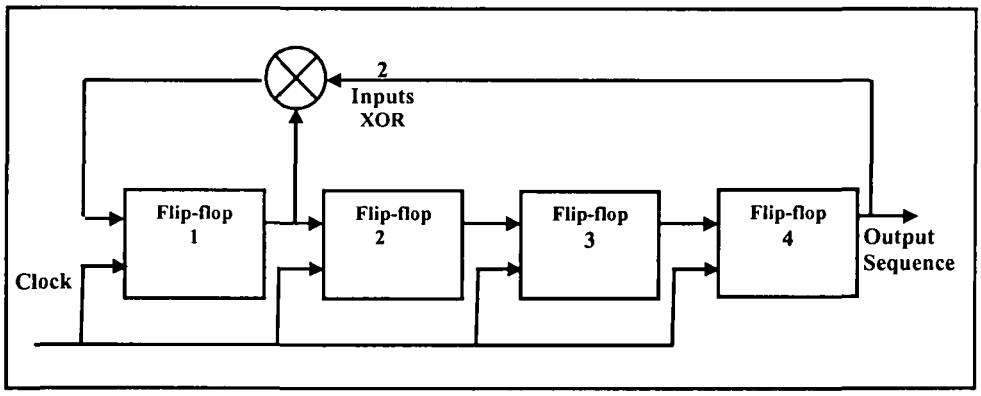


Fig.4.3: Block diagram of LFSR PN generator [10]

As discussed above the proposed CPSK based DSSS system is designed for 4-channels/users; therefore it requires total 2^N PN sequences to represents 4 bit data word. But 0000 states can be decoded with total $2^N - 1$ PN sequences only. Therefore, we have used $2^N - 1$ PN sequences in the design of 4-channels/users system. The data word "0000" will be decoded automatically in the decoder of demodulator.

In the PN sequence generator, the shift registers should be seeded to a non-zero value. All-zero's state is called the lock-up state and will not generate any PN sequence. In this state all the shift registers will be hanged for '0' states and therefore, at least one must be set to non-zero state. We have set the shift register to '1', and remaining 3-flip flops to '0' with set /preset controls by generating sharp pulse using the series R-C circuit as shown in the Figure 4.4.

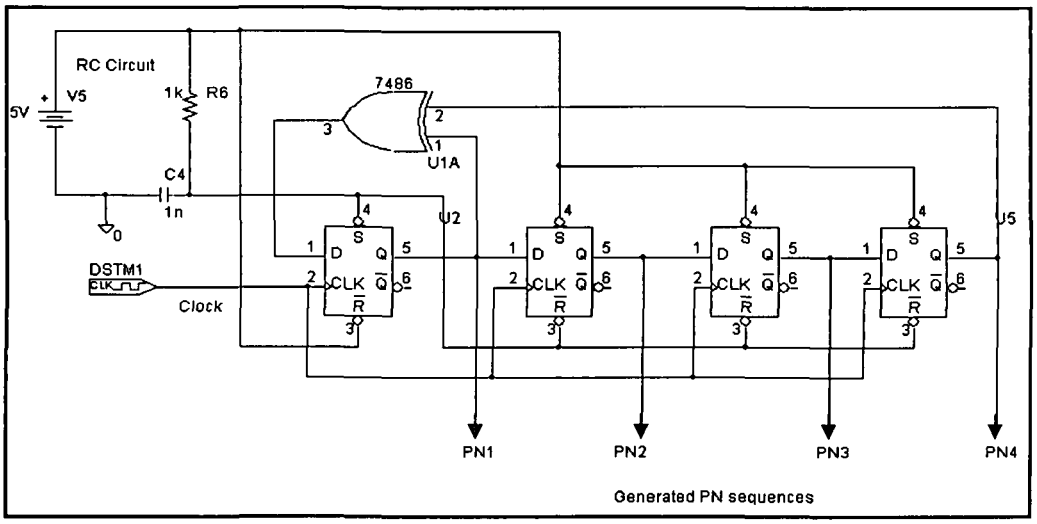


Fig.4.4: Simulated circuit diagram of PN sequence generator

To keep required components to a minimum, in this design we have taken minimum required PN sequence to accommodate total 4-channels. The output of a PN sequence generator repeats after $2^N - 1$ pulses where N flopshe number of flip flop. Higher the number of flip flops longer will be the PN sequence. As discussed above to keep the number of components to a minimum we have generated the PN sequence of smaller duration.

We have designed the CPSK based DSSS system to operate at 100 MHz channel frequency. The clock frequency to generate required PN sequences is used as 250 KHz with 50 percent duty cycle. With this specification, chip duration will be of $4\mu Sec\,(T_{ON} + T_{OFF})$. There are total four D Flip flops, in the PN generator circuit; the each PN generated sequence will repeat after 2^N-1=15 clocks. Therefore, one generated PN sequence will have 15 chips, with each chip of $4\mu Sec$, each PN sequence will have $(15\times 4) = 60\mu$ second duration. Figure 4.5 shows the simulated waveform obtained with Microsim Software Version 8.0. It shows four PN sequences and one clock of 250 KHz. The other waveform is obtained from the RC circuit and applied to set/preset controls of D-Flip flop for presetting to '1000' as an initial state.

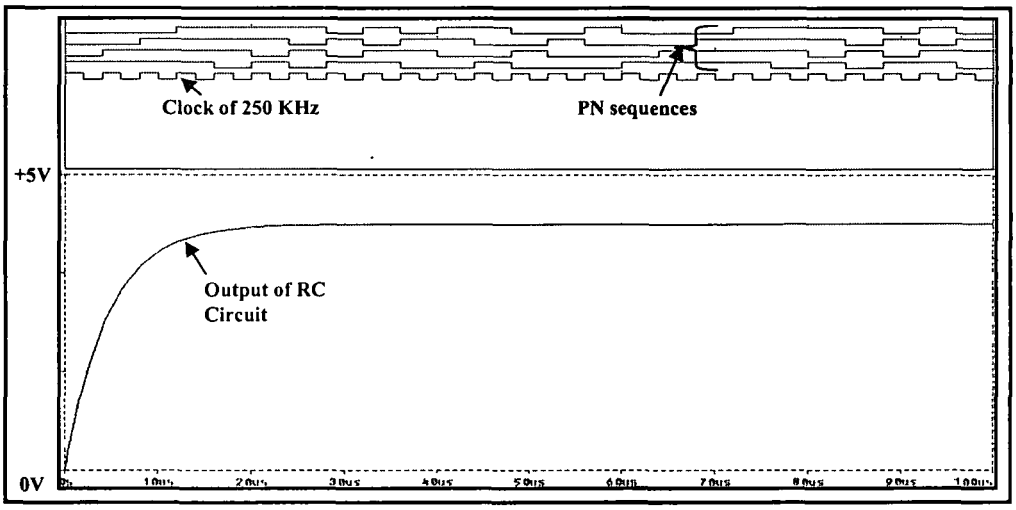


Fig.4.5: Simulated output of PN sequence generator

The PN sequence obtained at the output of the first D-flip flop in the PN generator circuit is **1 1 1 1 0 1 0 1 1 0 0 1 0 0 0.** This circuit generates total four PN sequences, each obtained at the output of flip flop. All PN sequences are of the same duration of 60 μ seconds and contain 15 chips. The number of ones and zeros in each PN sequence are same but phase shifted. Also the total numbers of ones in each PN sequence are more than the total number of zeros as discussed in the Chapter 2. It is seen from the table that in each PN sequence, the numbers of '1's and '0's differ only by one, i.e. the number of '1's is just one more than the number of '0's. Therefore, in each PN sequence out of 15 chips number of '1' are 8. The number of '0' in each sequence is 7 there are a number of '1' as 8 and the number of '0's as 7 as shown in Figure 4.5.

The total numbers of digit one ('1') are one more than that of the total number of zero ('0') in one PN sequence. Therefore, in each PN sequence there are 8 one and 7 zeros. The circuit diagram shown in Figure 4.5 has been simulated using integrated circuits SN7474 for D-flip flop and SN 7486 for the Ex - OR gate [24].

Table: 4.1 Output of PN sequence generator

Clock Pulses	Flip flop (1)	Flip flop (2)	Flip flop (3)	Flip flop (4)
Initial state	1	0	0	0
1	1	1	0	0
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	1	0	1	1
6	0	1	0	1
7	1	0	1	0
8	1	1	0	1
9	0	1	1	0
10	0	0	1	1
11	1	0	0	1
12	0	1	0	0
13	0	0	1	0
14	0	0	0	1
15	1	0	0	0

Table: 4.1 shows different PN sequences generated by the PN sequence generating circuit. These sequences are available at the Q output pin of each flop flops. The first PN sequence **1 1 1 1 0 1 0 1 1 0 0 1 0 0 0** obtained at the output of the first flip flop is used to generate 15 PN sequences using shift registers discussed in the Section 4.3.2.

4.3.2 Shift Register

To obtain more number of PN sequences from one PN sequence, a shift resister is used as shown. Table 4.2 shows these 15 PN sequences obtained using shift registers as discussed below.

Table-4.2: 15 PN sequences obtained from shift registers

Clock	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
Initial state	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**1**
1	1	0	0	0	1	0	0	1	1	0	0	0	1	1	1
2	1	1	0	0	0	1	0	0	1	1	0	0	0	1	1
3	1	1	1	0	0	0	1	0	0	1	1	0	0	0	1
4	1	1	1	1	0	0	0	1	0	0	1	1	0	0	0
5	0	1	1	1	1	0	0	0	1	0	0	1	1	0	0
6	1	0	1	1	1	1	0	0	0	1	0	0	1	1	0
7	0	1	0	1	1	1	1	0	0	0	1	0	0	1	1
8	1	0	1	0	1	1	1	1	0	0	0	1	0	0	1
9	1	1	0	1	0	1	1	1	1	0	0	0	1	0	0
10	0	1	1	0	1	0	1	1	1	1	0	0	0	1	0
11	0	0	1	1	0	1	0	1	1	1	1	0	0	0	1
12	1	0	0	1	1	0	1	0	1	1	1	1	0	0	0
13	0	1	0	0	1	1	0	1	0	1	1	1	1	0	0
14	0	0	1	0	0	1	1	0	1	0	1	1	1	1	0
15	0	0	0	1	0	0	1	1	0	1	0	1	1	1	1

Figure 4.6 shows the P-Spice simulated circuit diagram of shift register using integrated circuit SN7474 [24]. It consists of $2^4 - 1 = 15$ flip flops connected in SIPO configuration [17]. This circuit generates 15 PN sequences with the help of one PN sequence obtained from the PN sequence generator circuit shown in Figure 4.5. The clock and set/reset pulses used for initializing all the flips are also obtained from the PN sequence generating circuit. Before applying the PN sequence from which 15 PN sequences are generated, all the flip-flops used in the shift register are initialized to the one of the PN sequence using preset/clear controls.

We have initialized all the 15 flips flops of the shift register circuit as per reverse order of first PN sequence **1 1 1 1 0 1 0 1 1 0 0 1 0 0 0** which is used for generating 15 PN sequences. Therefore, by applying reset pulse to set/reset control pins of each flip flops used in the shift register in such a way that all flip flop are initialized as **0 0 0 1 0 0 1 1 0 1 0 1 1 1 1** as shown in Table : 4.2.

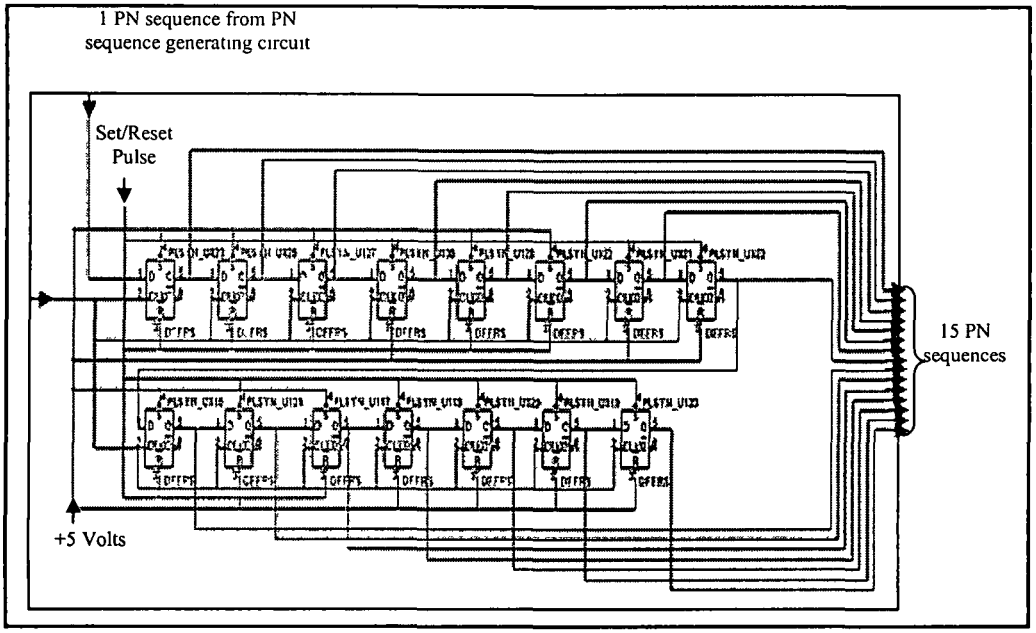


Fig.4.6:P-Simulated circuit diagram of shift register

Figure 4 6 shows the software simulated circuit diagram. The 15 PN sequences obtained from the simulated circuit are shown in Figure 4.7.

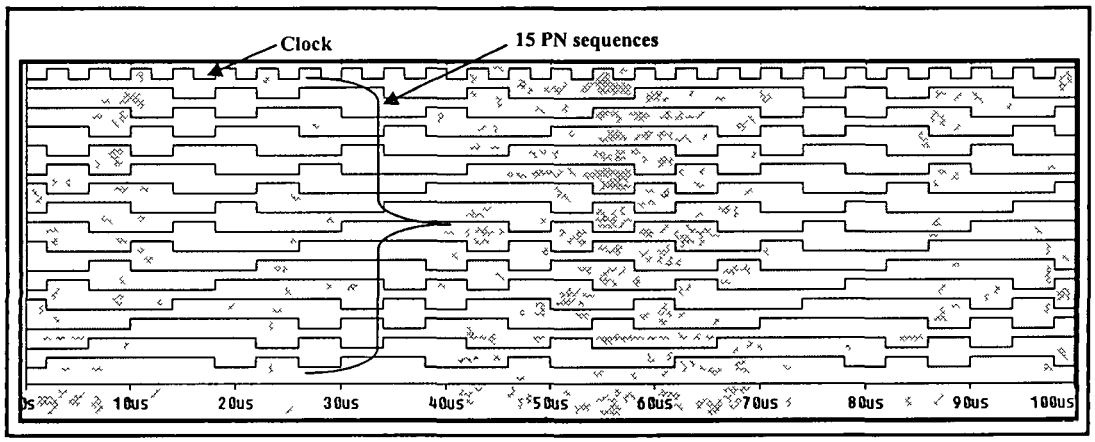


Fig.4.7: Simulated 15 PN sequences by shift register

4.3.3 Data Word Generator

The data word generator circuit is used to generate a 4-bit word which represents the number of users/channels for implementing the CPSK technique as a method of

multiplexing/accommodating 4-users on the same channel with DSSS. It generates a data word of 4-bit width with total $2^4 = 16$ symbols.

To represent 4-users/channels we have generated 4-bit binary data word with the help of 4-JK flip-flops with Serial-in Parallel-Out (SIPO) [23] configuration, as shown in Figure 4.8. The outputs Q1, Q2, Q3 and Q4 give a parallel representation of 4 bits data word. To have synchronization between the PN sequences obtained from shift registers and the data word, both the circuit is clocked with synchronized clocks. Therefore, the time duration of 4 bits data word combination should be same as, the time period of one PN sequence. The time period of clock used in a data word generator circuit is equal to the time period of PN sequence duration which is equal to 60μ seconds.

Figure 4.9 shows the software simulated 4 bit data word output. Table:4.3 shows all the combination of 4 bits data word obtained from the circuit.

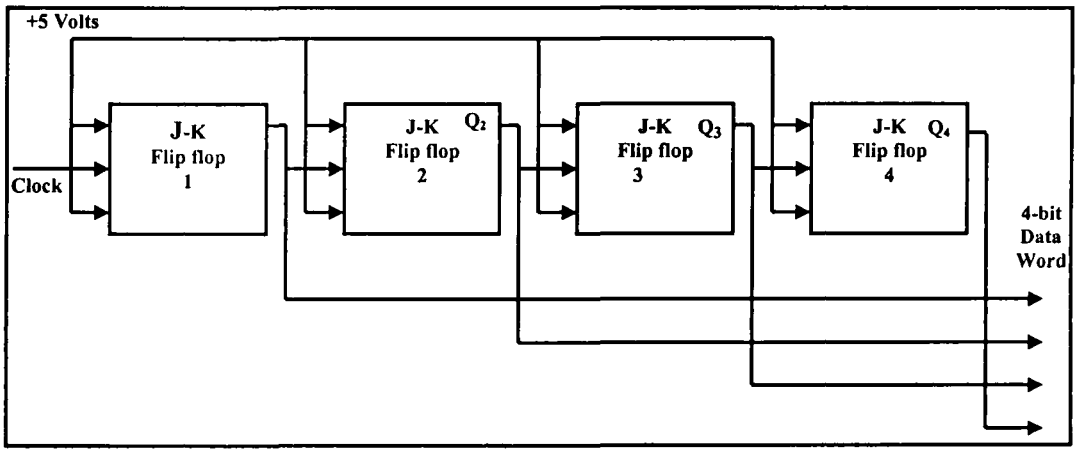


Fig.4.8: Block diagram of Data Word generator [23]

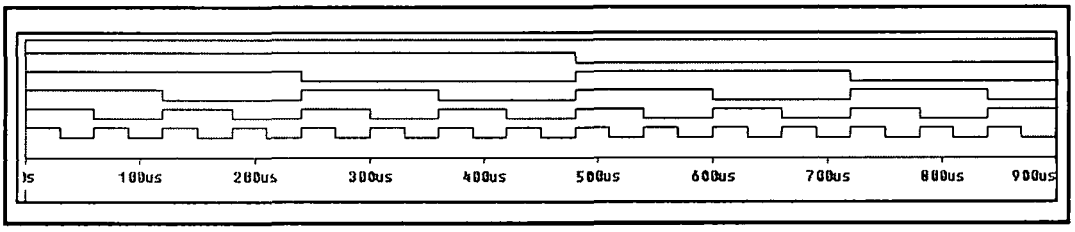
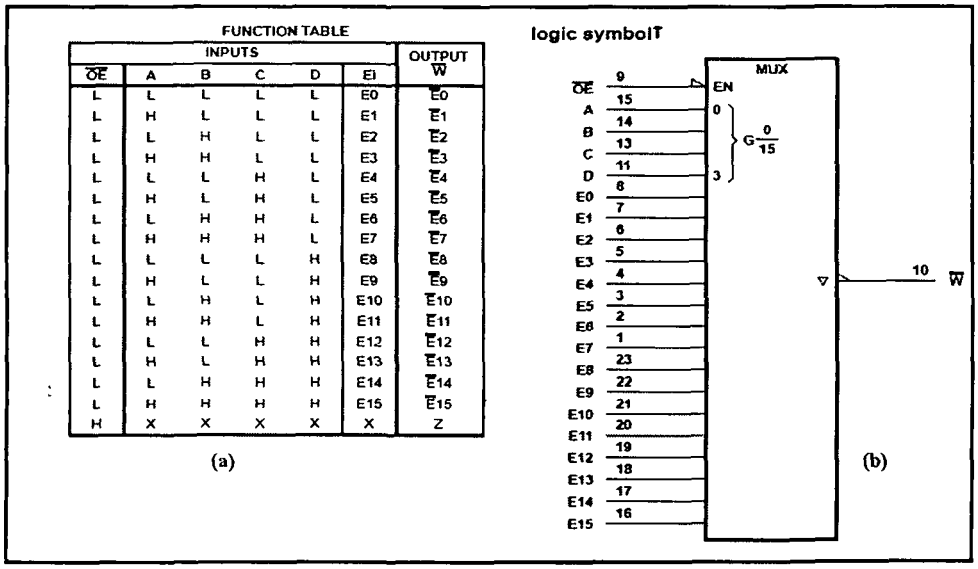


Fig.4.9: Simulated waveforms of Data word generator

4.3.4 PN Sequence Selector and Bi-level shifter

Code selector is basically a 2^N to1 switch/ multiplexer [24]. It takes 2^N inputs gives one output depending upon the different inputs applied at select lines. As shown in the block diagram of a transmitter in Figure 4.1, the output of data word, as the 4-bit word is applied at select control and PN sequences as inputs to this code selector switch. In this design we have used IC74as250 which is 16 to 1 multiplexer [24]. Figure 4.10 shows the truth table, logic diagram and pin diagram of the multiplexer.



FUNCTION TABLE

INPUTS						OUTPUT
$\overline{OE}$	A	B	C	D	EI	W
L	L	L	L	L	E0	$\overline{E0}$
L	H	L	L	L	E1	$\overline{E1}$
L	L	H	L	L	E2	$\overline{E2}$
L	H	H	L	L	E3	$\overline{E3}$
L	L	L	H	L	E4	$\overline{E4}$
L	H	L	H	L	E5	$\overline{E5}$
L	L	H	H	L	E6	$\overline{E6}$
L	H	H	H	L	E7	$\overline{E7}$
L	L	L	L	H	E8	$\overline{E8}$
L	H	L	L	H	E9	$\overline{E9}$
L	L	H	L	H	E10	$\overline{E10}$
L	H	H	L	H	E11	$\overline{E11}$
L	L	L	H	H	E12	$\overline{E12}$
L	H	L	H	H	E13	$\overline{E13}$
L	L	H	H	H	E14	$\overline{E14}$
L	H	H	H	H	E15	$\overline{E15}$
H	X	X	X	X	X	Z

(a)

Fig.4.10: Multiplexer (16 to 4) IC 74 as 250, (a) Truth table, (b) Logic Diagram [24]

Simulated circuit is shown in Figure 4.11. Figure 4.12 shows the different inputs and output from the data selector. The input signal is applied from the shift register which consist of 15 PN sequences and other input is the data word obtained data word generator.

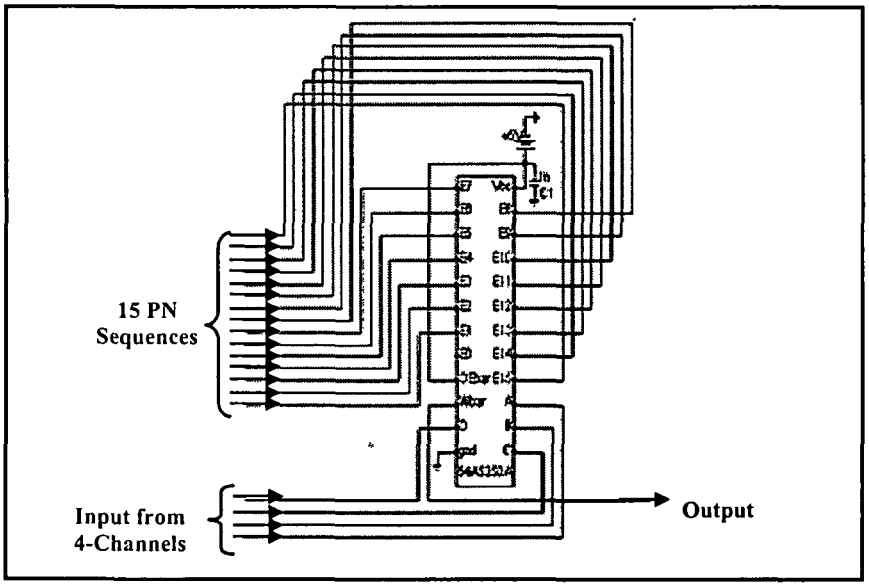


Fig.4.11: Pin diagram of Data selector [23]

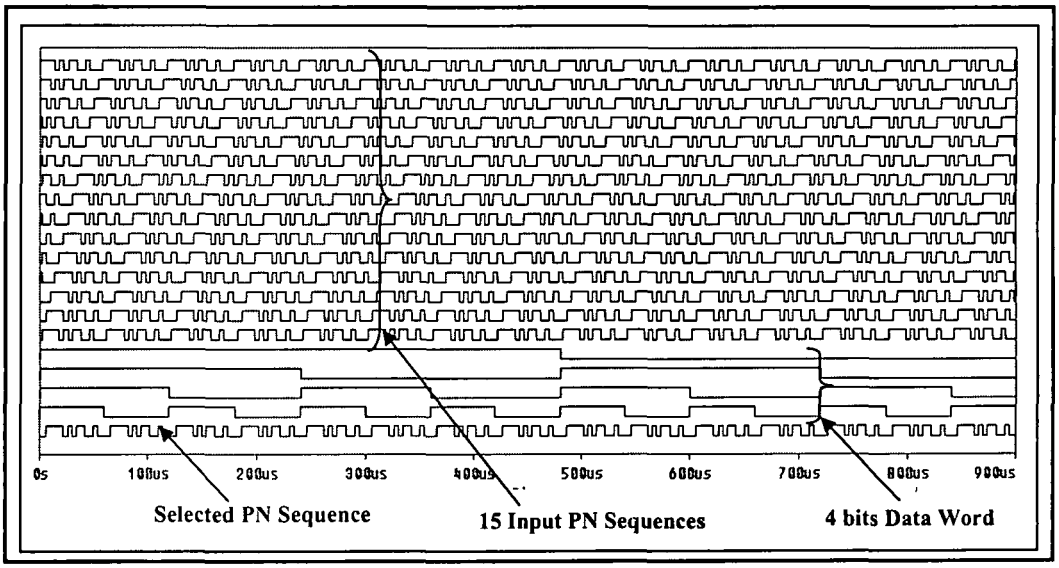


Fig.4.12: Simulated Input and Output signals of Data Selector

The bi-level shifter is used for converting the uni-polar PN sequences into bi-polar state by shifting the level of each selected PN sequence, to, $+V_{cc}$ and $-V_{cc}$ for logic high and logic low respectively. These bi-polar PN sequences are used in the multiplier stage of

modulator for generating the binary phase shift keying signal [25]-[26]. The circuit for converting the output of multiplexer into bi-polar PN is shown below in Figure 4.13. It is working as a comparator circuit in open loop configuration using high speed operational amplifier AD817/AD [24]. Where $+V_{cc}$ and $-V_{cc}$ are the operating supply used for the circuit with the help of pot meter, output is adjusted to 1Volt before it is applied to multiplier stage. Figure 4.14 shows the simulated waveform of the bi - level shifter.

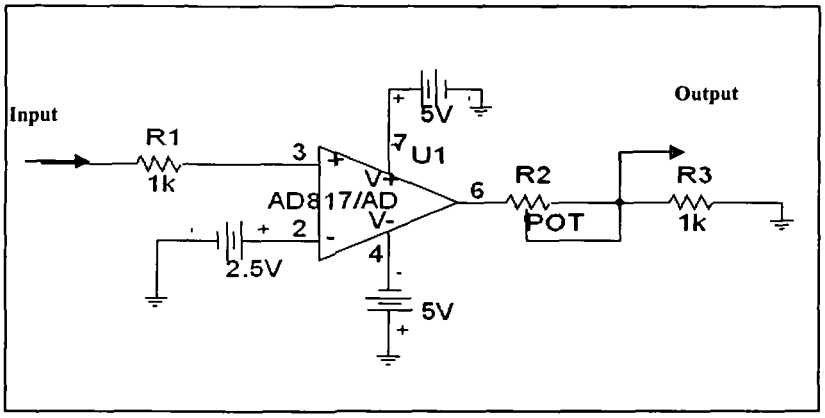


Fig.4.13: Simulated Bi-level Circuit diagram

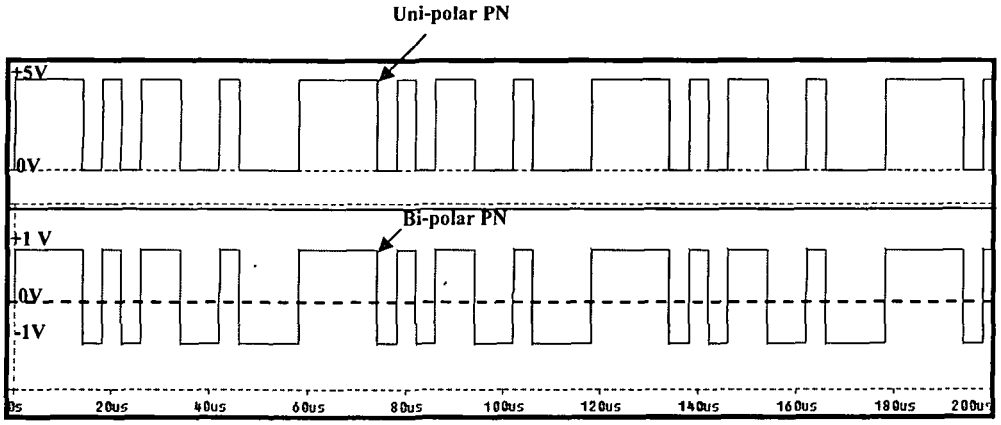


Fig.4.14: Simulated Input and Output of Bi-level Shifter

4.3.5 BPSK Modulator

To transmit digital data signals many modulation techniques are proposed in the literature. Among all modulation schemes, BPSK is very simple and robust with least BER performance [25]-[27]. It is widely used in many systems as for satellite communication, global positioning system, military and commercial application also. In this designing we have used the BPSK modulation scheme for the simulation of proposed 4-channel CPSK based DSSS system. The BPSK signals are generated by multiplying the bipolar PN sequences with the carrier frequency using an analog multiplier. The multiplication results in 180 degree phase change of constant-amplitude carrier signal according to two possible values of digital binary signal '1' and '-1'. If V_m, is the peak amplitude of sinusoidal carrier, f_c, frequency and m(t), the modulating signal then the BPSK signal is expressed as [15]:

$$s_{1,2}.(t) = m(t)V_m Sin(2\pi f_c)t \qquad 0 \leq t \leq T \qquad (4.2)$$

If, T= bit duration of the modulating signal. The Equation (4.2), for binary signal m(t)= '1' and m(t)= '-1' is written as:

$$s_1(t) = V_m Sin(2\pi f_c t) \quad \text{for,} \quad m(t) = '1' \qquad (4.3)$$

$$s_2(t) = V_m Sin(2\pi f_c t + \pi) \quad \text{for,} \quad m(t) = '-1' \qquad (4.4)$$

where s_1 and s_2 are the parameters to represent a modulated signal that bring an information '1' , '-1' respectively and are 180 degree out of phase as shown below in Figure 4.15. Figure 4.16 shows the graphical representation of BPSK signal.

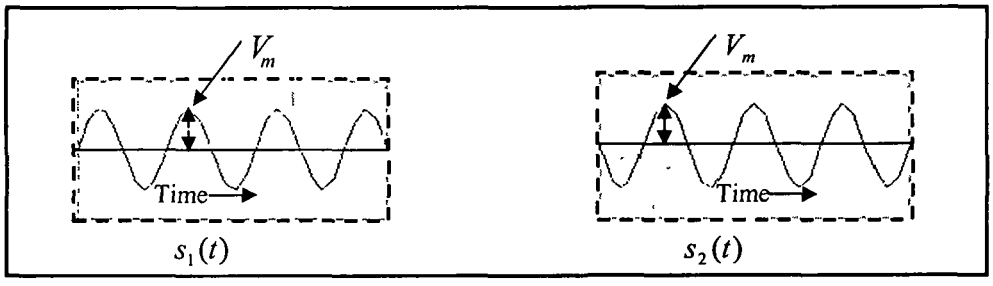


Fig.4.15: Representation of '1' and '0' in BPSK [25]

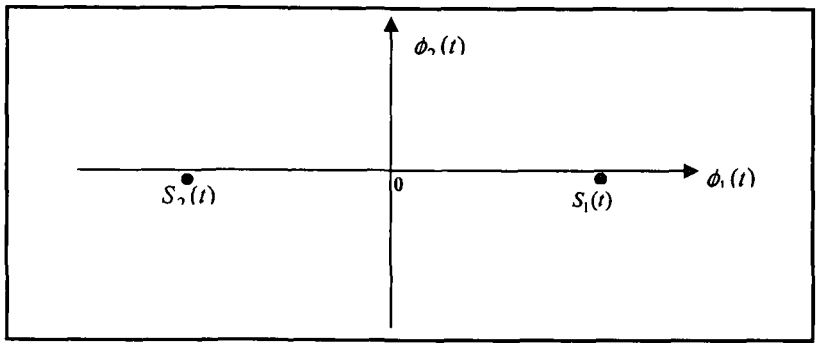


Fig.4.16: BPSK signal constellation [25]

$$\phi_1(t) = \sqrt{\frac{2}{T}} Sin(2\pi f_c t), \quad 0 \le t \le T \tag{4.5}$$

$$\phi_2(t) = -\sqrt{\frac{2}{T}} Sin(2\pi f_c t), 0 \le t \le T \tag{4.6}$$

BPSK signal is generated by multiplying the carrier signal $V_m Sin(2\pi f_c t)$ with the biplar binary signal m(t), as expresed by Equation (4.2). Figure 4.17 shows the block diagram representation of modulator stage [26].

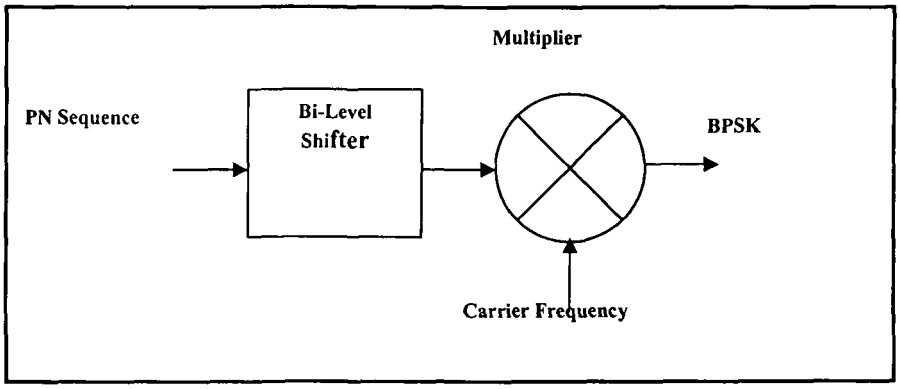


Fig.4.17: Block diagram of Modulator [26]

In this design we have used integrated circuit AD834 as an analog multiplier in the modulator circuit for generating the BPSK signal. It is a monolithic, laser-trimmed four-quadrant analog multiplier intended for use in high frequency applications, with a trans-conductance bandwidth (RL = 50 Ω) in excess of 500 MHz from either of the

differential voltage inputs. In multiplier modes, the typical total full-scale error is less than 0.5%, and performance is relatively insensitive to temperature and supply variations due to the use of stable biasing based on a band gap reference generator and other design features [24]. The overall multiplier transfer function of this multiplier is given as:

$$W = (X_1 - X_2)(Y_1 - Y_2) \tag{4.7}$$

where the *X1*, *X2*, *Y1*, *Y2* inputs and *W* output are in volts. Pin number 1, 2, 3 and 4 represents the *X1*, *X2*, *Y1*, *Y2* inputs of the integrated circuit AD834. The output obtained is obtained from *W* which is represented by pin 7 as shown in Figure 4.18. Figure 4.19 shows the different simulated waveforms of the modulator stage. The trace (a) represents the local carrier of 100 MHz with amplitude of +1 volts. Waveform b shows the bi-polar PN sequence with amplitude +1 volts for logic high and -1 volt for logic low. Waveform c represents the BPSK signal at 100 MHz carrier frequency which obtained by multiplication of both signals shown by waveform (a) and (b).

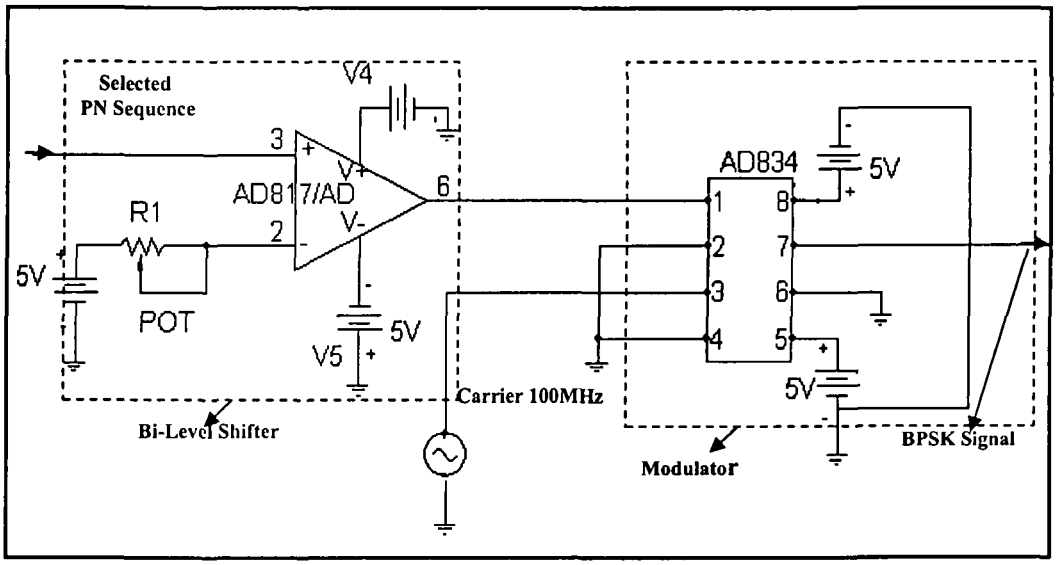


Fig.4.18. Circuit diagram of BPSK modulator

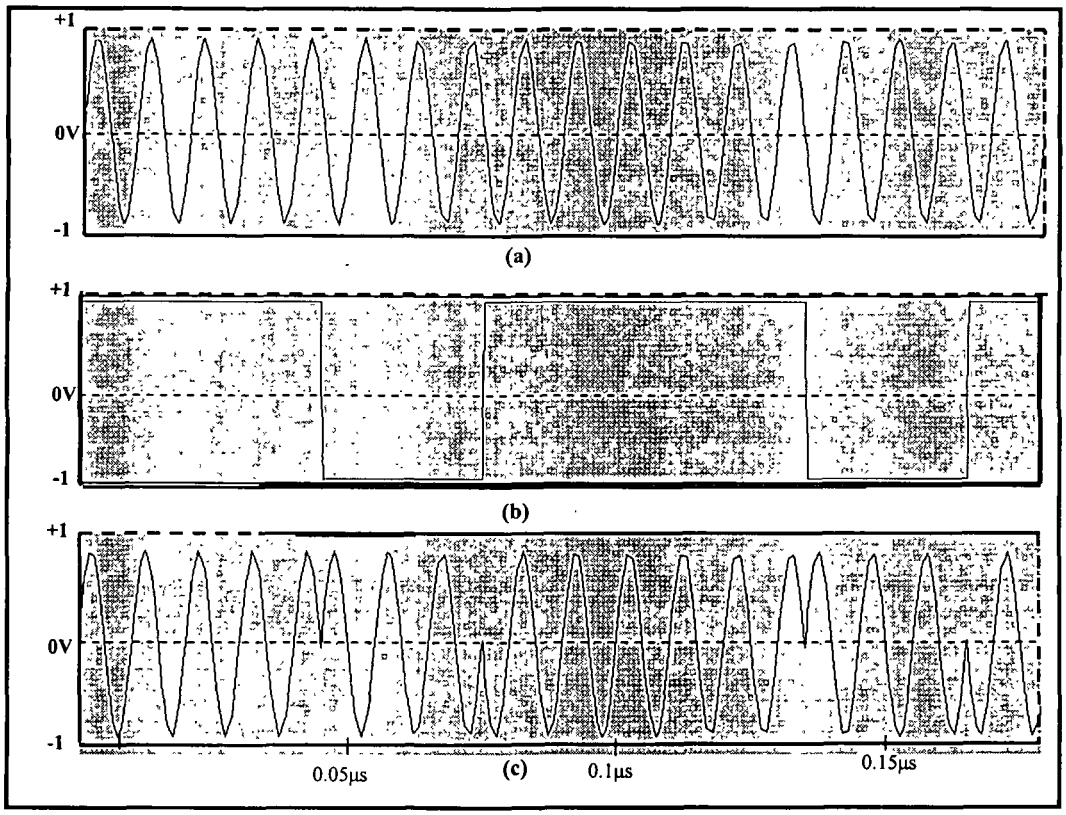


Fig.4.19: Input/output signals of modulator, (a) Carrier signal of 100MHz, (b) Bi-polar PN sequence, (c) BPSK signal as output of modulator

4.4 Simulation Results of CPSK based DSSS Transmitter

We have simulated the CPSK based DSSS transmitter circuit at 100 MHz carrier frequency using binary phase shift keying (BPSK) modulation technique. The simulated block diagram of the transmitter is shown in Figure 4.20. Figure 4.21 shows simulated circuit diagram using the Microsim software of the transmitter. Table-4.3 lists the different components with specification used for the simulation of transmitter circuit.

Table-4.3 List of components with specification

Block	Type	Value
PN Generator	D-flip flop- 4 No	SN74ls74a
	Resistance - 01 No	10 Ohms, 0.25Watt
	Capacitor- 01 No	2nF
	EX-OR gate-01 No	SN7486
	D-Flip Flop-15 No	SN74ls74a
Data word Generator	JK Flop Flops-4 No	SN74F109
PN Sequences selector and Bi-level Shifter	Multiplexer- 01 No	74as250
	NOT gate-01 No	74ls04
	Op Amplifer-01 No	AD817/AD
	Resistance -01 Pot meter -01	10K Ω, 0.25W 10K Ω, 0.5W
Modulator	Analog Multiplier	AD834

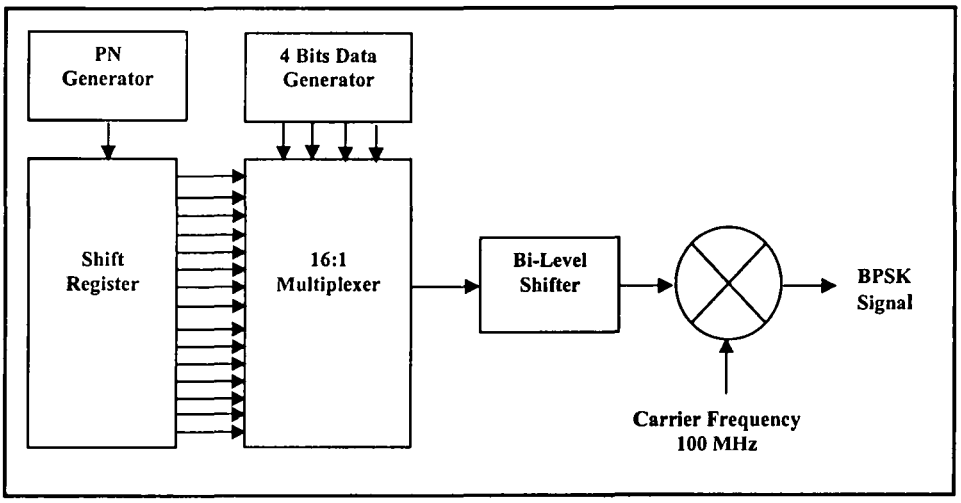


Fig.4.20: Simulated block diagram of CPSK based DSSS transmitter

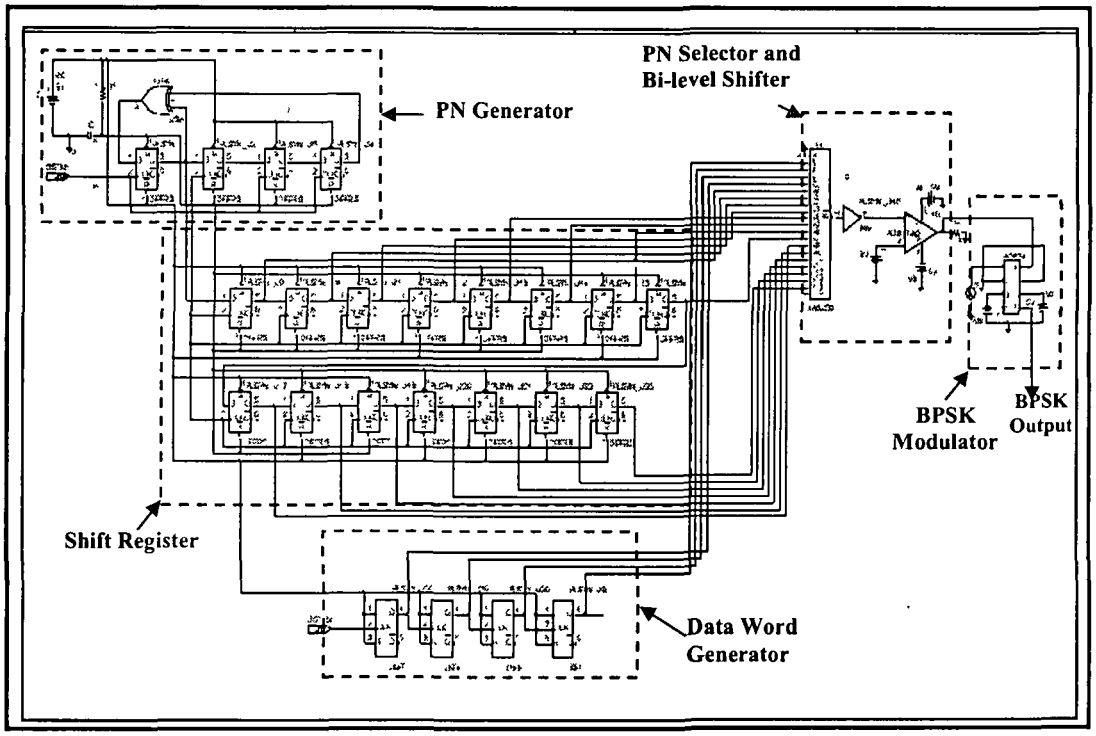


Fig.4.21: Simulated circuit diagram of CPSK based 4-channel DSSS transmitter

Figure 4.22 shows the simulated digital signal waveforms generated by different modules. In the designed 4-channel CPSK based DSSS system, digital signals are generated by the PN sequence generator, shift register and data word generator. All these signals waveforms are shown in the Figure. It shows 4-PN sequences, generated by PN sequence generator circuit. The time period of one PN sequence is 60μ which consists of 15 chips each with 4μ second duration. Next it shows the 15 PN sequences generated by shift registers. The same clock signal is used for both, PN sequence generating circuit and shift register circuit. In same Figure, 4 bits data word waveform is also shown which is obtained from the data word generator and applied to the control pins of the multiplexer. Each bit in the data word is of 60μ and are synchronized with PN sequences.

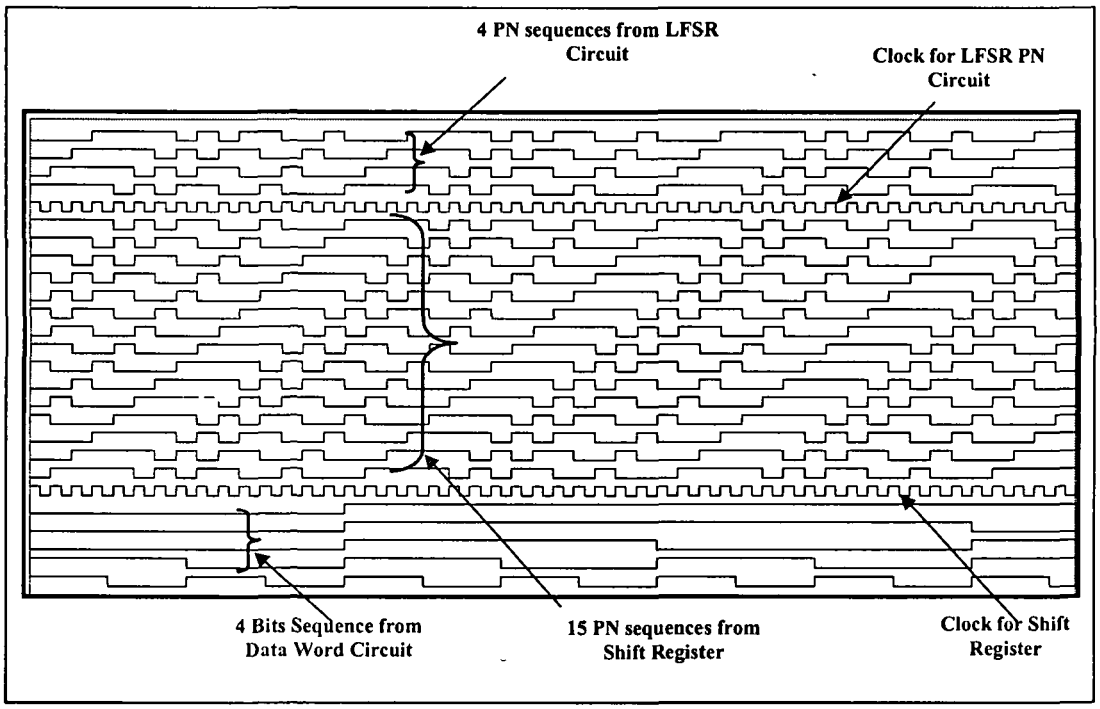


Fig.4.22: Simulated outputs from PN generator, shift register and data word circuit

Figure 4.23 shows the analog wave forms generated at the different stages of the transmitter. The analog stages are bi-level shifter and modulator stage. The bi-polar circuit receives the uni-polar PN signal waveforms from the multiplexer and changes it into a bi-polar as discussed earlier. The output from bi-polar circuit is applied to analog multiplier as one input and the second input is the carrier signal of 100MHz. The multiplier generates the BPSK signal as DSSS signal.

In Figure 4.23 trace (a) shows the input and output signals of the bi-level shifter stage. It takes a uni-polar PN sequence obtained from the output of data selector (multiplexer stage) and changes to bi-level which is required for the generation of BPSK signal. Waveform (b) represents the carrier frequency at 100MHz frequency and with amplitude 1 volt. Waveform (c) shows the output of CPSK based 4-channel DSSS transmitter generated by modulator stage as BPSK signal.

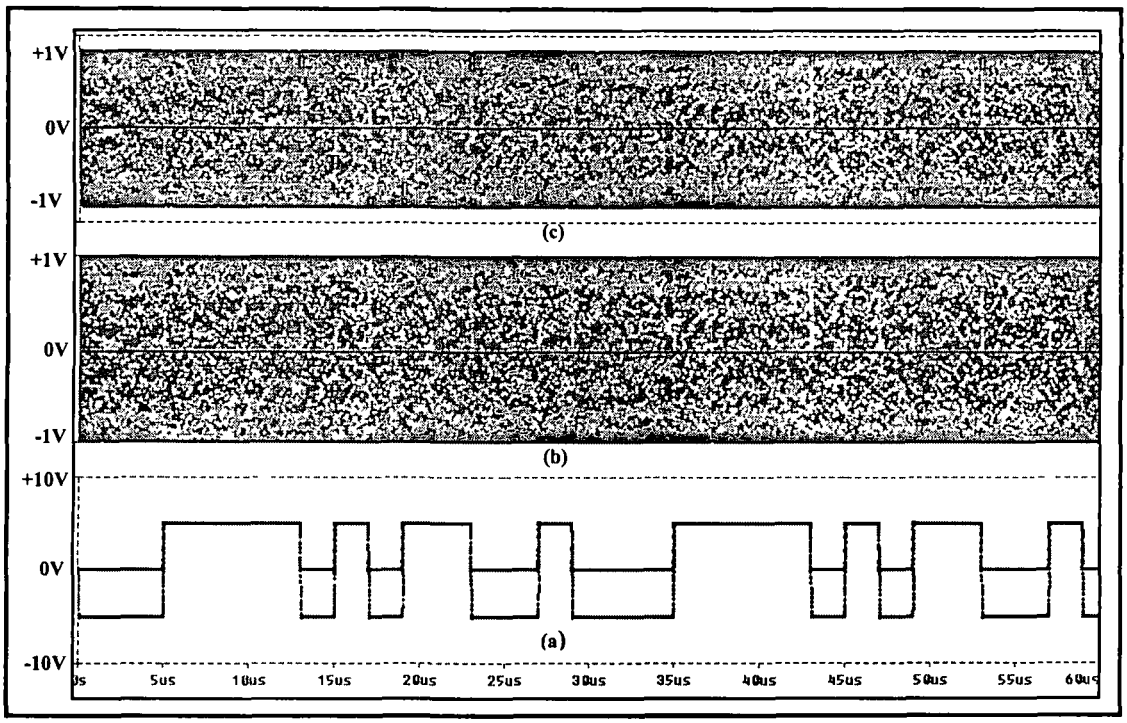


Fig.4.23: Simulated waveforms of the CPSK-DSSS transmitter, (a) Inputs to the modulator (b) Output and input of Bi-level shifter,, (c) BPSK which represents DSSS

4.5 CPSK based DSSS Receiver Design

A simple block diagram representation of a wireless receiver is shown in Figure 4.24. It consists of the low noise amplifier (LNA), down converter and demodulator stage. The LNA stage is very important and it should not introduce any noise which may degrade the performance of system by decreasing the signal to noise [27]. Down conversion section convert the channel frequency to a lower frequency usually with a mixer stage. Lastly, the down converted signal is processed in the demodulator stage and carried is decoded (demodulated) to extract the modulating data. Depending upon modulation technique, the signal is processed in the demodulator section. . First, we will concentrate on the design and simulation of CPSK based DSSS system using coherent detector and subsequently with proposed technique.

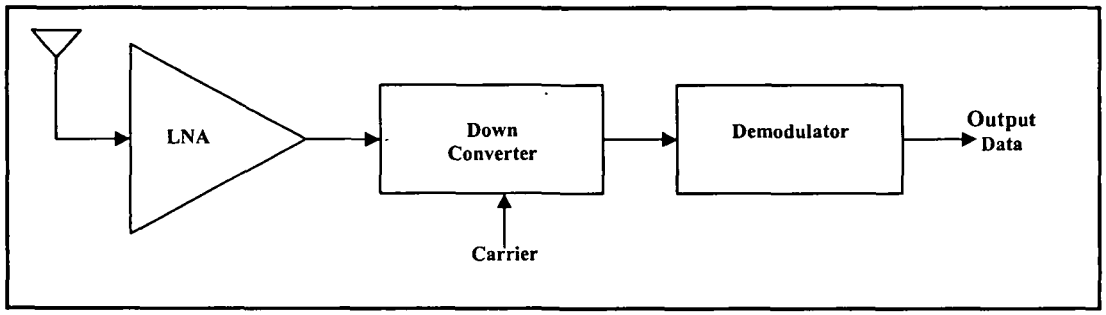


Fig. 4.24: Block diagram of a simple wireless receiver [27]

4.5.1 BPSK Demodulator

Figure 4.25 shows the block diagram of BPSK demodulator. Considering coherent detection of a BPSK signal in which the received signal is perfectly synchronized in frequency, phase with the local carrier signal [18]-[21]. The demodulator multiplies the received signal with the local carrier as given below:

The received signal can be written as:

$$V_{IN} = A_1 Cos\,\omega t \quad \text{or} \quad V_{IN} = -A_1 Cos(\omega t + \pi) \tag{4.8}$$

where A_1 and ω are the amplitude and frequencies respectively.

If the local carrier is expressed as:

$$V_{LO} = A_2 Cos\,\omega t \tag{4.9}$$

Then the output of multiplier can be written as:

$$V_{out} = A_1 A_2 Cos^2 \omega t \text{ , or, } V_{out} = -A_1 A_2 Cos^2 \omega t \tag{4.10}$$

From trigonometry the equation (4.10) can be written as:

$$V_{out} = \frac{A_1 A_2}{2}(1 + Cos2\omega t), \text{ or } V_{out} = -\frac{A_1 A_2}{2}(1 + Cos2\omega t) \tag{4.11}$$

Figure 4.25 shows the different inputs and output waveform as expressed by Equation (4.8), (4.9) and (4.10). We have used the same multiplier circuit as was used in the transmitter for modulation with integrated circuit IC AD/834 [24]. In Figure 4.26 waveforms (a), (b) and (c) shows the received BPSK signal applied to demodulator, local coherent signal and output obtained from the demodulator stage.

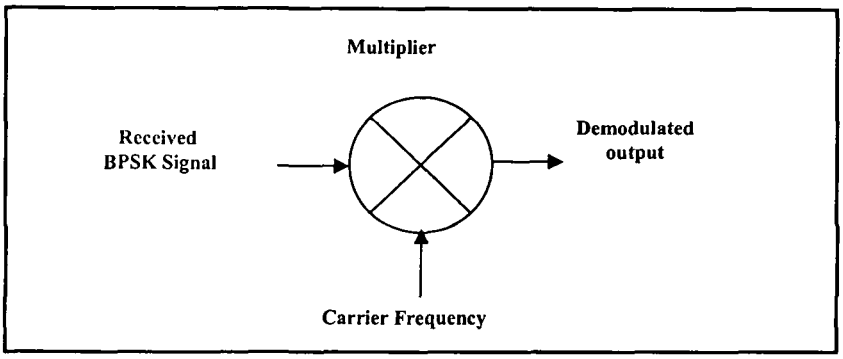


Fig.4.25: Block diagram of Demodulator [26]

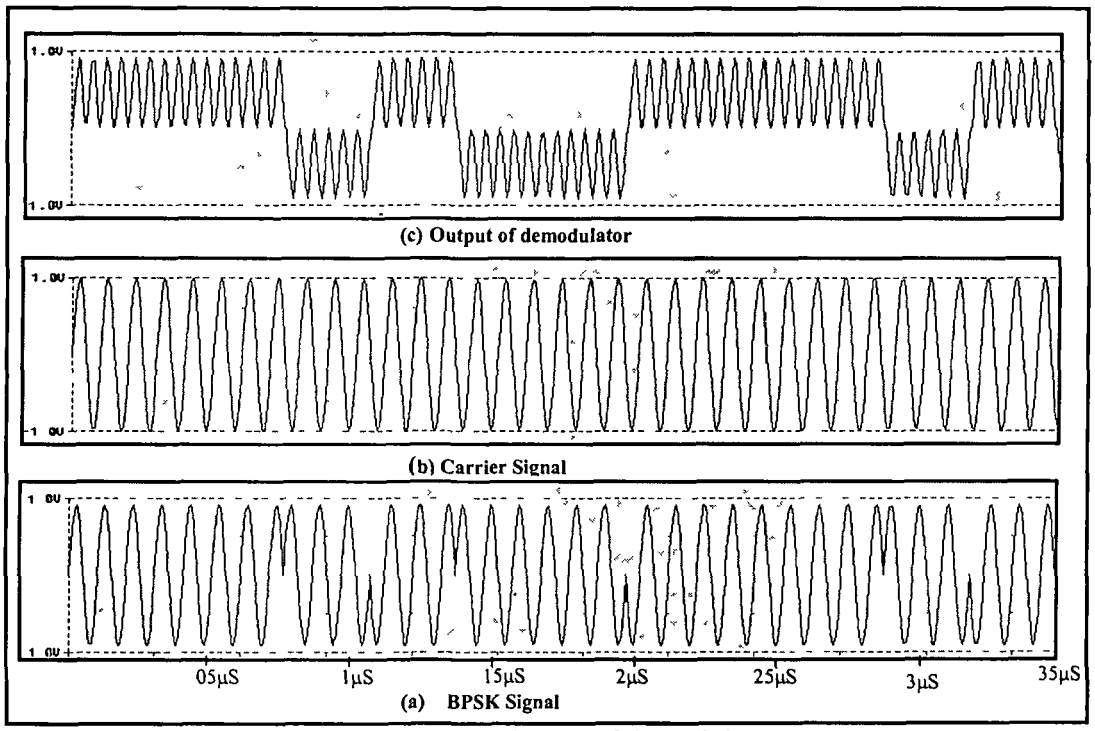


Fig.4.26: Input and output signals of demodulator stage

4.5.2 Filtering and Decision Device

A filter is a frequency selective device that removes unwanted information from the original message signal. Unwanted signals can be noise or other undesired information. Many filters as LPF, HPF and BPF of different order are available for filtering the

signal in the communication systems. In this design we have user second order Sallen-Key low pass filter [28] used for filtering the demodulated BPSK signal as shown in the Figure 4.27.

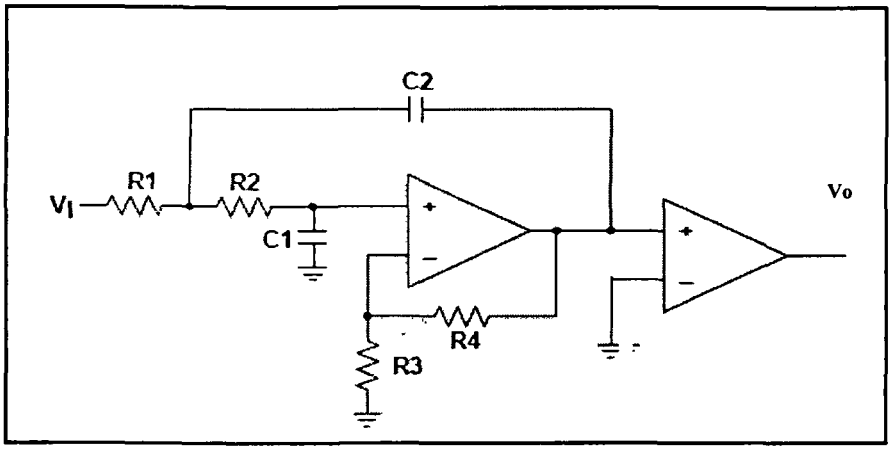


Fig.4.27: Sallen-Key Low Pass filter and Decision Device [24]

The transfer function of this low pass filter is expressed as:

$$\frac{V_o}{V_I} = \frac{K}{S^2(R_1R_2C_1C_2)+S(R_1C_1+R_2C_1+R_1C_2(1-K))+1} \tag{4.12}$$

Let $S = j2\pi f$, $f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$, and $Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1+R_2C_1+R_1C_2(1-K)}$, with these the Equation (4.12), can be expressed as:

$$H_{LP} = \frac{K}{-\left(\frac{f}{f_c}\right)^2+\frac{jf}{Qf_c}+1} \tag{4.13}$$

Where f_c is the corner frequency and Q is the quality factor. When $f << f_c$ Equation (3.14) reduces to K, and the circuit passes signals multiplied by a gain factor K. When $f = f_c$, Equation (4.14) reduces to $-jKQ$, and signals are enhanced by the factor Q. When $f >> f_c$, Equation (4.14) reduces to $-K\left(\frac{f_c}{f}\right)^2$.

Also with $R_1 = R_2$, and $C_1 = C_2$, the results in expression for f_C, and Q, above are simplified as:

$$f_C = \frac{1}{2\pi RC}, \text{ and, } Q = \frac{1}{3-K} \tag{4.14}$$

Using the above equation with $R_1 = R_2 = 100Ohms$ and $C_1 = C_2 = 1nF$, and gain $K = 1$, the circuit was simulated to filter the BPSK signal obtained from the analog multiplier at 100 MHz carrier frequency. These values of resistances, capacitor causes the low pass filters to suppress the sinusoidal components with 2ω frequency and gives the output as:

$$V_{out} = \frac{A_1 A_2}{2}, \text{ or } V_{out} = -\frac{A_1 A_2}{2} \tag{4.15}$$

These voltages are decoded to logic '1' and logic '0' respectively. Figure 4.28 shows the block diagram of the filter and decision device.

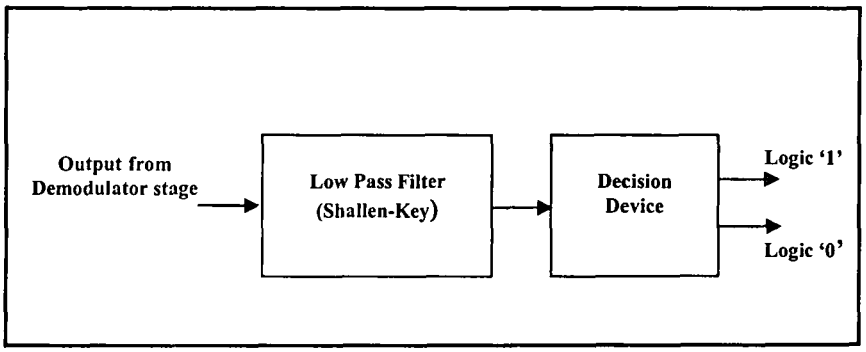


Fig.4.28: Block diagram of demodulator and filter [29]

Under zero-noise condition BPSK signal applied at the receiver input, the output of low pass filter will be positive ($\frac{A_1 A_2}{2}$) for logic high ('1') and negative ($-\frac{A_1 A_2}{2}$) for logic low ('0'). Therefore, the decision device has been implemented using operational amplifier AD 817/AD under open loop gain configuration. Figure 4.29 shows the simulated waveforms obtained from LPF and decision device using Microsim software Version 8.0.

In Figure 4.29 waveforms (a) shows the input to the filter. It is the output of multiplier stage (demodulator stage). It is a product of input BPSK signal and local coherent carrier signal. The filter as discussed above suppressed the high frequency component and provided the output shown with a trace (b). Trace (c) shows the shaped output of the filter stage. It is the output of the decision device which compares the signal (b) with a preset value and shape the signal as shown by trace (c).

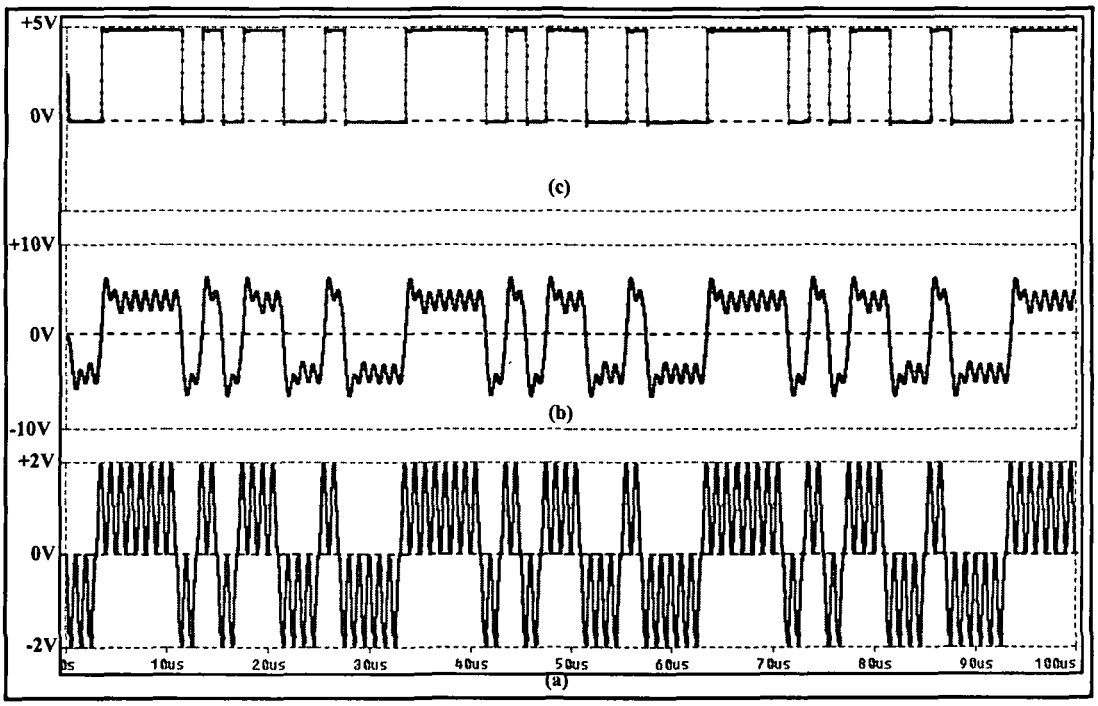


Fig.4.29: Input and out waveforms of demodulator and filter, (a) Input to filter, (b) Output from filter and (c) Output from decision device

4.5.3 Correlator Circuit

In the receiver, the signal obtained at the output of the filter and decision device shows the recovered PN sequence [30]. This recovered PN sequence is one of the 15 PN sequences, used by the transmitter for coding/multiplexing the 4-channels. The receiver has to identify this recovered PN sequence. To identify this received PN sequence, it is to be correlated with the phase matched replica of all 15 PN sequences used at the transmitter side. Therefore, all 15 PN sequences used in the transmitter are delayed for

phase matching; as the recovered PN sequence is delayed due to propagation and processing time took by the components used in the receiver.

The correlator circuit consists of 15 XNOR gates. At one input of each gate, the received PN sequence is connected and other input is connected with locally generated, phase matched PN sequences. The received PN sequence will match with one output of 15 locally generated PN sequences. Therefore, out of 15 XNOR gates only one gate will provide continuous high outputs for the PN sequence duration. Figure 4.30 shows the output of correlator circuits. The output of each correlator is applied to integrate and dump circuit for integration.

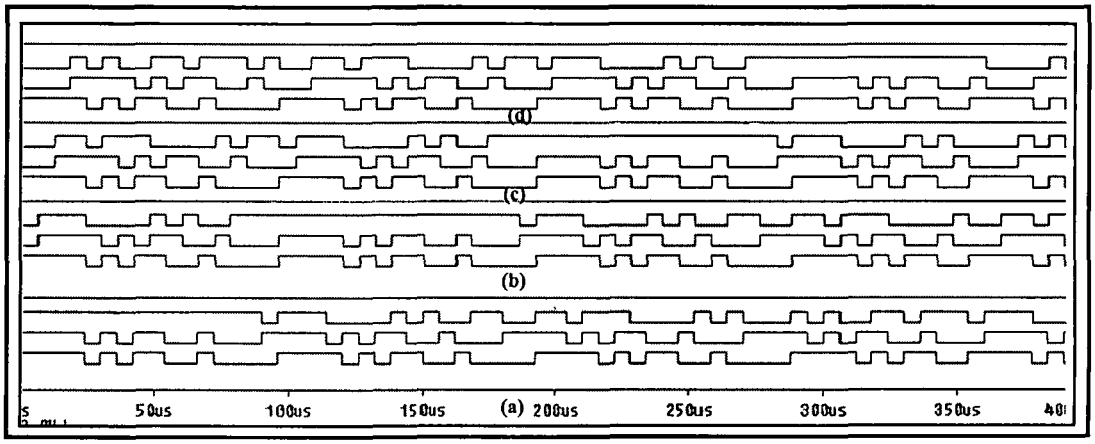


Fig.4.30: Simulated waveform of correlator, (a) Output of first XNOR gate, (b) Output of second XNOR gate (c) Output of third XNOR gate, (d) Output of 15^{th} XNOR gate

4.5.4 Integrate and Dump

Integrate and dump circuit integrates the output of each correlator circuit (XNOR gate) for PN duration and reset the output of Integrator circuit at the end of the integration period [31]-[32]. The Integrator circuits calculate the energy of each correlated PN sequence and compare it with a present value. The dump circuit dumps or resets the output of Integrator to zero at the end of integrates cycle and keep the Integrator to ready for integration of next PN sequence.

There are total 15 integrate and dump circuits one for each correlated output [31]. The circuit consists of the series R-C circuit as an Integrator and followed by dump circuit to reset each Integrator to zero at the end of PN duration with the help of one short pulse applied at the gate of the transistor. The response of integrator circuit depends on the ratio of the time constant τ of the circuit to the time period of one PN sequence duration T. If the PN duration is very short compared to the time constant $T << \tau$, capacitor integrates linearly and increment will be linear increment in the voltage developed across the capacitor. In this design PN chip duration is 4μ second and there are 15 chips in one PN sequence duration. PN sequence duration equal to 60μ seconds. The value of R and C are chosen as $2K\Omega$ and $1\mu F$, these values satisfy the above condition and designed circuit provides linear output across integrator. Figure 4.31 shows the circuit diagram for integrate and dump circuit. Figure 4.31 shows the generated waveform from simulation. Likewise there are total 15 such circuits one for each PN sequence.

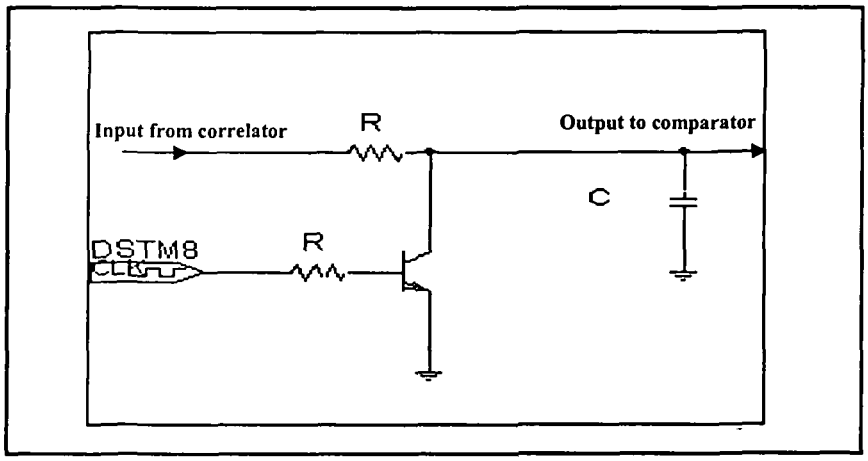


Fig. 4.31: Simulated Circuit of integrates and dump

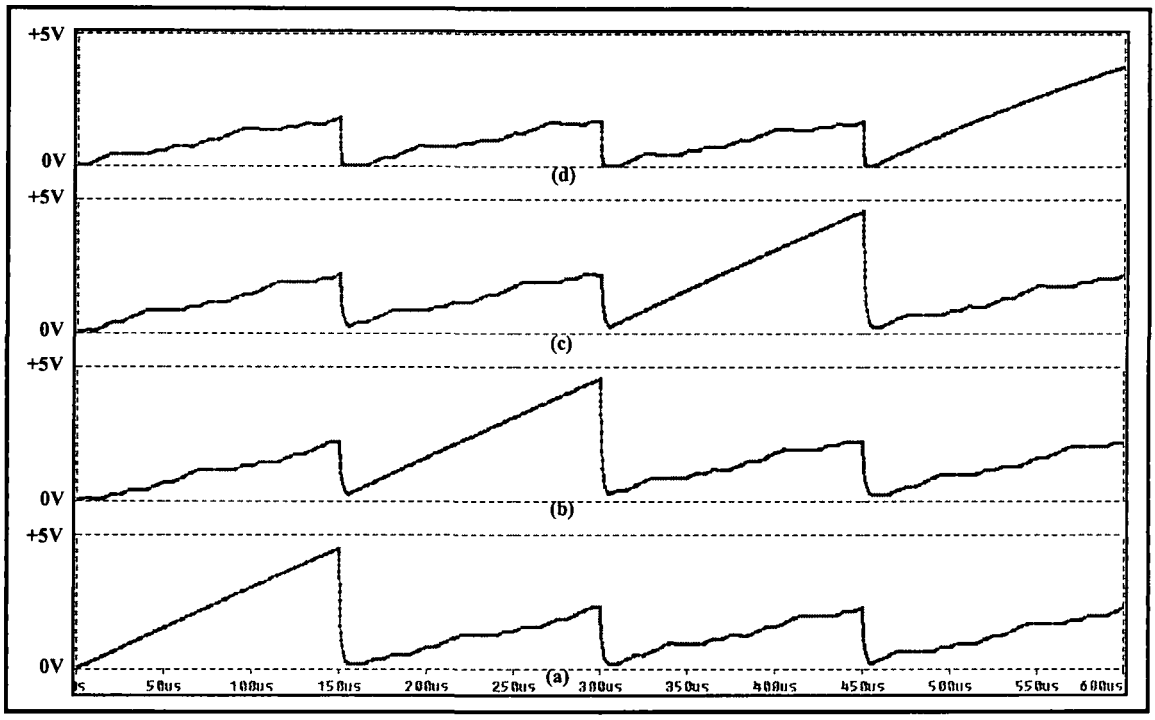


Fig. 4.32: Simulated waveform of Integrate and dump, (a) From first circuit, (b) From 2nd circuit, (c) From 3rd circuit, (d) From 4th Circuit.

4.5.5 Select Largest Logic

Select largest logic consists of a comparator using high speed operational amplifier AD817/AD, which compare the output of the integrator with the preset value [24]. If input obtained from the integrator is higher than the preset value the amplifier gets saturated to VCC (+5Volts) and gives logic '1' (logic high), otherwise logic '0' (logic low). There are total 15 decision devices (comparators) to decodes the output of the integrator to logic '1' or logic '0' as per its magnitude applied to non- inverting input. Out of 15 comparators, only one comparator will give high output and the remaining will give low output. Figure 4.33 shows the circuit for select largest logic working as a comparator circuit in open loop configuration.

Each comparator circuit is realized using AD817/AD in open loop configuration. The AD817/AD is a high speed amplifier with a slew rate of 350V/μ second and

bandwidth of 50 MHz provides the desired fast response. Figure 4.34 shows the output waveforms generated by the select largest circuit

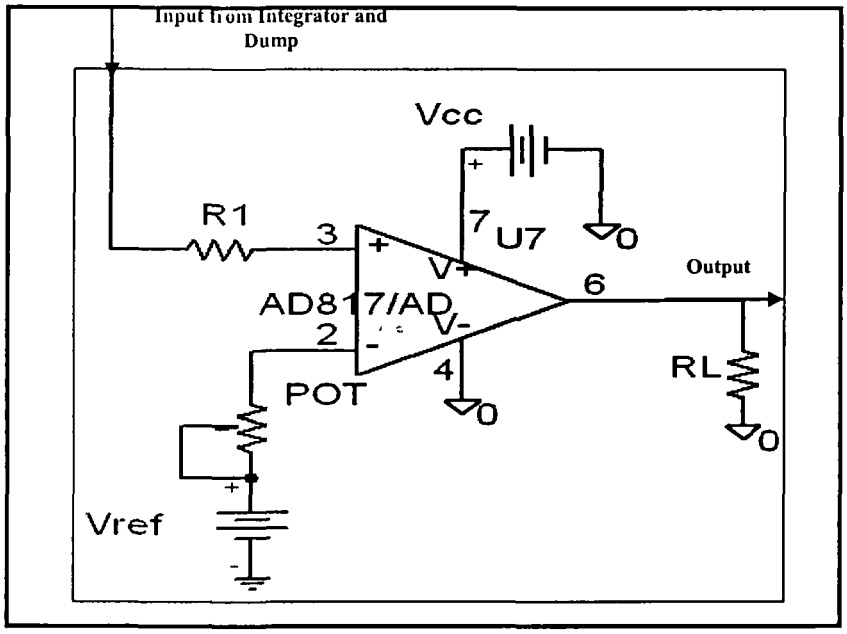


Fig.4.33: Simulated Circuit diagram for comparator

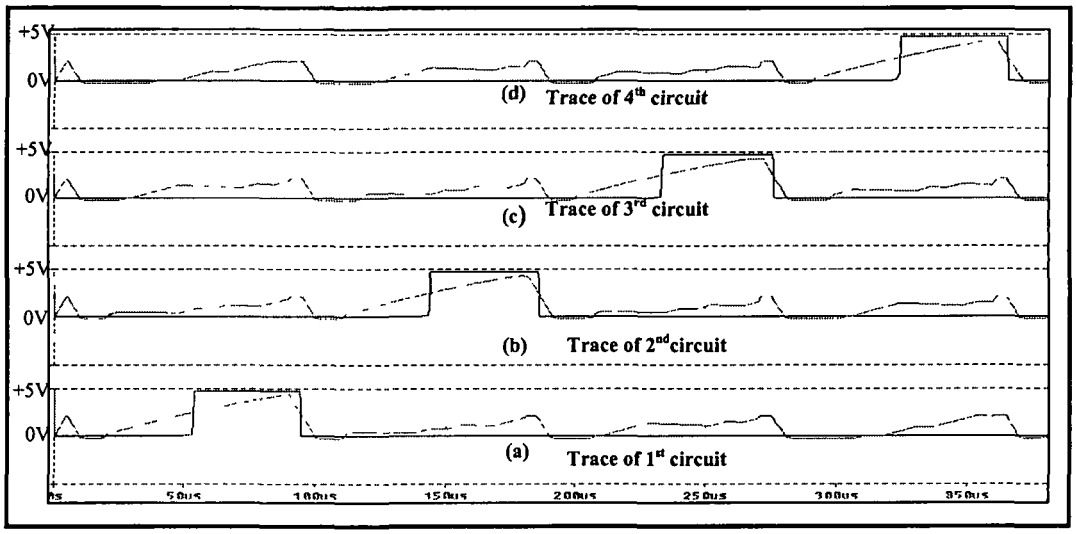


Fig.4.34: Simulated input/output waveforms of comparator circuits

4.5.6 Decoder

The decoder decodes the output of select largest module in 4-channels [11]. In general an encoder has 2^N input lines and N output lines. Out of 2^N inputs only one input must be of logic high ('1') and all other should be of logic low ('0') as shown below in the table 4.5.

Table: 4.4 Truth table of decoder

Inputs																Outputs			
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

This decoder circuit receives all the15 outputs from the select largest logic simultaneously and decodes into 4-channels. Figure 4.36 shows the circuit diagram of

decoder circuit. The decoder circuit has been realized using four 8-input OR gates with integrated circuit M74HC 4078 and the inputs to these OR gates are connected as per table 4.5 given. It is working as a 16 to 4 decoder [23]. Therefore, 15 possible input bits used in this 4- channel system are decoded into 4-bit data word as per table 4.5. We also see from the table that it shows 15 inputs form A_1 to A_{15}. Input A_0 is not used therefore, is not applied to the decoder circuit. Figure 4.37 shows the received P-Spice simulated data word waveform of 4 channels. These waveforms are the output of decoder circuit.

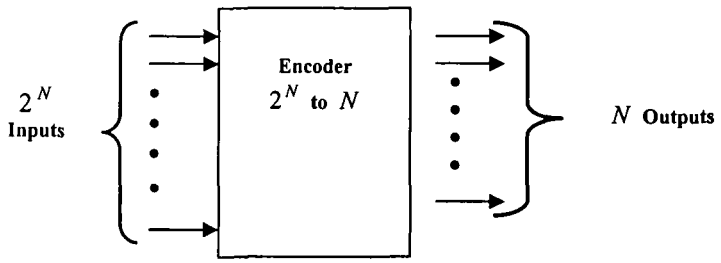


Fig.4.35: Block diagram of decoder [23]

Table: 4.5. 8 Input OR gate as a 16 to 4 decoder

Inputs	8-input OR Gate	Outputs
$A_1, A_3, A_5, A_7,$ $A_9, A_{11}, A_{13}, A_{15}$	OR Gate No 1	Y_0
$A_2, A_3, A_6, A_7,$ $A_{10}, A_{11}, A_{14}, A_{15}$	OR Gate No 2	Y_1
$A_4, A_5, A_6, A_7,$ $A_{12}, A_{13}, A_{14}, A_{15}$	OR Gate No 3	Y_2
$A_8, A_9, A_{10}, A_{11},$ $A_{12}, A_{13}, A_{14}, A_{15}$	OR Gate No 4	Y_3

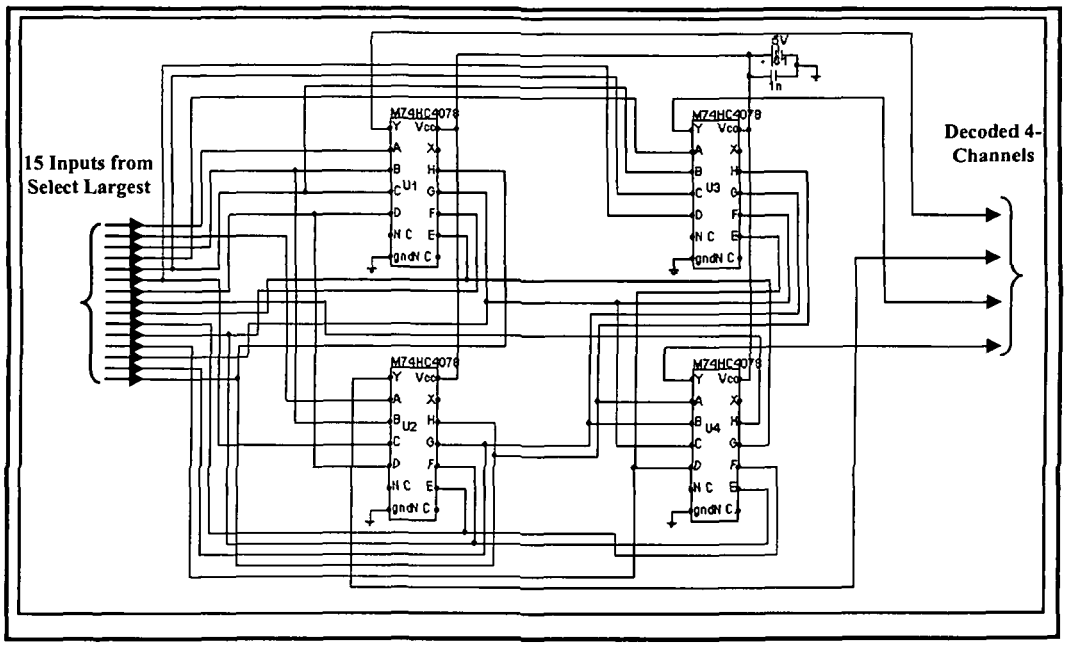


Fig.4.36: Circuit diagram of decoder

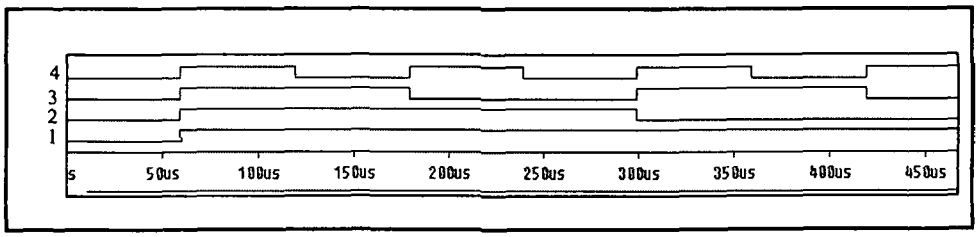


Fig.4.37: Decoder output which represents 4 -channels

4.6 Simulation Result of CPSK Receiver with BPSK Demodulator

We have designed and simulated the CPSK based DSSS multiplexed receiver for receiving the data transmitted by 4-channel CPSK based DSSS receiver. The receiver has been designed for demodulating the DSSS signal modulated by BPSK technique at 100 MHz carrier frequency. Table-4.6 shows the components used in the simulation. The simulated block diagram and circuit diagram of the receiver has been shown in Figure 4.38, and Figure 4.39 respectively.

Table- 4.6 List of components used for DSSS receiver design

Block	Type	Value
Demodulator	Multiplier-01No	AD834
Shallen-Key Filter	Amplifier-02No Resistance -02 No Capacitor-02 No	AD817/AD 100 Ω, 0.25 Watt 1nF, 100 Volts
Correlator	EX-NOR gate-04No	CD74HC7266
Integrate, Dump and Comparator	Op-Amplifier-015No	AD817/AD
	Resistance-15 No Resistance -15No Resistance -15 No Pot meter- 15No	2KΩ , 0.25 Watt 1KΩ. 0.25Watt 2KΩ, 0.25Watt 10KΩ, 0.5Watt
	Capacitor-15No	01μF, 100Volt
	Transistor -15No	2N2222
	Op-Amplifier-15No	AD811/AD
Decoder	8-Input OR gates -04No	M74HC4078

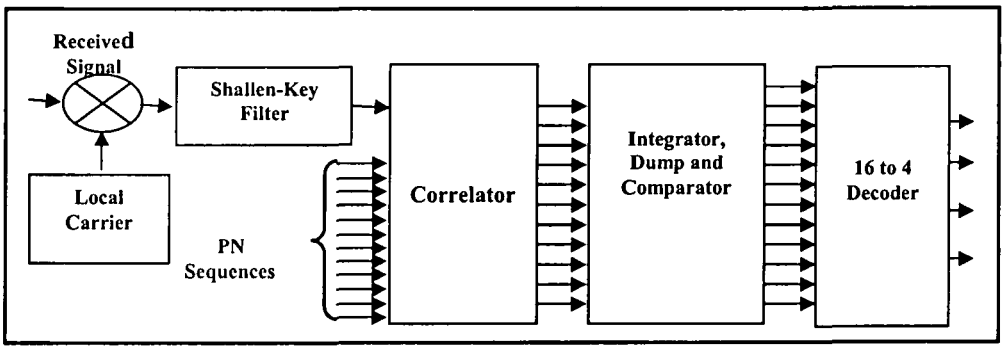


Fig. 4.38: P-Spice simulated block diagram of DSSS receiver

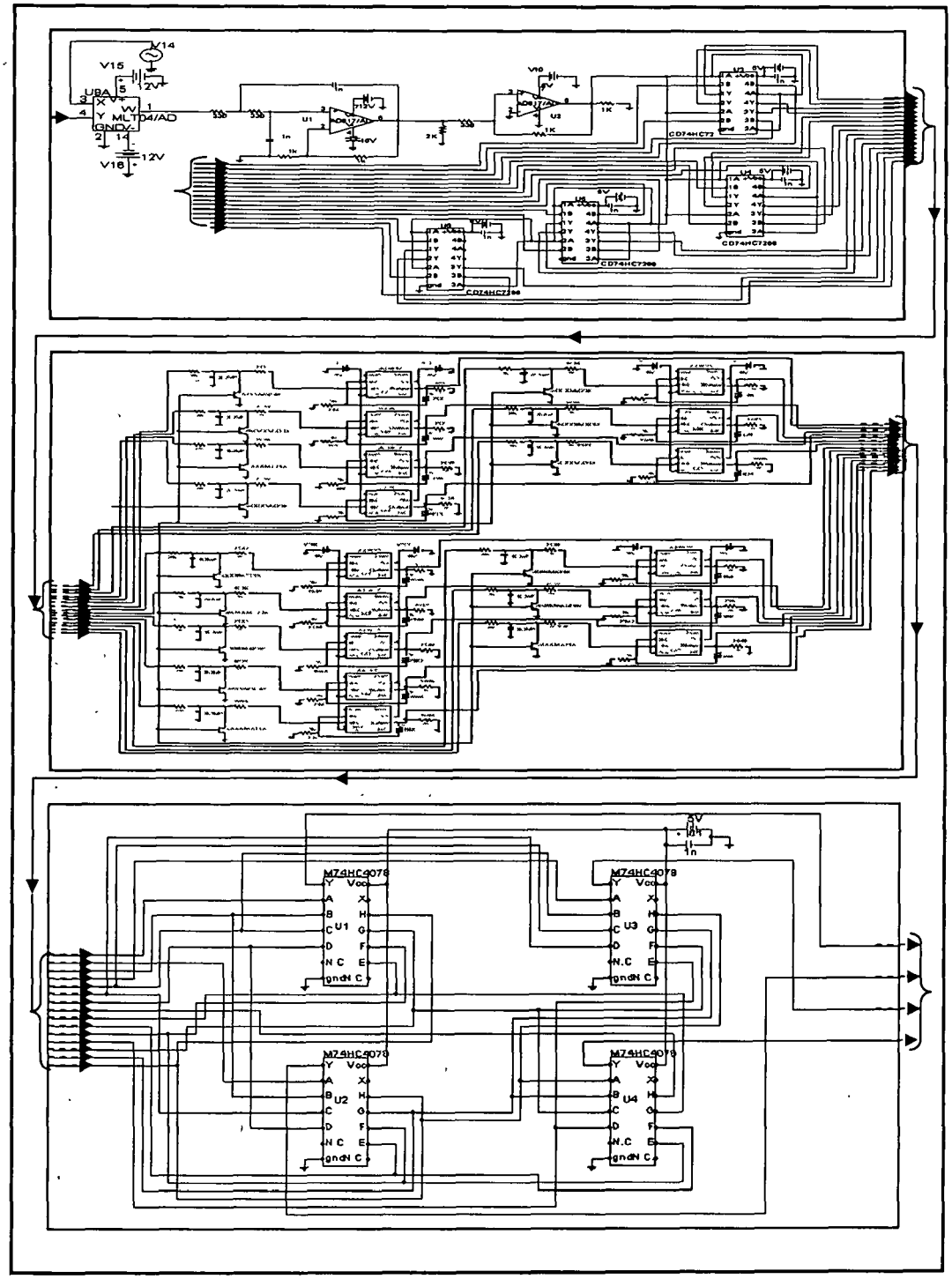


Fig. 4.39: P-Spice simulated circuit diagram of DSSS receiver

Figure 4.40 shows the simulated circuit wave forms obtained from different stages of the CPSK based DSSS receiver. In Figure 4.40, trace (a) shows the received BPSK signal at 100MHz as a DSSS signal and trace (b) shows the local coherent carrier of 100 MHz. The trace (c) shows the output of the product detector stage. Waveform (d) shows the output available at the output of Shallen-Key filter stage. The trace (e) represents the receiver PN sequence after passing the wave shaping circuit.

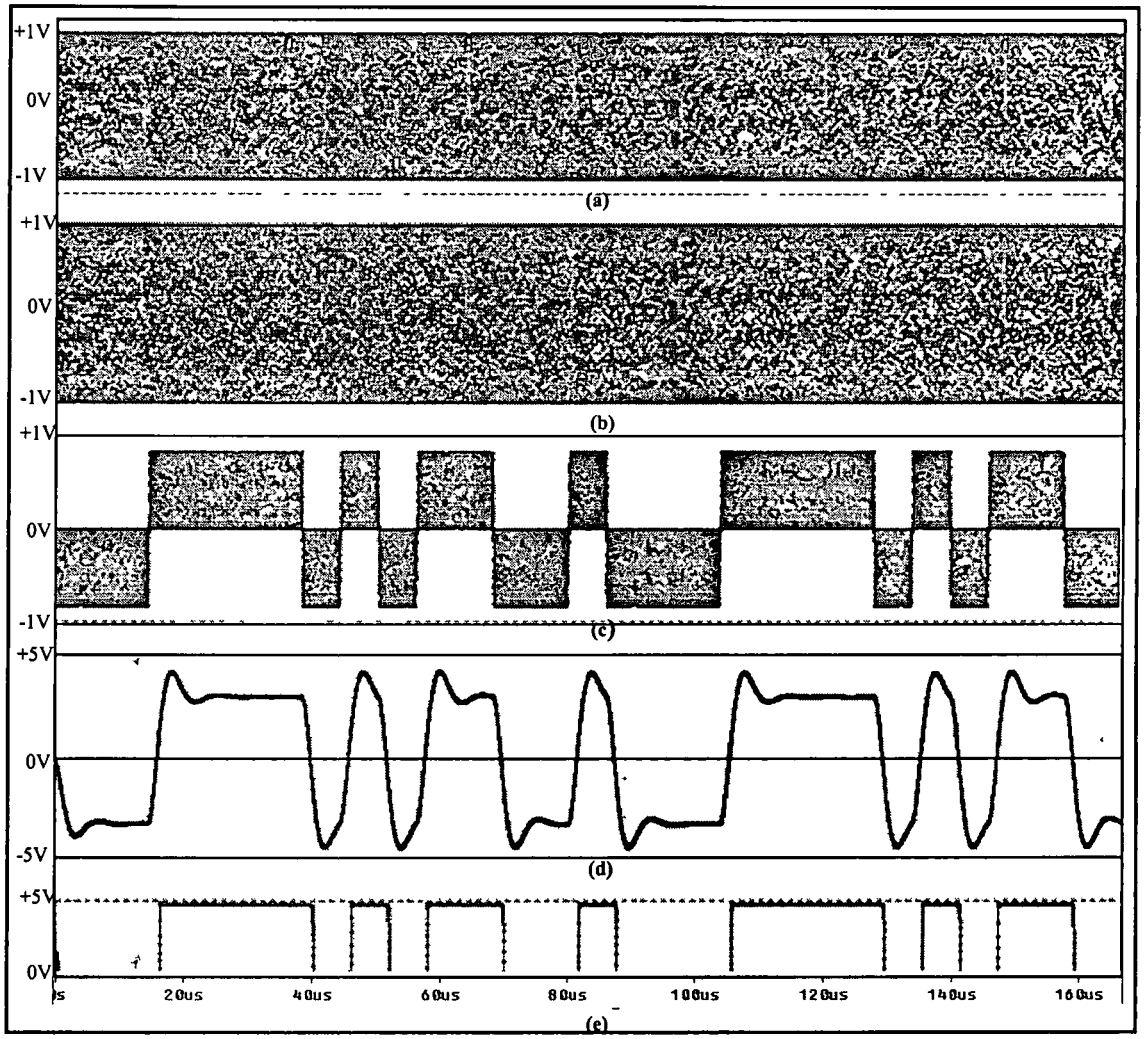


Fig.4.40: P-Spice Simulated Circuit diagram of DSSS receiver at 100 MHz, (a) Input BPSK signal, (b) Local coherent carrier, (c) Output from demodulator, (d) Output from Sallen-Key filter, (e) Output from decision device.

The received and decode PN is processed further in the correlator, integrate and dump, comparator and decoder circuits. The different processed signals through these circuits are shown in the Figure 4.41.

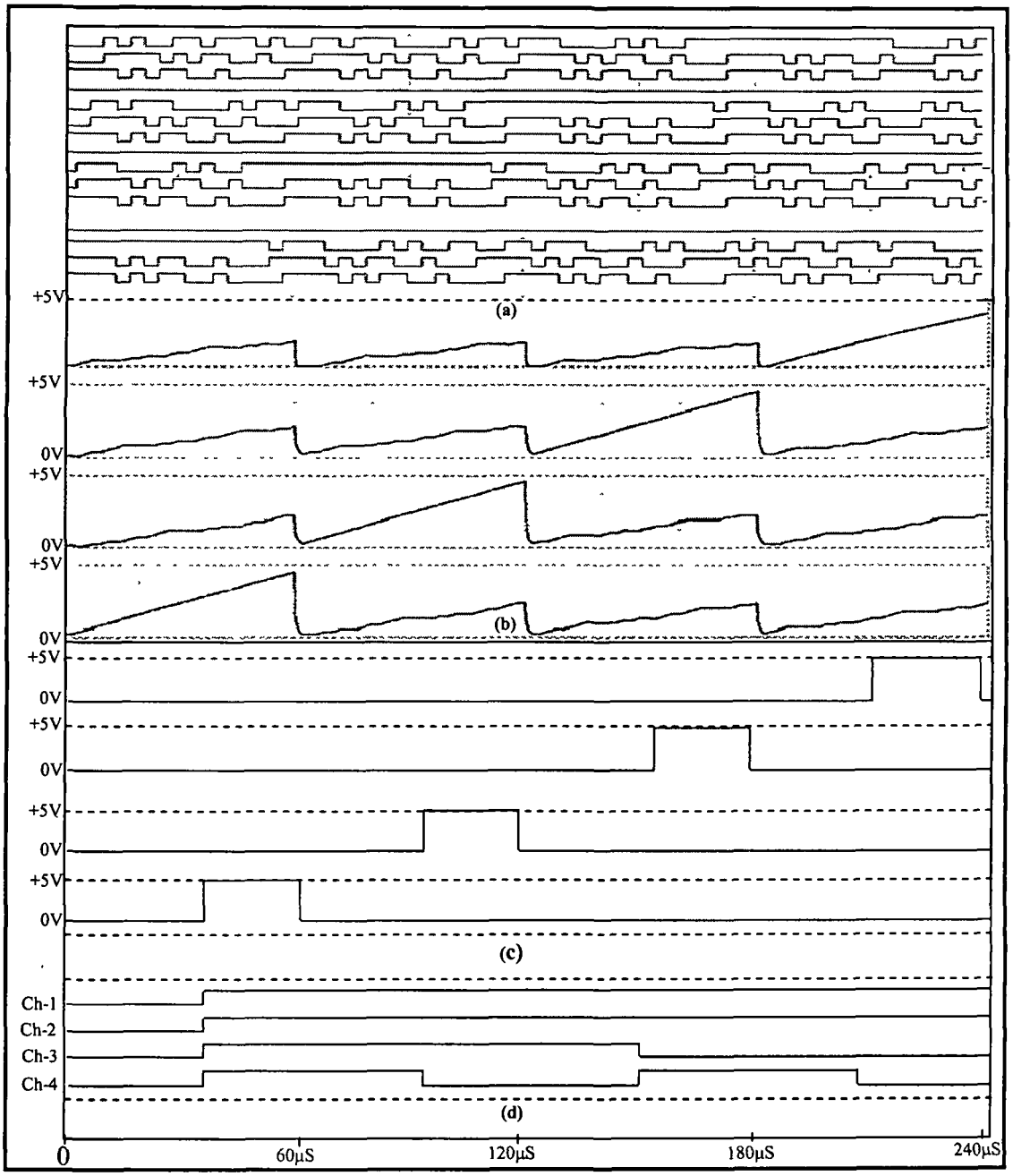


Fig.4.41: Simulated output of receiver at different stages, (a) Output from correlators, (b) Output from integrator and Dump, (c) Output from Comparator, (d) Output from Decoder

In this Figure waveform (a) shows the output and inputs of correlator stage. As seen from traces when received PN sequence matches with one of the received PN sequence the output of corresponding correlator is high for complete PN duration. Waveform (b) shows the output of integrator and dump circuit. It is seen from the waveform that when matched PN is received, the integrator circuit provides high output other wise output is lesser. The output of the Integrator is applied to the comparator as seen from the waveform (c). For matched PN sequence the output of the integrator is higher than the preset value and the particular comparator provides high pulse.

It is seen from the figure that at a time only one comparator provides high output. The output of other comparators is low, because the signal received from integrators stage is less than the preset value of the comparator stage. The output of the comparators is applied to decoder circuit which decodes the input data into four bits and the trace (d) shows the 4-bit output which represents the waveform of decoded 4-channels with delay ~40 μs to 50 μs. This delay is mainly due to propagation delay in components used in the design.

We, have tested the performance of the designed 4-channel CPSK based DSSS transceiver. The performance is tested under noise, additive white Gaussian noise (AWGN) and under jamming condition. For jamming and AWGN performance, measurement setup is used with P-Spice simulation. The performance of this designed of the 4-channel CPSK based DSSS receiver will be discussed in Chapter 5.

4.7 Receiver Design with Proposed BPSK to ASK Converter and Peak Detector

We have proposed a new method for BPSK demodulation by converting the BPSK signal into amplitude shift keying (ASK) and then processing with peak square detector. The succeeding section discusses the proposed BPSK demodulator in details. The block diagram of proposed demodulator is shown in Figure 4.42.

It consists of adder1, 90° phase shifter, squarer1, squarer2 and adder 2 circuits. The input BPSK signal is added in the adder 2 circuit stage with locally generated coherent

carrier signal. The BPSK signal consists of two sinusoidal signals shifted by 180°. Therefore, the output of the adder1 will be ASK signal. The output of adder 1 is applied to the 90° phase shifter and squarer 2 circuits simultaneously. The output of 90° shift shifter is also squared using squarer circuit 1 and applied as one input to adder circuit 2. The other input to adder circuit 2 is obtained from the squarer 2. These both signals are added in this summing circuit and it provides the demodulated output as discussed below.

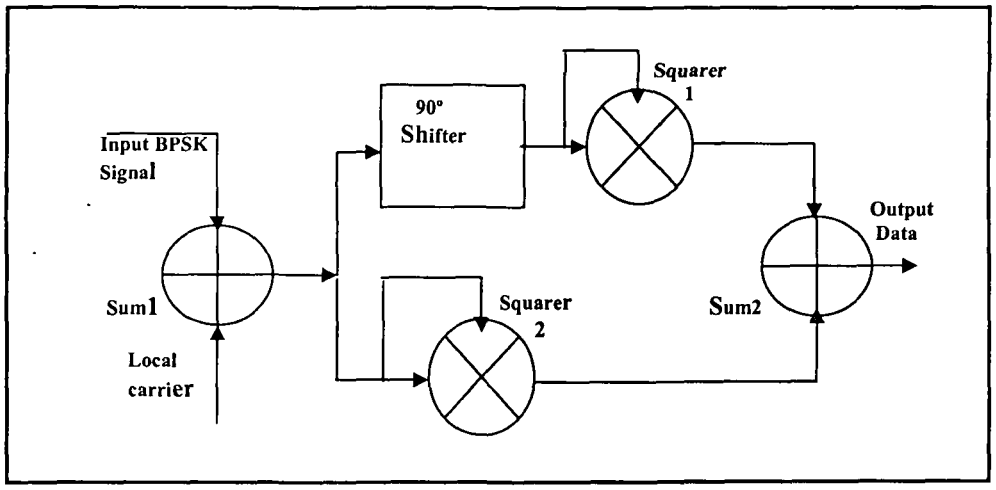


Fig.4.42: Block diagram of proposed BPSK demodulator

The BPSK signal is expressed as:

$$s(t) = V_m m(t) Sin\omega t \qquad 0 \leq t \leq T \qquad (4.16)$$

where V_m is peak magnitude of BPSK signal, m(t) = '-1' or '1', ω=angular frequency, and T= bit duration of the modulating signal. Under coherent demodulation condition, the local input signal to adder 1 will be phase matched with the incoming signal and expressed as:

$$I_{Phase} = V_c Sin\omega t . \qquad (4.17)$$

The signals in Equation (4.16) and Equation (4.17) are added in adder 1 circuit and output is obtained as:

$$s_{ASK}(t) = (V_m + V_c)Sin\omega t \quad \text{(for logic '1')} \quad (4.18)$$

and $$s_{ASK}(t) = (V_m - V_c)Sin\omega t \quad \text{(for logic '0')} \quad (4.19)$$

Assuming the magnitude of local carrier is same as of input BPSK signals such that $(V_c = V_m)$. Therefore, Equation (4.18) and (4.19) are expressed as,

$$s_{ASK}(t) = 2V_m Sin\omega t \quad \text{, for m(t) = '1'} \quad (4.20)$$

and $$s_{ASK}(t) = \text{'0'} \quad \text{, for m(t) = '0'} \quad (4.21)$$

Equation (4.20) and Equation (4.21), represents the ASK signals. This signal is processed as per the remaining blocks of Figure (4.42) and data is extracted.

In the upper arm, the ASK signals, after 90° phase shifting, are squared as $4V_m^2 Cos^2\omega t$, and, applied at one input of adder circuit 2. The other input to this adder circuit is obtained from lower arm as, $4V_m^2 Sin^2\omega t$. These two signals are added in the adder 2, as, $4V_m^2 Sin^2\omega t + 4V_m^2 Cos^2\omega t$, and will provide outputs equal to $4V_m^2$. Therefore, from Equations (4.20) and (4.21) we can write:

$$\text{m(t) = '1'= } 4V_m^2 \quad (4.22)$$

$$\text{m(t) = '0'= 0Volt} \quad (4.23)$$

The design of demodulator is discussed in the following section.

4.7.1 Adder 1

Adder1 adds the received CPSK based DSSS signal which are the BPSK signals with locally generated coherent carrier signals. It consists of an operational amplifier configured as a non inverting summer with unity feed back as shown in Figure 4.43, using high speed integrated circuit AD8001A/AD [24]. Figure 4.44 shows the input and output waveforms of the adder1 circuit.

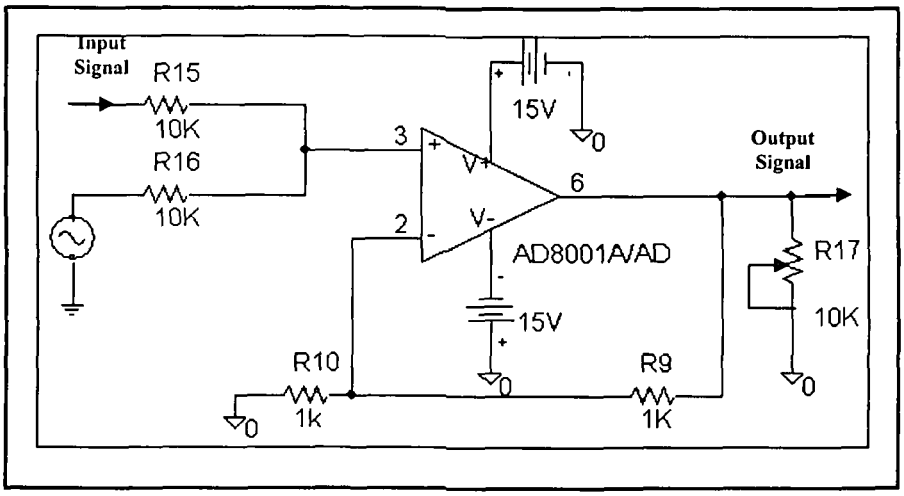


Fig.4.43: Simulated circuit diagram of adder1 [28]

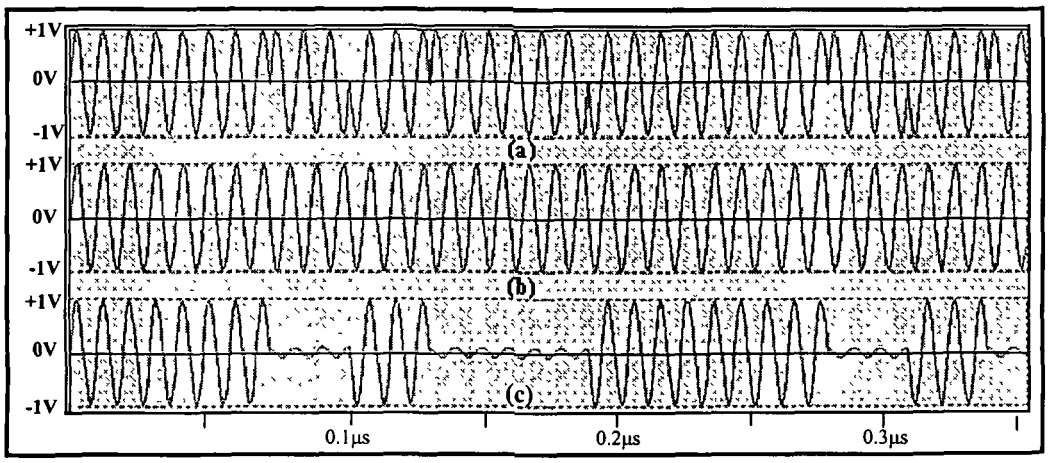


Fig.4.44: Simulated waveform, (a) Input BPSK signal, (b) Local coherent carrier, (c) Output from adder 1

As seen from the Figure 4.44, trace (a) shows the incoming 100MHz BPSK signal and trace (b) shows the local coherent carrier signal at the same frequency. As seen from trace (a) the BPSK signal with consists of two signals one in phase and other 180 degree output of phase with the coherent carrier signal. When both the input signals are in the same phase they get added up and the after addition the magnitude of the output becomes double. At the same when they are output of the phase they cancel out each other and zero output is obtained at the output. As a result, the BPSK signal is converted

into the ASK signal as shown by tracing (c). If the amplitude of the signals are not equal then also output will be ASK signal only.

4.7.2 90° Phase Shifter

To provide the 90° phase shift to signals obtained from the summer 1, we have used all pass filter which provides the required phase shift with unity gain as no attenuation to input signals [28]. The required phase shift is obtained using the expression given in Equation 4.24 by varying the value of resistance (R) and capacitor (C). At an operating frequency of 100 MHZ, a resistance of 160 Ω and capacitor of 10pF gives the required phase shift of 90° to the incoming signal. The software simulated circuit diagram of 90 ° phase shifter is shown in Figure 4.45.

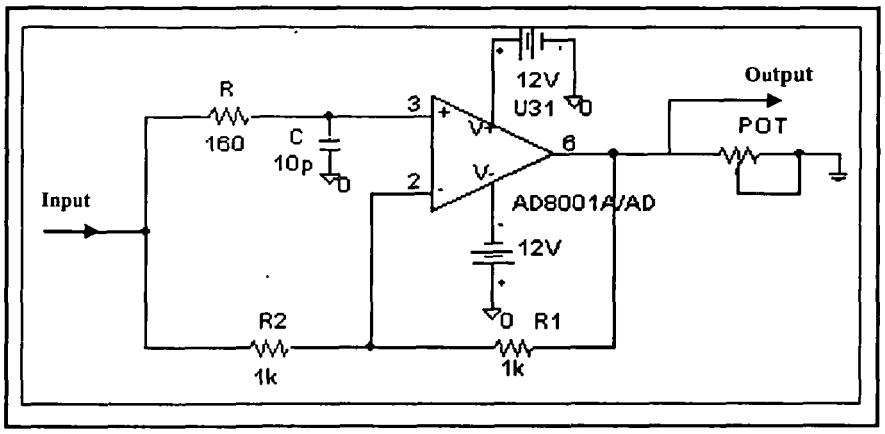


Fig.4.45: Simulated circuit diagram of all pass filter [28]

The Figure 4.46 shows the simulated input and 90° phase shifter signals at 100MHz. The trace (a) shows the input signal and trace (b) shows the 90° phase shifted signal.

$$\phi = -2\tan^{-1}(\omega RC) \qquad (4.24)$$

where ω is the frequency of input signal in rad/sec. R and C the resistance and capacitor in ohms and farads. The value of phase shift (ϕ) is in degree.

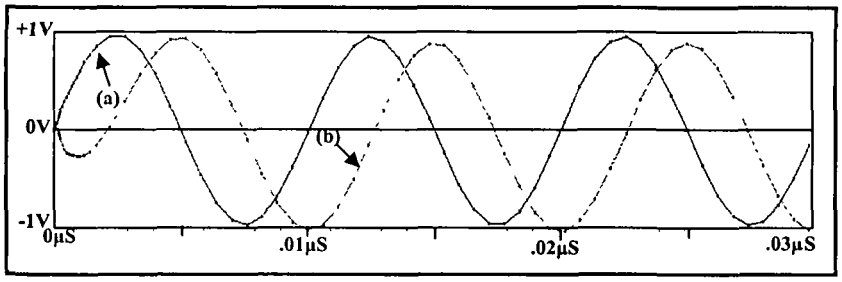


Fig.4.46: Simulated circuit diagram of all pass filter,
(a) Input signal, (b) Output signal delay by 90°

4.7.3 Squaring Circuits

Squaring 1 and squaring 2 circuits squares the output signal of 90° phase shifter and from summer 1 respectively. These are analog multipliers and provide a signal at its output terminal equal to square of input signals. In the proposed circuit the squaring 1 and squaring 2 circuits are realized using high speed amplifier integrated circuit AD834/AD. Its details are given in section 4.3.2 for BPSK modulator design.

4.7.4 Adder 2

The adder 2 circuit adds the signal obtained from the squaring circuit 1 and squaring circuit 2. The circuit is implemented using integrated circuit AD8001A/AD as discussed in Section 4.7.1. Therefore, same circuit as discussed in Figure 4.43 for adder 1 is used for adder 2. Figure 4.46 shows the simulated input and output waveforms for this circuit. Trace (a) and trace (b) show the output obtained from squaring circuit 1 and squaring circuit 2. Trace (c) shows the output of the adder 2 stages. The trace (d) shows the transmitted PN sequence and received PN sequence. The signal obtained at the output of Adder 2, is the demodulated PN sequence.

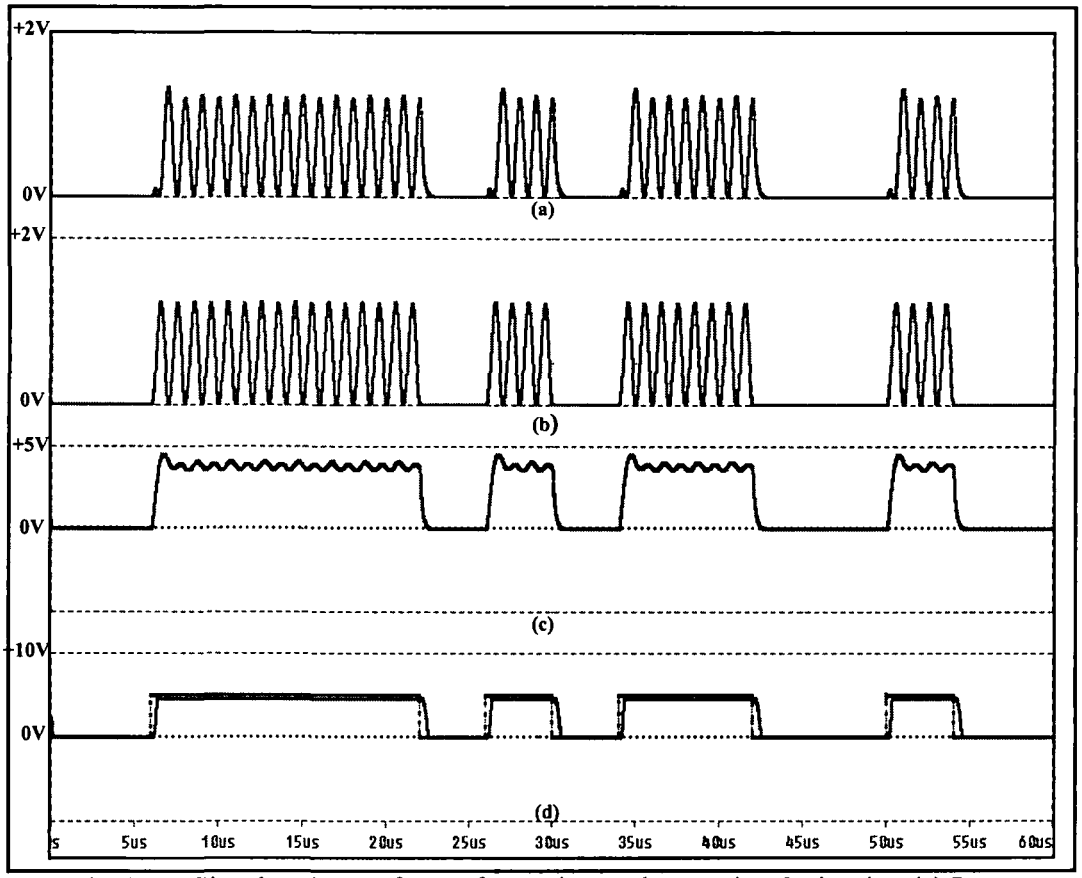


Fig.4.47: Simulated waveform of squaring and summing 2 circuits, (a) Input from squarer 1, (b) Input from squarer 2, (c) Output from summing Circuit 2, (d) Transmitted and received PN sequence.

The proposed demodulator has been designed and the transmitted PN sequences are decoded at this stage. In the next stage the received PN sequences are processed for further detection and translation into transmitted data word. These all stages are same as discussed in the design of the receiver with coherent multiplier. These stages are discussed in Section from 4.5.3 to Section 4.5.6. Therefore, these blocks are not discussed here. However, the complete CPSK based system has been simulated with this proposed BPSK demodulator.

4.8 Simulation Result of CPSK Receiver with Proposed BPSK to ASK Converter and Peak Detector

We have designed and simulated the CPSK based DSSS multiplexed receiver for receiving the signal transmitted by the transmitter. In this design we have used our proposed BPSK to ASK converter for demodulating the DSSS signal for decoding the signals of 4-channels/users. Table-4.6 shows the components with specification used for receiver circuit simulation.

Table- 4.7 Simulated Component list for proposed DSSS receiver

Block	Type	Value
Demodulator	Op-Amplifier-03 No	AD8001A/AD
	Multiplier -02 No	AD834
	Capacitor- 01 No	10pF
	Resistance -15 No	Different values
Correlator	EX-NOR gate -04No	CD74HC7266
Integrate and Dump	Resistance-15 No Resistance -15No Resistance -15 No Pot meter- 15No	2KΩ , 0.25 Watt 1KΩ. 0.25Watt 2KΩ, 0.25Watt 10KΩ, 0.5Watt
	Capacitor-15No	01μF, 100Volt
	Switching Transistor- 15No	2N2222
Comparator	Op-Amplifier -15	AD811/AD
Decoder	8-Input OR gates-04	M78HC4078

The simulated block diagram and simulated circuit diagrams have been shown in Figure 4.48 and Figure 4.49 respectively. The different waveforms obtained from simulations of the designed and proposed circuits are shown in the Figure 4.50 and Figure 4.51.

In Figure 4.50, waveform (a) shows the input BPSK signal with a level of 1Volt and at frequency of 100MHz. The waveform (b) shows the local carrier with amplitude of 1 volt and at channel frequency of 100MHz which is considered as have perfectly matching with the received DSSS signal. Waveform (c) shows the output from the adder 1 circuit which converts the BPSK signal into ASK signal. The waveform (d) shows the output of adder 2, which is the demodulated signal as expressed by Equations: (4.22) and (4.23) respectively. The waveforms show some ripples which can be removed with the help of filters. Finally, the waveforms (e) and (f) show the decoded and transmitted PN sequences. These received PN sequences are further processed and waveforms are shown in the Figure 4.51.

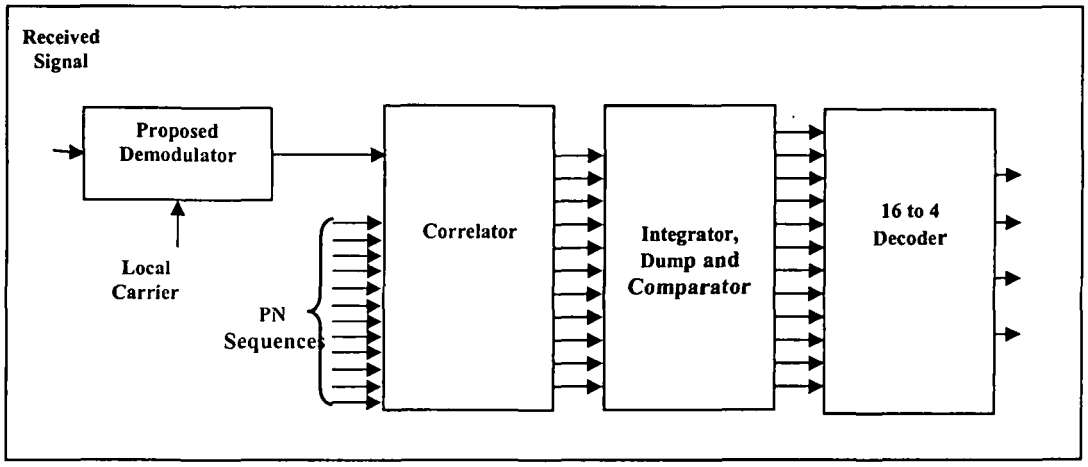


Fig. 4.48: Simulated block diagram of DSSS receiver

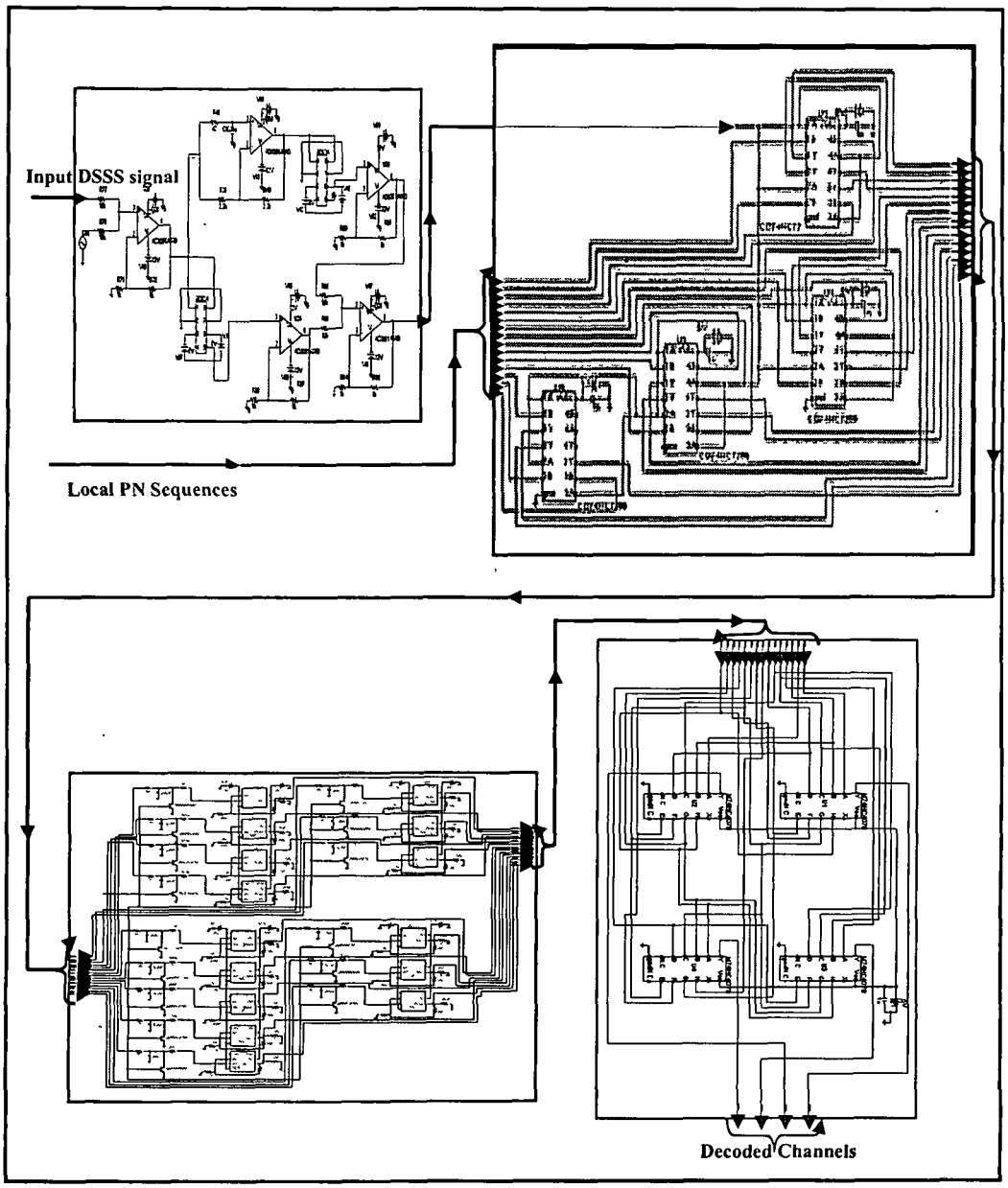


Fig4.49: Simulated circuit diagram of Proposed BPSK demodulator based DSSS receiver circuit diagram

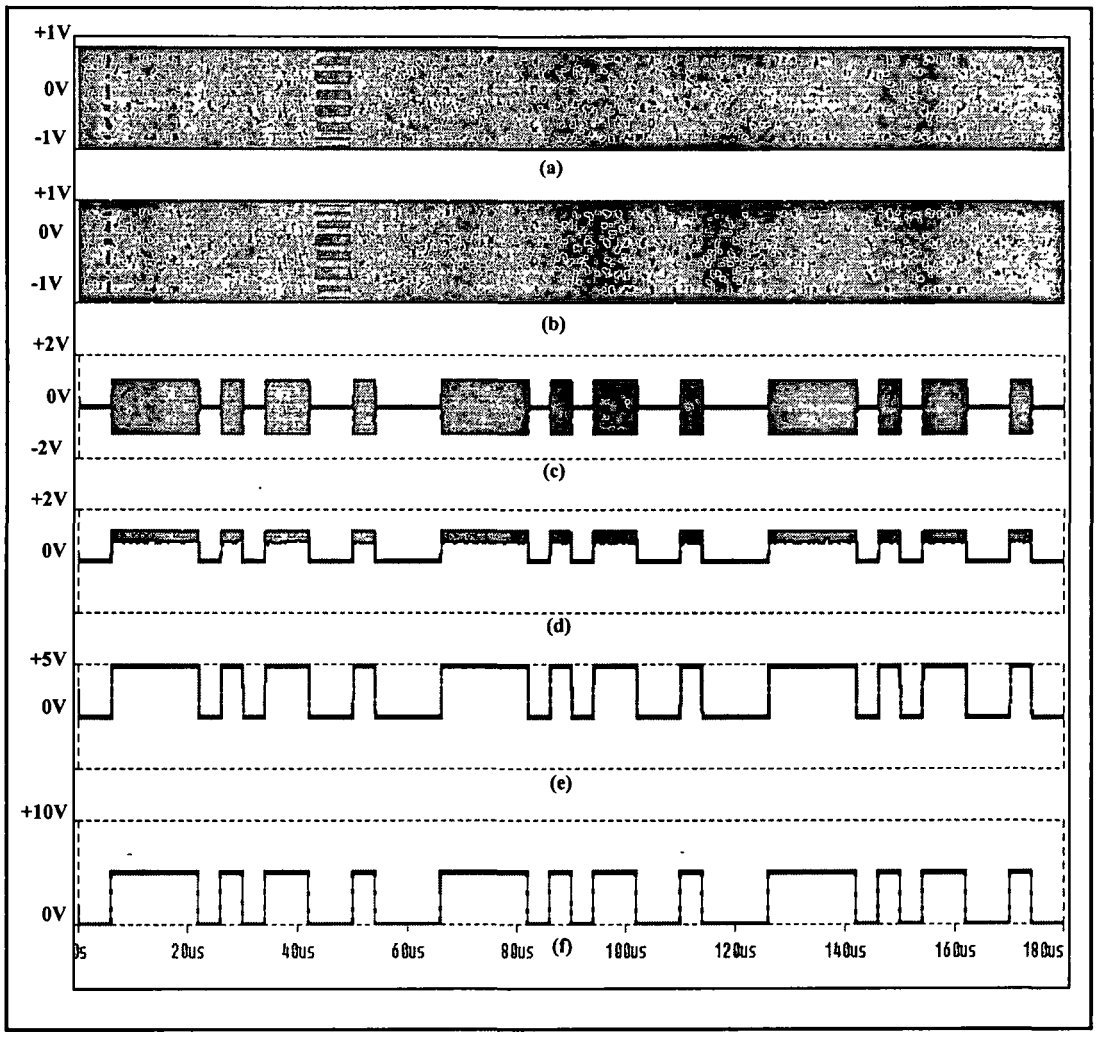


Fig.4.50: Simulated waveforms of proposed demodulator at different stages (a) Input DSSS signal at 100MHz, (b) Local carrier at 100MHz, (c) Output from Sum1, (d) Output from Sum 2, (e) Received PN sequence, (f) Transmitted PN sequence

The waveforms shown in Fig.4.50 and Fig.4.51 are as similar as discussed in Section 4.6. But the time delay of the separated waveforms for four channels is ~ 45-55 μs, which is slightly more than that of the transceiver using conventional BPSK demodulator. As discussed earlier in Chapter 1, for improvement of the performance the proposed BPSK demodulator has been used. In the next Chapter, the improvement of the performance by the proposed demodulator is shown.

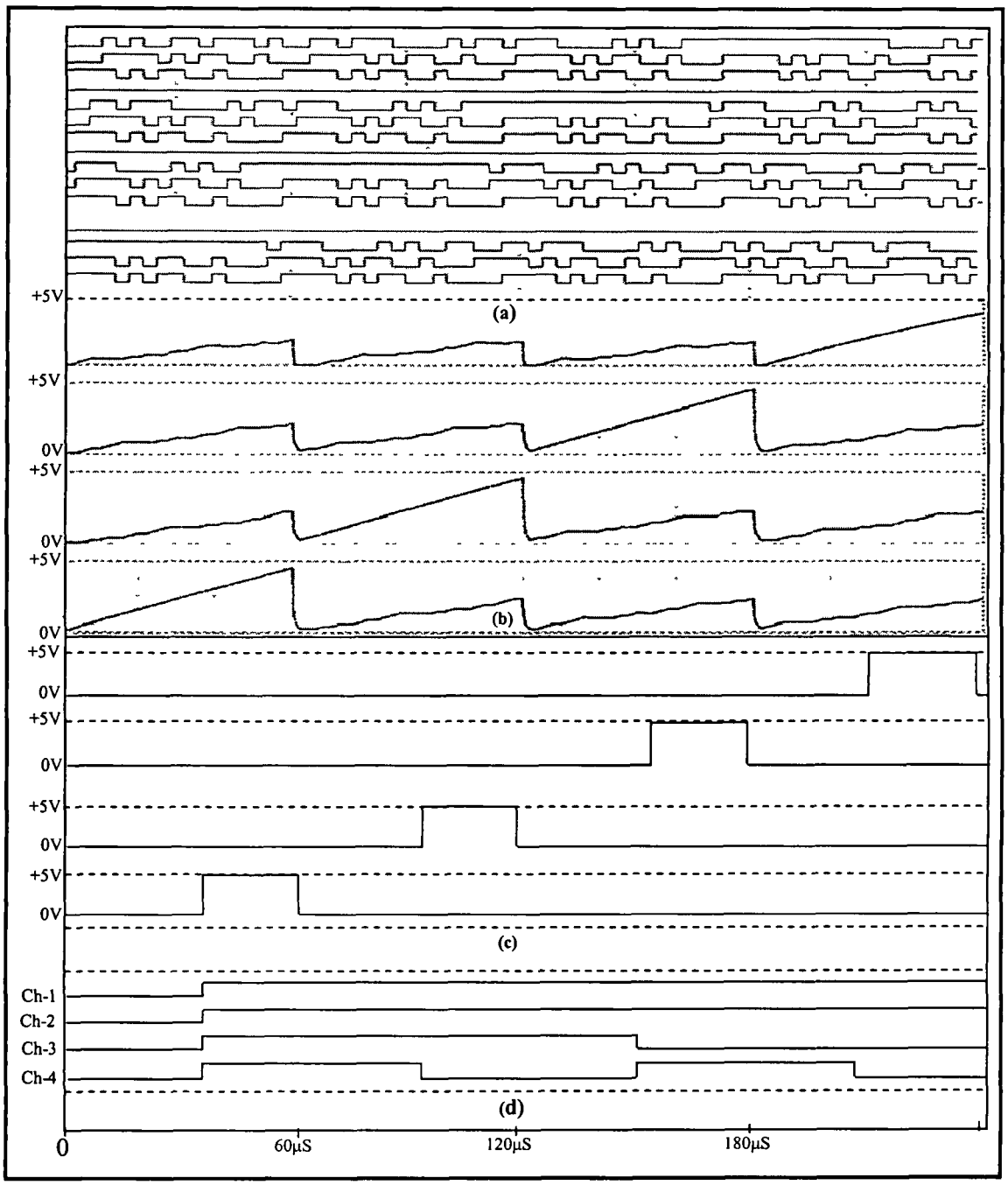


Fig.4.51: Simulated waveforms of receiver at different stages, (a) Output from correlators, (b) Output from integrator and dump, (c) Output from comparator, (d) Output from decoder as 4 channels

4.9 Conclusion

In this chapter, we have discussed the design and simulation of the proposed multi channel CPSK based DSSS transceiver for multiplexing four users at 100 MHz carrier frequency with PN duration of 60 μs using CPSK based DSSS technique. The proposed circuits have been simulated using P-Spice software Microsim Version 8 by using the components shown in tables 4.4 and 4.7. Multi-channel DSSS receiver based on proposed BPSK demodulator also has been designed and simulated to improve the performance (under AWGN). It is seen that the signal of four transmitted channel are separated with delay~ 40 -55 μs. The performance analysis of BER/ SER, Phase mismatch and noise margin /distortion for the proposed and designed DSSS has been discussed in next Chapter 5.

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Chapter 5

Performance Evaluation of CPSK based DSSS System

5.1 Introduction

In chapter 4, CPSK multi-channel DSSS system has been proposed, designed and simulated. It is essential to analyze the performance of the designed system for various for bit error rate (BER) and jamming error rate (JER) [1]-[3]. In this Chapter, we have tried to study the performance of the proposed system both analytically and with simulation models. Noise is the main source of performance degradation for any wireless system [4]-[7]. The proposed system is simulated for its BER and jamming performance under varying signal to noise ratio.

Further, this chapter is organized as follows. Section 5.2 presents a theoretical evaluation of bit error rate (BER) performance of the designed DSSS system under Additive White Gaussian Noise (AWGN) and jamming. The DSSS device was tested with simulation model under different AWGN condition [8]-[10]. The simulation results are discussed in Section 5.3. Section 5.4 presents the performance of proposed BPSK demodulator analytically. Section 5.5 shows the performance measurement by eye pattern. Experimental results are shown in Section 5.6. Finally, the conclusion is presented in Section 5.7.

5.2 Analytical Performance Evaluation

It is important to evaluate the performance of wireless devices by considering the transmission characteristics, wireless channel parameters and device structure. The performance of data transmission over wireless channels is well captured by observing their BER, which is a function of SNR at the receiver. So we will study the performance of designed device under AWGN, jamming and phase mismatch [11-12].

5.2.1 Performance under AWGN

The designed multi-channel DSSS transmitter generates the BPSK signal obtained after multiplication of coded pseudorandom (PN) sequence with carrier frequency $Cow(\omega_c t)$

and sent over the channel to the receiver as discussed in Chapter 4, Section 4.3.2. The modulated signal obtained from the output of the transmitter is written as [1]:

$$x_c = AC(t)\cos(\omega_c t) \tag{5.1}$$

In the channel this signal is corrupted with AWGN $n(t)$ and narrow band jamming signal $j(t)$ [13]-[16]. At the receiver, the received signal can be expressed as:

$$z(t) = x_c(t) + n(t) + j(t) \tag{5.2}$$

Let the local carrier is perfectly synchronized in phase and frequency, the demodulated BPSK signal at the output is given as [16]-[18]:

$$x_c = A\ C(t)\cos^2(\omega_c t) + n(t)\cos\omega t + j(t)Cos\omega(t) \tag{5.3}$$

After passing through the low pass filter, the second and higher frequency harmonic components are attenuated and output of the low pass filter is written as:

$$X_c = AC(t) + n'(t) \tag{5.4}$$

$$\text{where } n'(t) = 2n(t)C(t)Cos\omega_c t \tag{5.5}$$

Equation (5.5) is a Gaussian random process with zero mean [19]-[21]. These signals after passing through integrate and dump circuit (correlator also) for bit duration T_b, provides an output signal as:

$$V_o = \pm AT_b \tag{5.6}$$

The noise component at the integrator output is:

$$N_g = \int_0^{T_b} 2n(t)C(t)Cos(\omega_c t)dt \tag{5.7}$$

Since noise is a random variable with zero mean, the N_g also has zero mean. Its variance, which is the same as its second movement, and given as:

$$\text{var}(N_g) = E(N_g^2) = N_o T_b \tag{5.8}$$

N_o is the single sided power spectral density of the input noise. This with the signal, component of the integrator output provides a signal power equal to $\frac{A^2}{2}$.

Therefore, the bit error rate of the system is given as:

$$P_E = Q\sqrt{\frac{A_2 T_b}{N_o}} = Q\sqrt{\frac{2E_b}{N_o}} \tag{5.9}$$

Equation 5.9 shows that under AWGN condition, DSSS system also provides the same BER performance as a BPSK system [19].

Figure 5.1 shows the plot for the BER performance of BPSK system and DSSS system. Both the plots overlap each, other and show the same performance in AWGN environment. It has been seen from the Figure that BER increases as the E_b/N_o decreases.

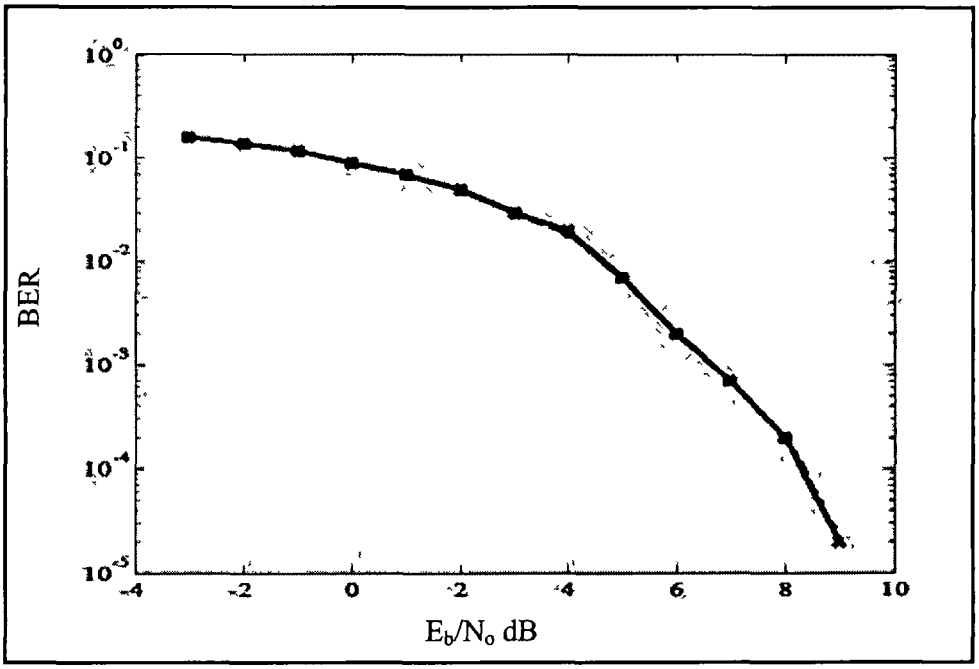

Fig.5.1: Analytical performance of BPSK System and DSSS system

5.2.2 Performance in AWGN with Continuous Wave Jamming

For performance analysis, of the DSSS system, the interfering signal at the input of the receiver is written as [3]:

$$Z_I(t) = Ad(t)Cos(\omega_c t) + n(t) + A_I Cos(\omega_J + \theta_J) \tag{5.10}$$

The signal is processed in the demodulator stage and assuming perfect code synchronization, the input to integrate and dump circuit, leaving the double harmonic components due to multiplication is expressed as:

$$Z_I' = Ad(t) + n'(t) + A_I Cos(\Delta\omega t) \tag{5.11}$$

where A_I is the amplitude of the continuous wave interfering component and $\Delta\omega$ is its offset frequency from the carrier frequency. The output from integrate and dump circuit is written as:

$$V_o' = \pm AT_b + N_g + N_I \tag{5.12}$$

The last term is due to the interference and defined as:

$$N_I = \int_0^{T_b} A_I C(t) Cos(\Delta\omega) dt \tag{5.13}$$

This term is approximated by multiplication of PN sequences and subsequent integration, as a random variable equivalent to Gaussian random variable [20]. Therefore, the mean is zero, and for $\Delta\omega << \frac{2\pi}{T_c}$, the variance will be as:

$$\text{var}(N_I) = \frac{T_c T_b A_I^2}{2} \tag{5.14}$$

With the Gaussian approximation with N_I, the probability of error is given as:

$$P_E = Q\left(\sqrt{\frac{A^2 T_b^2}{\sigma_T^2}}\right) \tag{5.15}$$

where $\sigma_T^2 = N_o T_b + \frac{T_C T_b A_I^2}{2}$

Further manipulating the Equation (5.14) [4] as:

$$\frac{A^2 T_b^2}{2\sigma_T^2} = \frac{\frac{A_I^2}{2}}{\frac{N_o}{T_b} + \left(\frac{T_c}{T_b}\right)\left(\frac{A_I^2}{2}\right)}$$

$$= \frac{P_s}{P_n + \frac{P_I}{G_p}} \tag{5.16}$$

where $P_s = \frac{A^2}{2}$ is the signal power at the input.

$P_n = \frac{N_o}{T_b}$ is the Gaussian noise power in the bit-rate bandwidth.

$P_I = \frac{A_I^2}{2}$ is the power of the interfering component at the input.

$G_p = \frac{T_b}{T_c}$ is the processing gain of the DSSS system.

Re-arranging the Equation (5.16) as:

$$\frac{A^2 T_b^2}{2\sigma_T^2} = \frac{SNR}{1 + \frac{(SNR)(JSR)}{G_p}} \tag{5.17}$$

From Equation (5.17), [4] it has been seen that the effects of the interfering components resulted by tone jammer are decreased by the processing gain G_p. Figure 5.2 shows the BER versus SNR for JSR values of 10dB, 15dB, 20dB and 25 dB by Equations 5.14 to 5.17.

It has been seen from the Figure that the probability of error decreases with more SNR and the rate of decrease of probability of error is low for higher JSR. It is because of more jamming signal that causes the signal power at the output of integrator circuit to decreases. With this, the decision device takes a wrong decision which provides more error. The overall system performance gets degraded.

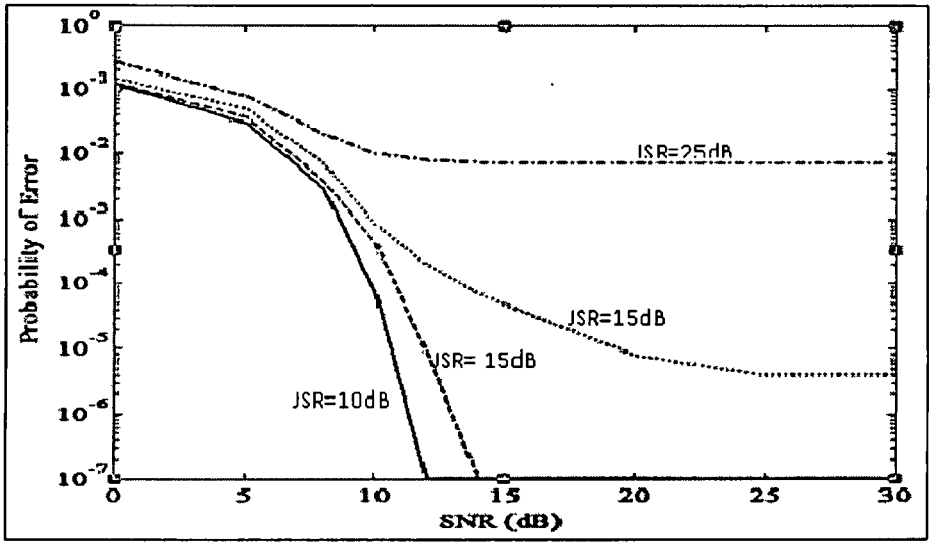

Fig.5.2: Jamming Performance with processing gain

5.2.3 Performance with Phase Mismatch

In coherent BPSK demodulation [14], [19] the demodulator is able to locally generate the carrier with correct phase and frequency. To this end, the coherent receiver tracks the carrier by using a carrier recovery circuit; generally Costas loop is used for carrier synchronization [20]. When both the signals are not synchronized system degrades the performance as discussed below:

In BPSK system the signals are given as:

$$x_c = AC(t)\cos(\omega_c t) \tag{5.17}$$

At the input of the receiver, the signal is mixed with AWGN received signal from the channel as:

$$z(t) = x_c(t) + n(t) \tag{5.19}$$

At the multiplier the received signal is multiplied with local signal as:

$$\begin{aligned} Z_1(t) &= AC(t)Cos(\omega_c t)Cos(\omega_o t + \phi) + n(t)Cos(\omega_c t + \phi) + n(t) \\ &= \frac{AC(t)}{2}[(1 + Cos2\omega_c t)Cos\phi] - \frac{AC(t)}{2}[(Sin2\omega_c t)Sin\phi] + n'(t) \end{aligned} \tag{5.20}$$

where

$$n'(t) = 2n(t)Cos(\omega_c t + \phi) \tag{5.21}$$

After passing through the integrate and dump circuit, the signal component is given as:

$$= \pm \frac{AC(t)}{2}[Cos(\phi)] \tag{5.22}$$

Based on this condition, the energy of the received signal for bit duration becomes as $\frac{1}{2}ET_bCos^2\phi$. Therefore, expression for BER is written as:

$$Pe = \sqrt{\frac{ET_b}{\eta}Cos^2\phi} \quad \text{or} \quad Pe = Cos\phi\sqrt{\frac{ET_b}{\eta}} \tag{5.23}$$

It is clear from Equation (5.23) that under mismatch condition angle ϕ will have non zero value and this value will decrease the energy available in the bit duration. Therefore, the energy of signal obtained from the integrator circuit will decrease as seen from the equation. The overall BER performance of the system also will degrade as discussed below. Figure 5.3 shows the variation of BER for local carrier phase and the received signal phase mismatch [20].

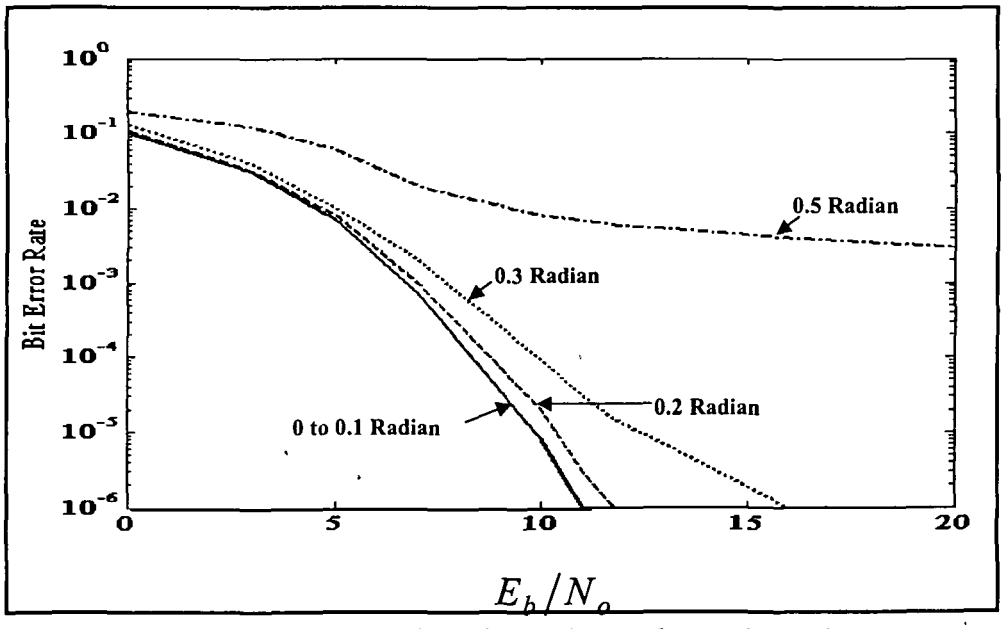

Fig.5.3: BER degradation due to phase mismatch

It is seen from the plot that when deviation of phase angle is smaller or equal to 0.1 radian, this does not produce any appreciable degradation in the BER. With a deviation of phase equal to 0.2 also degrades the performance of the system. However, as deviation in phase equal to 0.3 radian, plot shows appreciable degradation in the performance. To have a BER performance of 10^{-5} as obtained at 10dB for perfect phase matching; it requires an increase of SNR by 3dB for 0.3 radian deviation in the carrier phase mismatch. Also, it has been seen from the Figure 5.3 that with deviation in phase by 0.5 radian has degraded the BER performance. Even increasing the SNR does not improve the system performance much.

5.3 Performance Evaluation with Simulation Setup

In digital communications bit error rate (BER) is expressed as the rate at which errors occur in a transmission system. BER is the ratio of error-bits received to the total bits sent [8]-[10]. In case of M-ary digital communication [17]-[18], symbols are transmitted and each symbol represents a unique sequence of bits. The performance analyses are estimated with symbol error rate (SER). It is defined as the total number of erroneously decoder information symbols divided by the total number of transmitting symbols [8]. The BER performance of the system can be calculated from the SER using their relation.

Consider a K-bit symbol is received with error, it may be that 1 bit or 2 bits or that all K bits are in error. If we assume that the probability P_e, of receiving any of these erroneous symbols is the same. To assess the noise performance of a digital pass band transmission system, the average probability of the symbol error system is used. Therefore, BER is written in terms of SER as [8].

$$BER = SER\left(\frac{2^{K-1}}{2^K - 1}\right) \tag{5.24}$$

Figure 5.4 shows the block diagram of simulation model BER/SER analysis. Simulation model consists of data generator, CPSK [18] transmitter, CPSK demodulator, AWGN

generator (2 kHz–150 MHz), and jamming signal generator, and comparator. The data generator generates the signal of four channels and CPSK transmitter modulates the signal at the carrier frequency of 100 MHz. AWGN generator produces noise, which is mixed with CPSK signal from mixer circuit. The generated jamming signal is then mixed with CPSK signal in the mixer stage. The output from the mixer is applied to CPSK demodulator. CPSK demodulator processes the signal and decodes back to the data as transmitted but with some delay. This delay is the processing time took by the different stages in the receiver. For SER calculation using the simulation model is shown in the diagram in Figure 5.4.

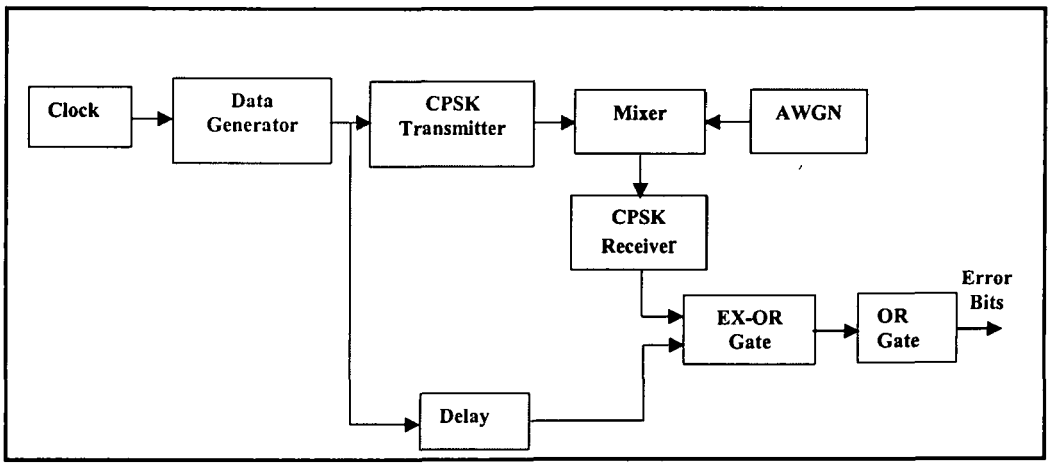

Fig.5.4: Simulation model for SER/BER estimation

It is required that both the transmitted and received signals should be phase matched perfectly. Therefore, a delay is introduced in the transmitted signal and both the transmitted and received data are phase matched before applied to EX-OR gates [21]-[22]. An EX-OR gate gives high output for dissimilar inputs and low output for similar inputs. The high bits available at the output of EX-OR gate show the error. By counting these bits, total number of error symbols with error bits is estimated. By dividing these symbols to the total number of transmitted symbols, SER is determined. BER is estimated from SER using Equation (5.24).

We have simulated the complete circuit of CPSK based 4-channels DSSS system using P-Spice software Microsim Version 8.0 for performance evaluation under AWGN and the simulated circuit diagram is shown in the Figure 5.5.

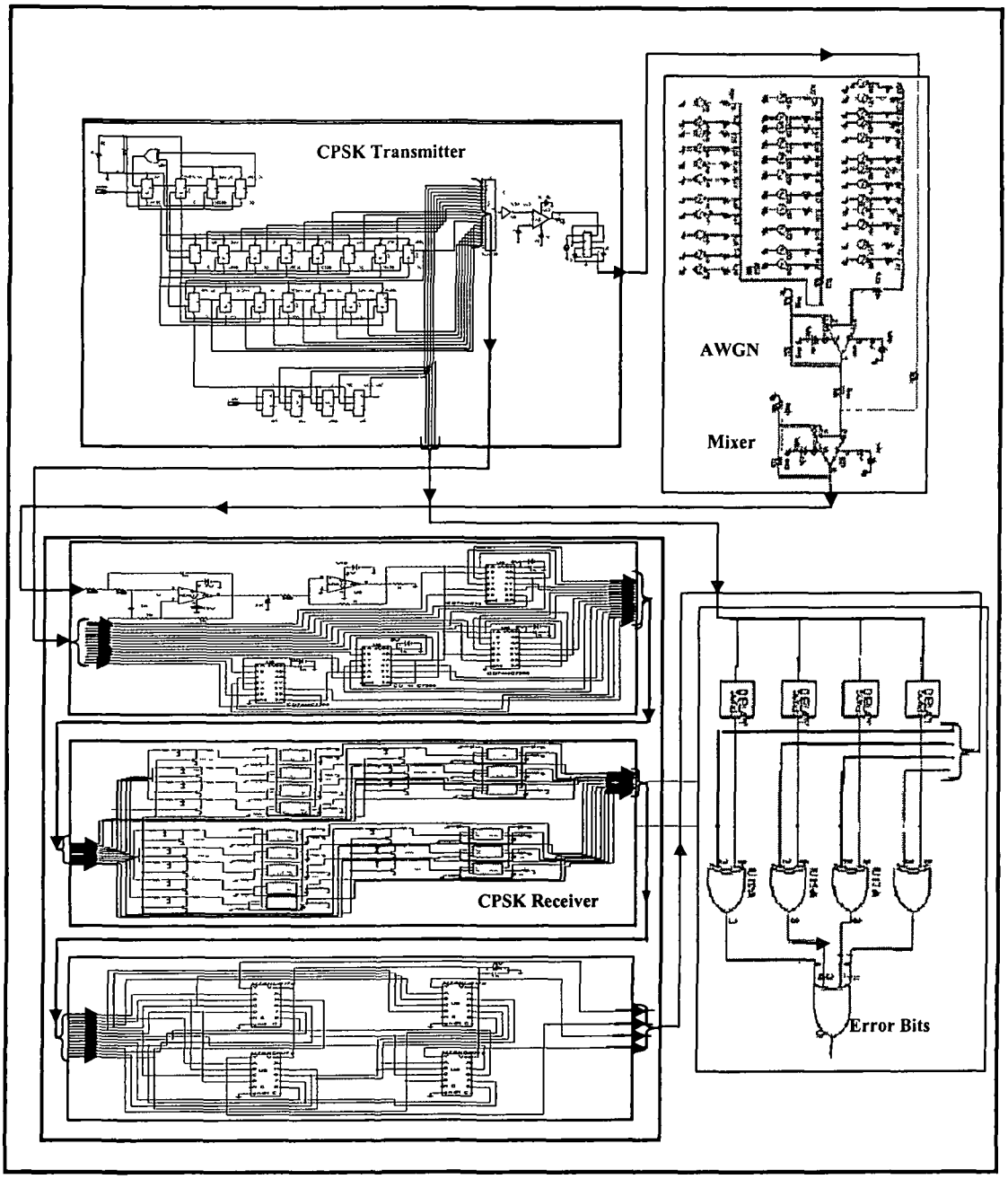

Fig.5.5: P-Spice simulated circuit diagram for SER estimation

5.3.1 Bit Error Rate Measurement

For measuring the performance of the CPSK based 4-channel DSSS receiver, the block diagram for simulation model is shown the Figure 5.4. The simulated output signal of the transmitter at the carrier frequency of 100 MHz and simulated noise from the AWGN noise source are added to the summing circuit as per the block diagram. The complete P-Spice simulated circuit diagram for BER/SER estimation is given in Figure 5.5 As discussed above the BER is calculated using Equation 5.24 for the proposed circuit by varying the signal to noise ratio and the plot is given in Fig- 5.6 for the same. Simulated results obtained from simulation model for our designed 4 channel CPSK based DSSS systems are compared with the field programming gate array (FPGA) based CPSK DSSS system [17].

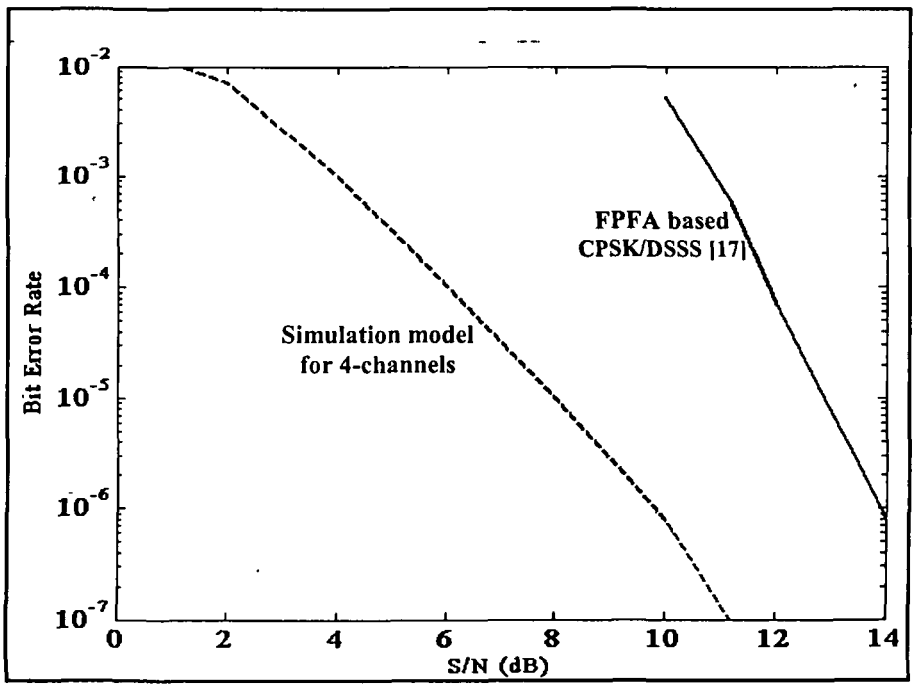

Fig.5.6: Comparisons of BER performances between CPSK/DSSS using simulation model and with the FPGA based CPSK /DSSS [12]

As seen in the Figure 5.6, the BER performance is degraded when SNR decreases in both the DSSS systems. The BER performance of four-channel CPSK/DSSS system is better than that of FPGA based CPSK/DSSS system [17].

5.3.2 Jamming Performance from Simulation Model

The BER performance is analyzed when the predefined data patterns sent by transmitter mixed with the jamming signals. For BER analysis under jamming, we have taken SNR 4, 12, and 14 dB. Figure 5.7 shows the variation of BER with jamming to signal ratio (JSR) in case of four-channel CPSK/DSSS circuit with our simulation model of carrier frequency fc = 100 MHz. It is evident from the figure that the BER increases with JSR for all SNR. As SNR decreases, the system is more tolerant to the jamming signal. When there is no jamming, the BER is 1.5×10^{-5} at an SNR of 8 dB. With the introduction of jamming signal, the BER is increased to 3.2×10^{-3} and 8×10^{-3} at JSR of -11dB and -8 dB, respectively. The cross sign represents experimental results which are discussed in Section 5.6.

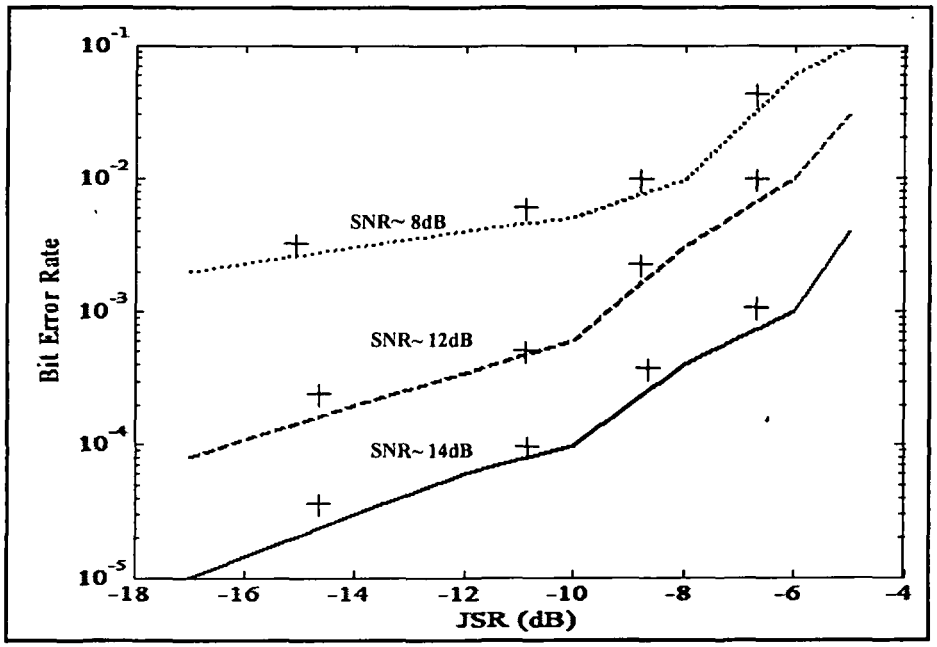

Fig. 5.7: Jamming performance with simulation model

5.4 Performance of Proposed BPSK Demodulator

In literature many techniques are proposed for BPSK demodulation [24]-[27]. In Chapter 4, we have discussed out proposed technique for BPSK signal demodulation using BPSK to ASK converter and 90 degree phase shifter. Figure 4.41 in Chapter 4 shows the block diagram of proposed demodulator. The BER performance of the circuit is derived in the presence of AWGN. We have discussed in Section 4.7 in Chapter 4 that the received DSSS signal is applied to the proposed BPSK demodulator. From Equation (4.22) and Equation (4.23), the received BPSK signal is converted into ASK and it can be written as:

$$s_{ASK}(t) = 2V_m Sin\omega t \quad \text{, for m(t) = '1'} \tag{5.25}$$

$$s_{ASK}(t) = \text{'0'} \quad \text{, for m(t) = '0'} \tag{5.26}$$

The output of summing circuit 2 (Figure 4.42) can be written as: $4V_m^2$ for logic '1' and '0' for logic '0', which is normalized power of the detected signal.

We know that the probability of error of the optimum filter is given as [23],

$$P_e = \frac{1}{2} erfc\left[\frac{x_{o1}(T) - x_{02}(T)}{2\sqrt{2\sigma}}\right] \tag{5.27}$$

$$\text{Where, } \left[\frac{x_{o1}(T) - x_{02}(T)}{\sigma}\right]^2_{max} = \int_{-\infty}^{\infty} \frac{|X(f)|^2}{S_{ni}(t)} df \tag{5.28}$$

Considering the AWGN, the power spectral density of white Gaussian noise is given as [23]:

$$S_{ni}(f) = \frac{N_o}{2} \tag{5.29}$$

Substituting this value of $S_{ni}(f)$ in Equation (5.28), we get,

$$\left[\frac{x_{o1}(T) - x_{02}(T)}{\sigma}\right]^2_{max} = \frac{2}{N_o} \int_{-\infty}^{\infty} |X(f)|^2 df \tag{5.30}$$

Using Parseval's power theorem [14], above equation becomes as:

$$\left[\frac{x_{o1}(T)-x_{02}(T)}{\sigma}\right]^2_{\max} = \frac{2}{N_o}\int_{-\infty}^{\infty} x^2(t)dt \tag{5.31}$$

In case of ASK, x(t) is present from 0 to T, hence the limits in above Equation (5.31) can be changed as:

$$\left[\frac{x_{o1}(T)-x_{02}(T)}{\sigma}\right]^2_{\max} = \frac{2}{N_o}\int_{0}^{\infty} x^2(t)dt \tag{5.32}$$

Further $x(t)=x_1(t)-x_2(t)$ and for ASK, $x_2(t)$ is zero, hence $x(t)=x_1(t)$ so Equation (5.32) can be written as:

$$\left[\frac{x_{o1}(T)-x_{02}(T)}{\sigma}\right]^2_{\max} = \frac{2}{N_o}\int_{0}^{T} x_1{}^2(t)dt \tag{5.33}$$

The value of $\int_0^T x^2(t)dt$ obtained from the output of sum2 is $4V_m^2$ T. Therefore, Equation (5.33) can be written as:

$$\left[\frac{x_{o1}(T)-x_{02}(T)}{\sigma}\right]^2_{\max} = \frac{8}{N_o}V_m^2 T \tag{5.34}$$

$$\left[\frac{x_{o1}(T)-x_{02}(T)}{\sigma}\right]_{\max} = 2\sqrt{\frac{2P_sT}{N_o}},$$

where P_s and T are the signal power and time period of carrier signal.

Now P_sT is the signal energy in one bit, the error probability is given as:

$$P_e = \frac{1}{2}erfc\left\{\sqrt{\frac{2E}{N_o}}\right\} \tag{5.35}$$

But the average energy per bit is $E_b = \frac{E}{2}$

Probability of error in terms of energy of one bit can be written as:

$$P_e = \frac{1}{2}erfc\left\{\sqrt{\frac{E_b}{N_o}}\right\} \tag{5.36}$$

Figure 5.8 plots the BER performance of the system obtained from simulation model and it is equal to theoretical value as expressed in Equation (5.36).

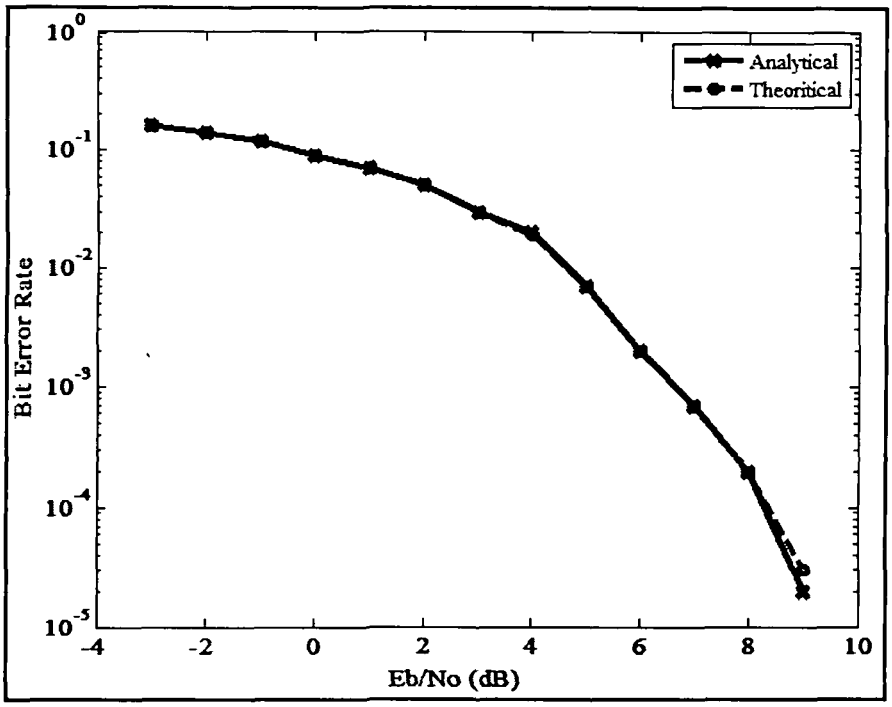

Fig.5.8: Analytical performance of BPSK system

5.5 Phase and Amplitude margin with Simulation Model

The proposed BPSK demodulator as discussed in Chapter 4 has been tested for phase and amplitude margin of received and local oscillator signals. In coherent detection it has been assumed that both the received and local signals were in same phase. The phase lock loop (PLL) circuit is used in all wireless systems for phase synchronization [1]-[3]. If phase of both the signals are not matched, it results in performance degradation in terms of more BER as discussed in Section 5.2.3. We have varied the phase of local carried from 0 degree to 80 degree. Upto phase mismatch of 80 degree, demodulator demodulates the signal without an error as shown in Figure 5.9. As phase

mismatch goes beyond 80 degree the received signal demodulates with an error. The phase difference between the incoming carrier and the local signal causes summer 1 as discussed in Figure 4.42 of Chapter 4 to give a low output instead of '0' for logic low reducing the difference between the two detected levels. Hence threshold margin goes higher than logic '1' and demodulator decodes logic '0' instead of logic '1'.

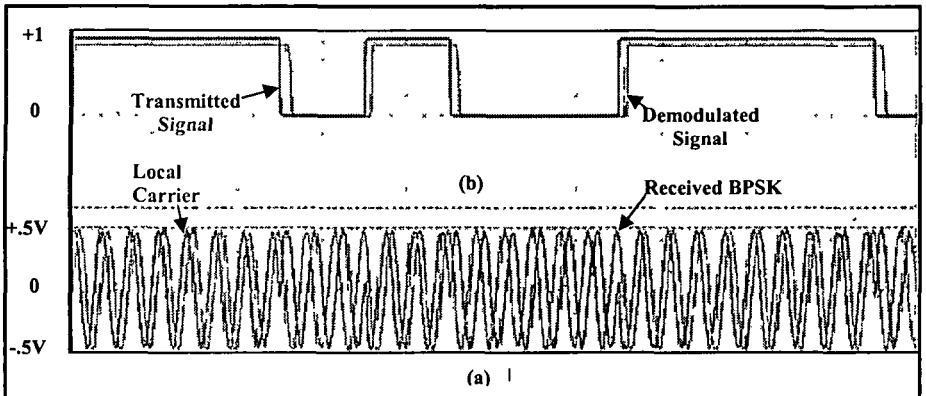

Fig: 5.9 Phase margin for error free demodulation of BPSK signal

In Section 4.7 and Section 5.4, the proposed circuit converts the incoming BPSK signal into ASK as shown in Figure 4.44 of Chapter 4 and the output of summing Circuit 2 in Figure 4.42 can be written as $4V_m^2$ for logic high and '0' for logic low. Both the signals may be in phase coherence but they may differ in magnitude. So the proposed circuit has been simulated with varying the magnitude of the local carrier amplitude and but keeping the level of received BPSK signal fixed at 500mVolt and vice versa. The simulation shows that a further decrement upto140mVolt provides an error free demodulation as shown in Figure 5.10. Further decrement decreases the amplitude of the integrated signal than the threshold setting resulting in an error.

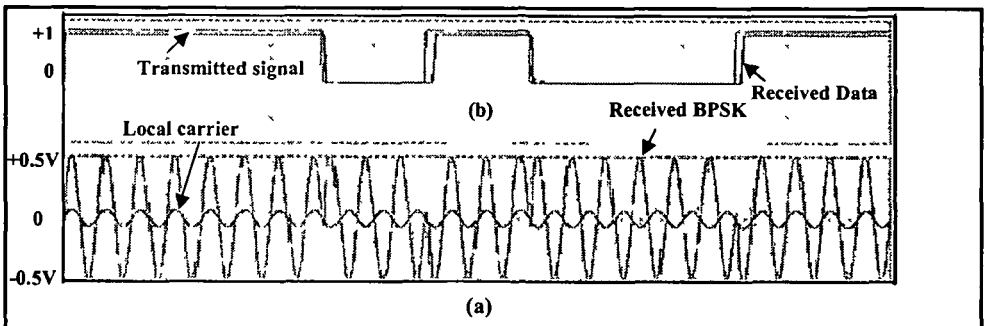

Fig: 5.10 Amplitude margin for error free demodulation of BPSK signal

In another situation the both signals may be both non-coherent and unequal in magnitude. The circuit demodulates satisfactorily BPSK signal of 500mVolt with local signal of magnitude 190mVolt and phase shift upto 62 degree as shown in Figure 5.11 using Microsim software.

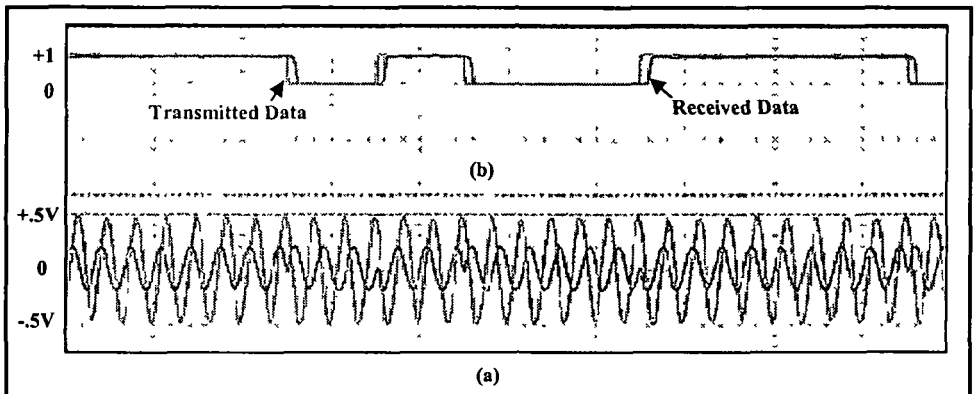

Fig: 5.11 Amplitude and phase margin for error free demodulation

5.6 Performance Measurement with Eye Pattern

In communication, an eye pattern is an oscilloscope display in which a received digital data from a receiver is repetitively sampled and applied to the vertical input, while the data rate is used to trigger the horizontal sweep. The effect of distortion caused by noisy channel and filtering can be studied by observing these oscilloscope patterns. In high

speed signaling system, the distortion, noise, and interference on signal waveforms constrain the system performance, e.g. bandwidth and power. An eye diagram provides one fundamental and intuitive view to evaluate the quality of the channel [28].

The proposed circuit performance has been studied using the eye pattern. Figure 5.12 shows the obtained eye diagram under SNR 10dB for BPSK signal at 100 MHZ carrier frequency. From the eye diagram, we have estimated noise margin and distortion as 0.9V and 0.5V respectively at SNR of 10 dB. Figure 5.13 shows the plot for noise margin and distortion. It is seen from the Figure that as SNR increases, the distortion decreases whereas noise margin increases.

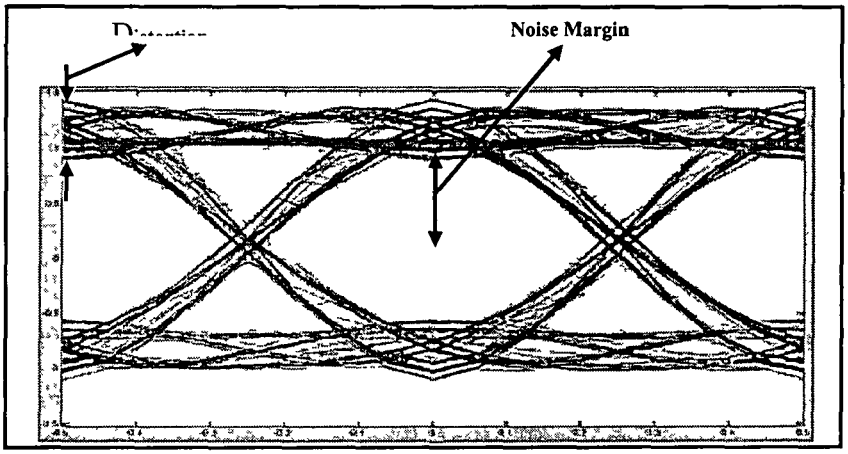

Fig.5.12: Eye pattern of received data at 10dB

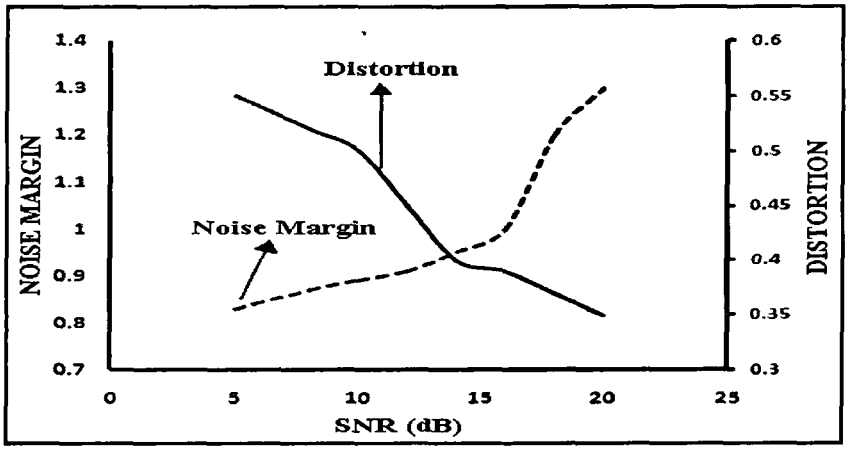

Fig.5.13: Plots for noise and distortion from eye

5.7 Experimental Performance Measurements

We have implemented the designed four channel CPSK based DSSS transceiver (shown in Figure 4.39) with active and passive components [29]. Figure 5.14 shows the experimental setup for the hardware implementation with different test equipments.

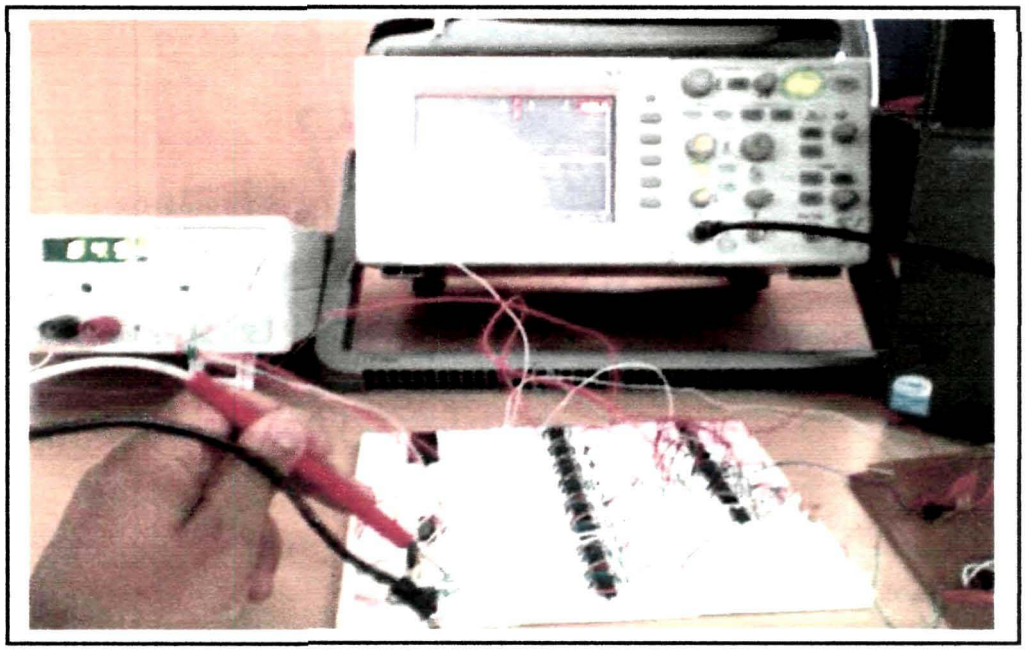

Fig.5.14: Photograph of experimental setup for CPSK based DSSS system

Figure 5.15 shows the oscilloscope traces of waveforms of different stage of the circuit. Trace (a) shows the waveform of four channels. Trace (b) shows PN sequences generated by PN sequence generator circuit. Trace (c) shows the waveform of received four channels.

The traces of PN sequences and four channels shown in the Figure 5.15 are matched well with simulated waveforms of PN sequences and four channels. We have measured BER by using a BER meter at SNR values of 8 dB, 12 dB and 14 dB for different JSR value . As shown in Figure 5.7, the experimental values of BER are very close to the simulated values.

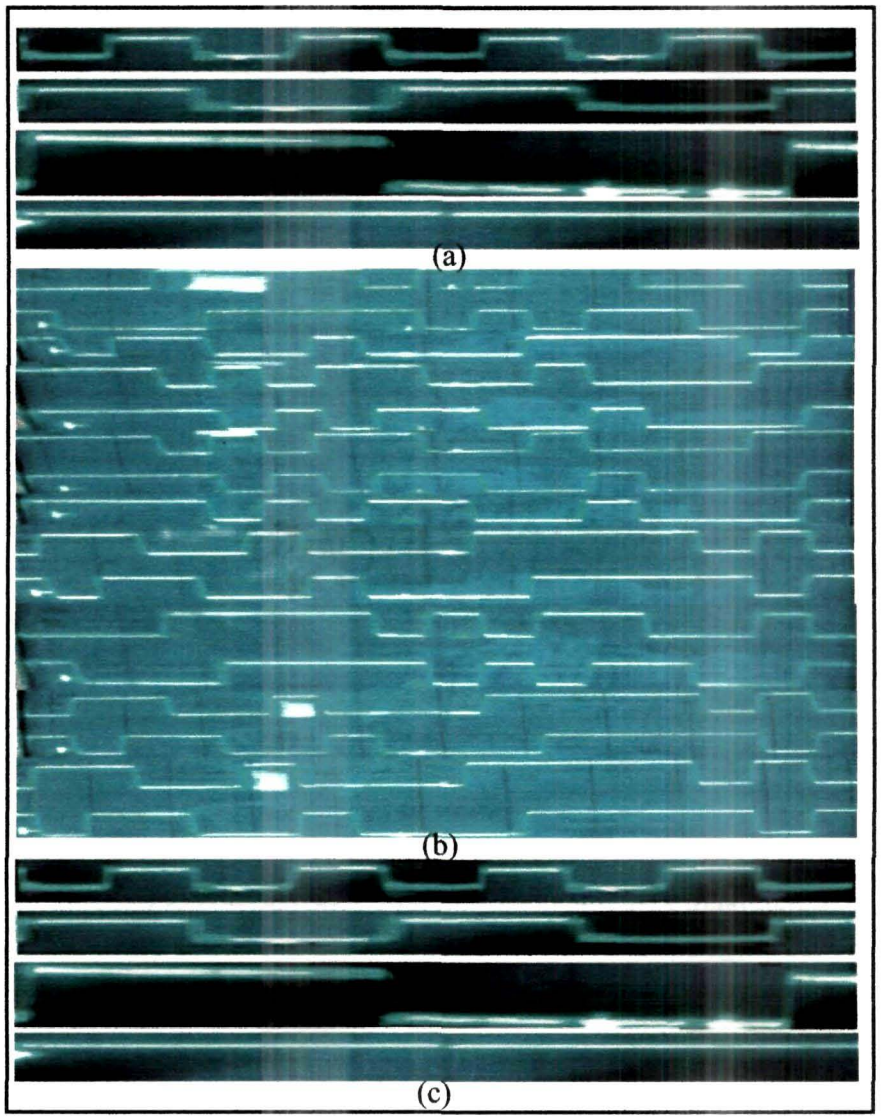

Fig.5.15: Experimental results (a) Transmitted 4–channels, (b) Different PN sequences, (c) Received 4-channels

5.8 Conclusion

In this chapter, we have investigated CPSK based DSSS transceiver for performance evaluation with 4 users on a single channel as multi-channeling scheme. This scheme provides capacity improvement for the accommodation of more users on a single channel in comparison to single channel with the existing CDMA system. BPSK

technique was used as it is the most robust and provides excellent performance under noise condition. The performance was tested by simulation model with the help of Microsim software Version 8.0 and designed device provide a good performance under AWGN and jamming condition. The proposed circuit for BPSK demodulator was investigated for BER performance. The performance has been compared with the existing system and provides the same performance as the existing system.

We have carried the performance test using eye diagram and it is seen that noise margin and distortion at SNR of 10dB are as 0.94 and 0.5 volts respectively. The BER of the CPSK- DSSS system using conventional BPSK and proposed BPSK at SNR of 8 dB JSR of 8dB are $2x10^{-2}$ and 10^{-4} respectively. So there is an improvement of BER performance using CPSK based DSSS system using the proposed BPSK. The circuit was also demonstrated experimentally. It was observed that oscilloscope traces matches with the simulated waveforms of the circuit and the experimental values of BER are also close with simulated values of BER.

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Chapter 6

Design and Simulation of Multi-Channel Frequency Hopping Spread Spectrum Communication System using coded M-ary Frequency Shift Keying

6.1 Introduction

From Chapter-4 and 5 it is seen that multi channel direct sequence spread spectrum communication does not perform well when subjected to jamming and intentional interference/ multiple access interference, due to having no frequency hopping concept. So it is required to use frequency hopping concept to encounter the problem of jamming and intentional interference [1]-[10]. At the same time we have to provide multi services to multi users [11]-[14] by using multi-channel capability within the limited available bandwidth. The conventional frequency hopping spread spectrum (FHSS) technique uses the band pass filters (BPF) for separating the different hops for further processing [1]-[18]. For this we have proposed a wide band sinusoidal frequency to voltage converter for separating the different bands in FHSS system. It reduces the circuit complexity and provides better performance. In this chapter we have discussed the design of code M-ary frequency shift keying technique based multi-channel frequency hopping (CMFSK/FH) spread spectrum signaling for multi channel communication

This Chapter is structured as follows. Section 6.2 briefly describes the architecture of a CMFSK system for transmitter and receiver. Section 6.3 Section 6.4 is devoted to the design and simulation of band pass filter (BPF) based FHSS transmitter and receiver respectively. Section 6.5 discusses the design and simulation of proposed sinusoidal frequency to voltage (FVC) methods for separating signal in M-ary FSK system. Finally, the conclusion is given in Section 6.6.

6.2 Architecture of Proposed CMFSK based Multi-Channel Frequency Hopped Spread Spectrum System

In this section the basic architecture of CMFSK based frequency hop transceiver system for multi-channeling has been presented.

6.2.1 CMFSK based FHSS Transmitter

The CMFSK module groups the input data from K users into K bit ($K = 2Log_2 M$), and represented by an integer m, $0 < m < M-1$. This K-bit data is composed by taking one bit from each user and have total 2^K symbols. Using the PN sequence generator, 2^K PN sequences are generated and applied to input lines of the sequence selector. Each symbol selects one of $M = 2^K$ PN sequences, of same duration as the period of select word.. A PN waveform with length N (N is the spreading factor, and N>>K) chips is selected from signaling waveform 2^K sets. If chip duration is T_C, then symbol duration is expressed as: $T = N \times T_C$. These selected PN sequences are converted into parallel bits with the help of serial in parallel out (SIPO). These parallel bits are converted into analog voltage level, (Digital to analog converter) which is fed into VCO. The VCO will generate the frequency as a function of analog voltage level, with a pre-specified hop size fm. The transmitted signal of m^{th} symbol is defined as:

$$s_m(t, f_m) = \sqrt{\frac{2E_s}{T}} Sin[2\pi(f_c + mf_m)t] \qquad (6.1)$$

Where m=1, 2, 3.....M. $M = 2^K$ and K=total number of channels in CMFSK signaling system, f f_c = Carrier frequency, T=Symbol period and E_s = signal power. Block diagram in Figure 6.1 show the concept of proposed CMFSK transmitter for multiplexing the K-user.

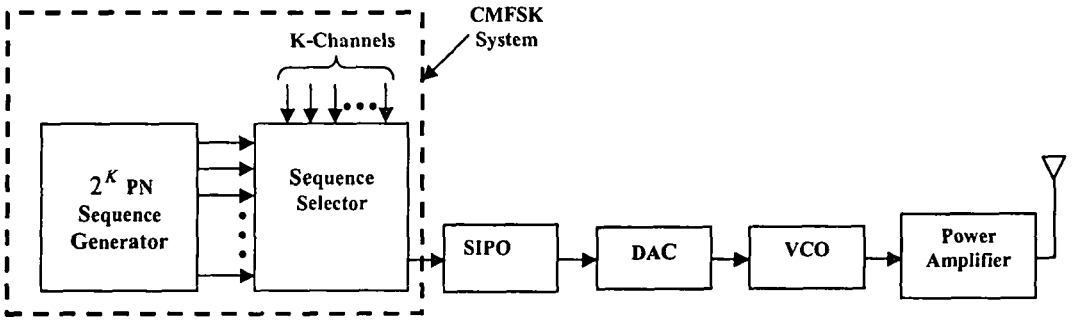

Fig. 6.1: Block diagram of CMFSK based FHSS transmitter

6.2.2 CMFSK based FHSS Receiver

Figure 6.2 shows the block diagram of K-channel CMFSK/FH receiver, which consists of the band pass filters, detectors and integrators, comparators and decoder. Since there are $M = 2^K$, hop frequencies for M symbols, $M = 2^K$ band pass filters (BPF) are required and each BPF allows the corresponding hop frequency while rejecting all other frequencies. The output of the filter is detected by diode detector and integrated with the R-C circuit for the fixed time period. The outputs of all, detectors are applied to $M = 2^K$ comparator circuits. The threshold setting of comparators allows only one out of $M = 2^K$ comparator to give high output and other gives low output. The outputs of the comparator are applied to decoder circuit which decodes 2^K inputs into K- data word as was transmitted from the transmitter side.

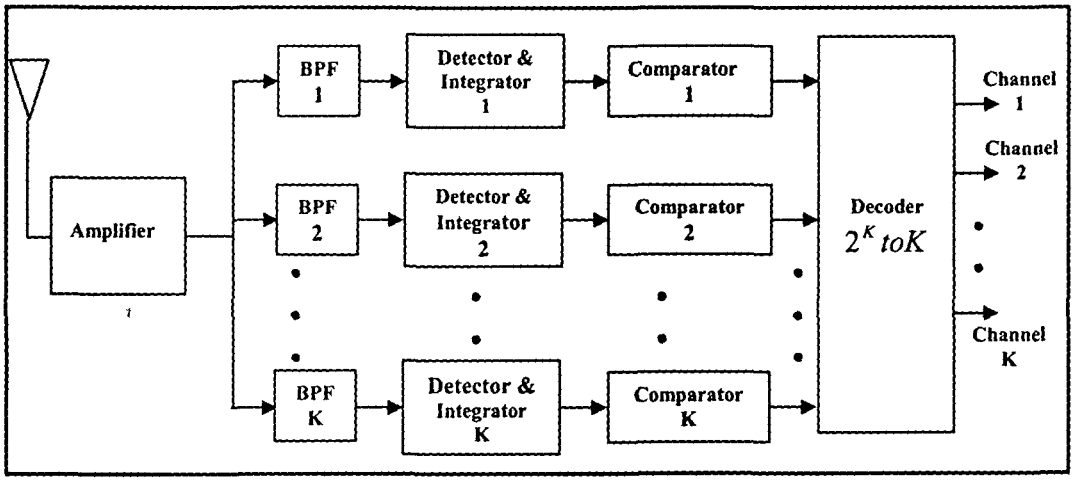

Fig.6.2: Block diagram of CMFSK based FHSS system

6.3 CMFSK based FHSS Transmitter Design

In Section 6.2.2 we have discussed the proposed technique for multi-channeling by multiplexing the K-users with frequency hop spread spectrum. In this technique as number of users increases the circuit becomes complex. In view of circuit complexity,

we have designed the proposed system for (K= 4), 4-channels only. Therefore, we will concentrate on design and simulation of 4-channel CMFSK based transmitter.

The block diagram of the proposed transmitter for CMFSK based FHSS is shown in Figure 6.1. This block diagram has some common blocks as shown in Chapter 4 Figure 4.1, for design of CPSK based DSSS system [12]-[15]. The working of these common modules is same. These modules are PN sequence generator, shift register, data word generator and PN sequence selector and represented by the CMFSK system in Figure 6.1. The modules are discussed in details with their design, simulation and simulation results in section 4.3.1.Therefore, design and simulation of common modules is not discussed in this Chapter. However, P-Spice simulated waveforms are used.

The CMFSK system selects one PN sequence out of 2^K PN sequences, as per the address select lines of the sequence selector. Address lines are the 4-bit data word generated by data word generator circuit. The selected PN sequence is applied to the serial in parallel out (SIPO) circuit for driving the digital to analog converter as discussed in the next section 6.3.1. Figure 6.3 shows the block diagram of CMFSK system.

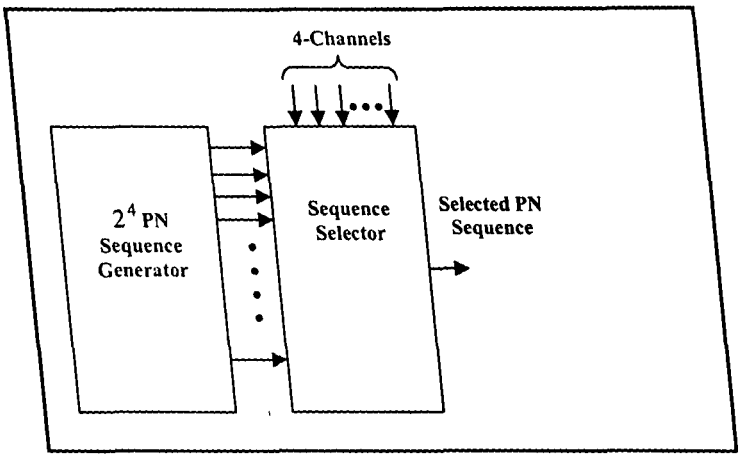

Fig. 6.3: Block diagram of CMFSK system

Figure 6.4 shows the simulated wave forms of CMFSK system. Trace (a) shows the 4-PN sequences generated by PN generating circuit. Trace (b) shows the clock signal used for PN generating and shift register circuits [19]. Trace (c) shows the 15 PN sequences generated by shift register using one PN sequence. Trace (d) shows the selected PN sequence at the output of data selector. The trace (e) shows the 4-bit data word to represent 4-channels.

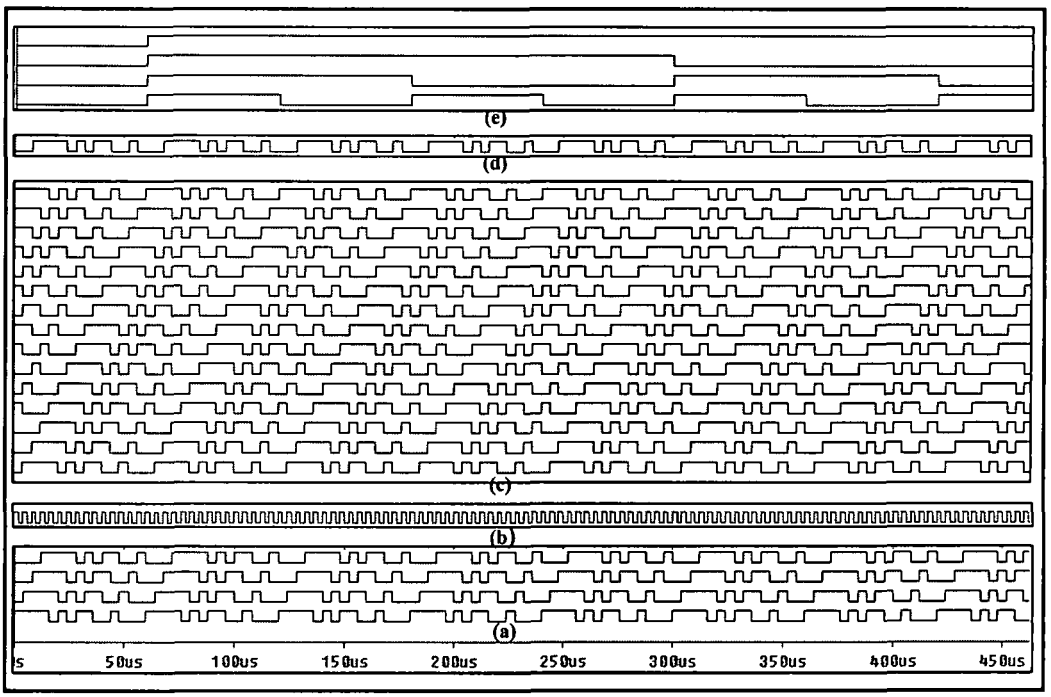

Fig.6.4: P-Spice simulated waveforms of CMFSK system

6.3.1 Serial In Parallel Out

Shift registers are sequential logic circuit used for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop [19]-[20].

Each selected PN sequence from the data selector is to be converted from serial bits to parallel bits for applying to digital to analog converter (DAC). The SIPO performs this operation and convert each selected PN sequence available at the output of data selector from serial to parallel. SIPO is a sequential logic circuit for storage of digital data. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. For converting the 15 bits of PN sequence into parallel output we have used integrated circuit 74ls673 which is 16 bit storage register in a single 24 pin package [21]. The selected PN sequences from the data selector are applied to this register and bits enter serially. The clock used in the PN generating circuit as shown in Figure 6.4 is used to drive the integrated circuit. And as the last bit enters the shift register the data are stored and simultaneously appears at the output lines. Figure 6.5 shows the 15 PN sequences available in parallel. The clock used for SIPO has a time period of 60μS with 30μS T_{ON} and 30μS T_{OFF}. It is equal to the time period of one PN sequence

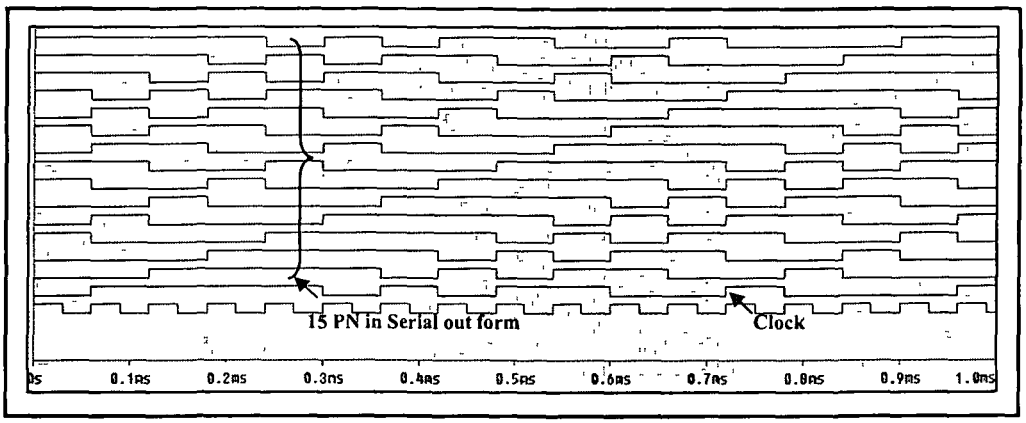

Fig.6.5: Simulated output of SIPO

6.3.2 Digital to Analog Converter

Digital to analog converters (DAC) are used for transforming digital data into analog form [22]-[23]. Many integrated circuits are available with different configurations as 8-bits, 10-bits, 12-bits, 16-bits and 24 bits input. The output of a DAC is expressed as:

$$V_{out} = \sum_{i=1}^{N} b_i = \Delta \sum_{i=1}^{N} b_i .2^{N-i} \qquad (6.2)$$

where, N = No. of bits in the DAC input

V_{FS} = Full scale input voltage

$$\Delta = \frac{V_{FS}}{2^N} = 1LSB$$

B_i = '0' or '1'

Good linearity is a measure of the deviation if the actual output amplitude from the ideal output amplitude. It is determined by measuring the amplitude of the output signal as the amplitude of the output signal is digitally to a low level. A perfect DAC exhibits no difference between the ideal and actual amplitudes. In Figure 6.6 plot (a) and (b) show the block diagram and transfer function respectively of a linear DAC.

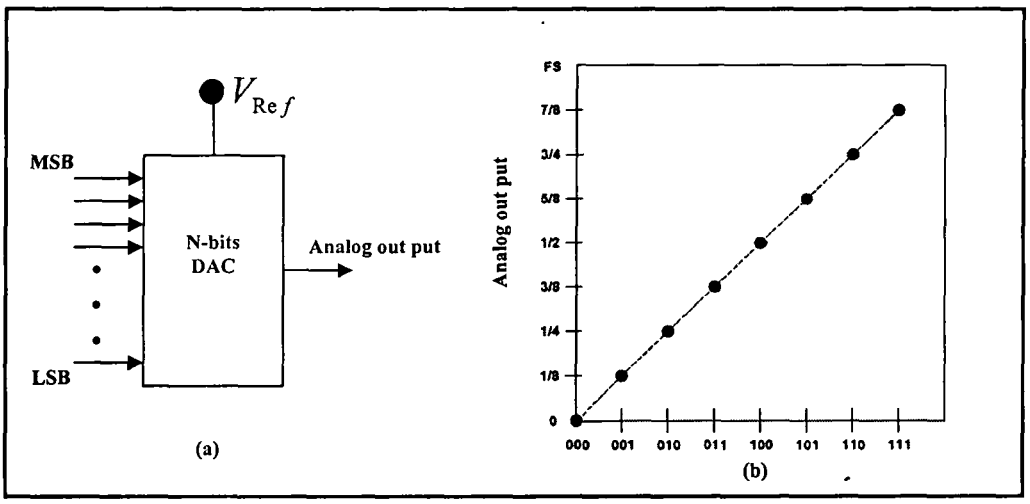

Fig. 6.6: Block diagram and characteristics of a DAC [21]

In this design the DAC provides the necessary control voltage for the voltage control oscillator (VCO) and using integrated circuit DAC 701 which is a 16 bit digital to analog converter [21]. This DAC has precision buried zener voltage reference and low noise, fast settling output operational amplifier on a small monolithic chip. Linearity

error is very low and of the order of ±0.0015%. The pin configuration and connections are shown in the Figure 6.7. The output of DAC varies from 90mVolt to 1350mVolts as shown by trace obtained from simulation and shown in Figure 6.8.

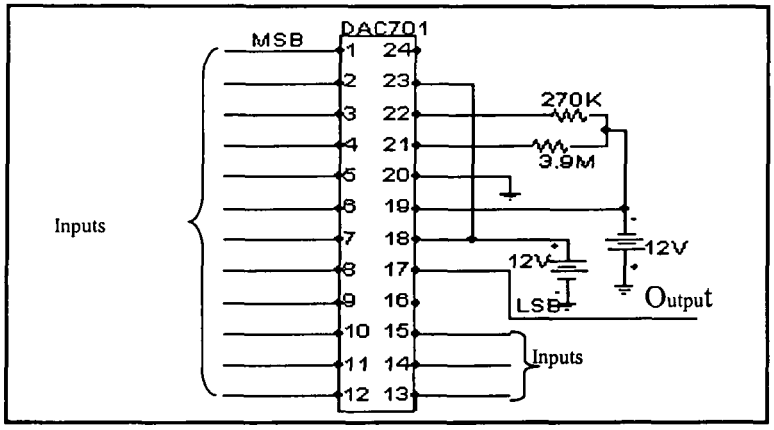

Fig.6.7: PIN diagram of DAC 701

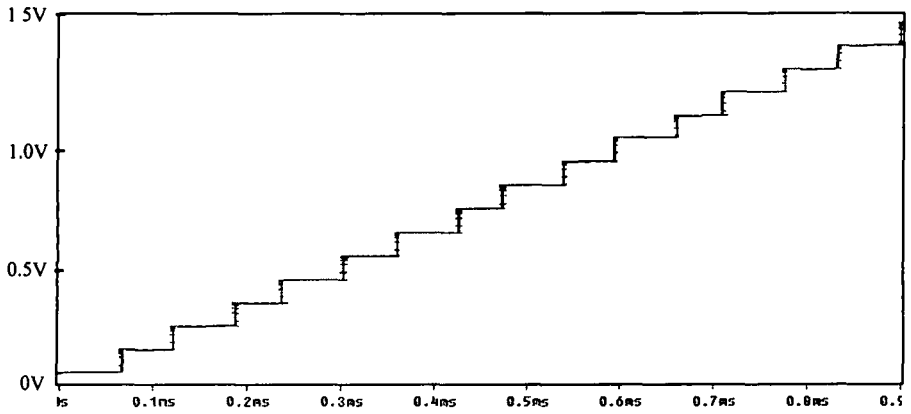

Fig.6.8: P-Spice simulated output from DAC

6.3.3 Voltage Controlled Oscillator

Voltage control oscillator (VCO) is very important electronic circuit whose oscillation frequency is controlled by a voltage input over a wide range. The applied tuning voltage determines the instantaneous oscillation frequency. Consequently, a modulating signals

applied to control input may cause frequency modulation (FM) or phase modulation (PM). A VCO may also be part of a phase-locked loop. VCO must have a linear relation between applied voltage and generated frequency. Here we have used MAX 038 VCO (seen in Figure 6.9) for generating the sinusoidal frequency for design of the proposed FHSS system. Figure 6.10 shows the internal configuration of MAX 038 operating with the principle of a relaxation type oscillator [21] in which capacitor C_F is alternately charging and discharging with constant currents, simultaneously producing a sinusoidal wave, triangle wave and a square wave depending upon control voltage A_0 and A_1 as shown in Table -6.1 .

Table-6.1: Control voltage of MAX 038 [21]

A0	A1	WAVEFORM
X	1	Sine wave
0	0	Square wave
1	0	Triangle wave

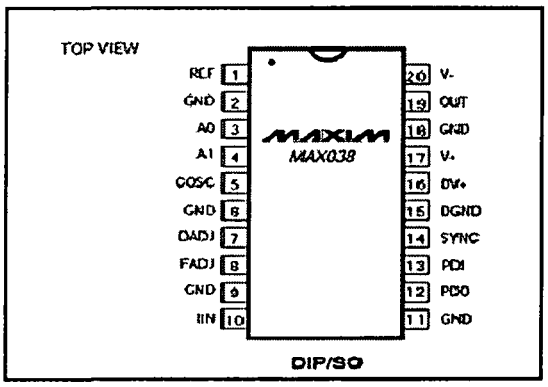

Fig. 6.9: Pin diagram of VCO Max038 [21]

The MAX038 is a high-frequency function generator that produces low-distortion sine, triangle, saw tooth, or square (pulse) waveforms at frequencies of less than 20 MHz or more, using a minimum of external components. Frequency and duty cycle can be independently controlled by programming the current, voltage, or resistance. The desired output waveform is selected under logic control by setting the appropriate code

at the A0 and A1 inputs as shown in Table-6.1. The duty cycle can be varied over a wide range by applying a ±2. 3V control signal, facilitating pulse-width modulation and the generation of sawtooth waveforms. Figure 6.9 shows the Pin diagram of the VCO. An internal closed-loop amplifier forces I_{IN} to virtual ground, with an input offset voltage less than ±2mV. IIN may be driven by either a current source I_{IN}, or a voltage V_{IN}, in series with a resistor R_{IN}.

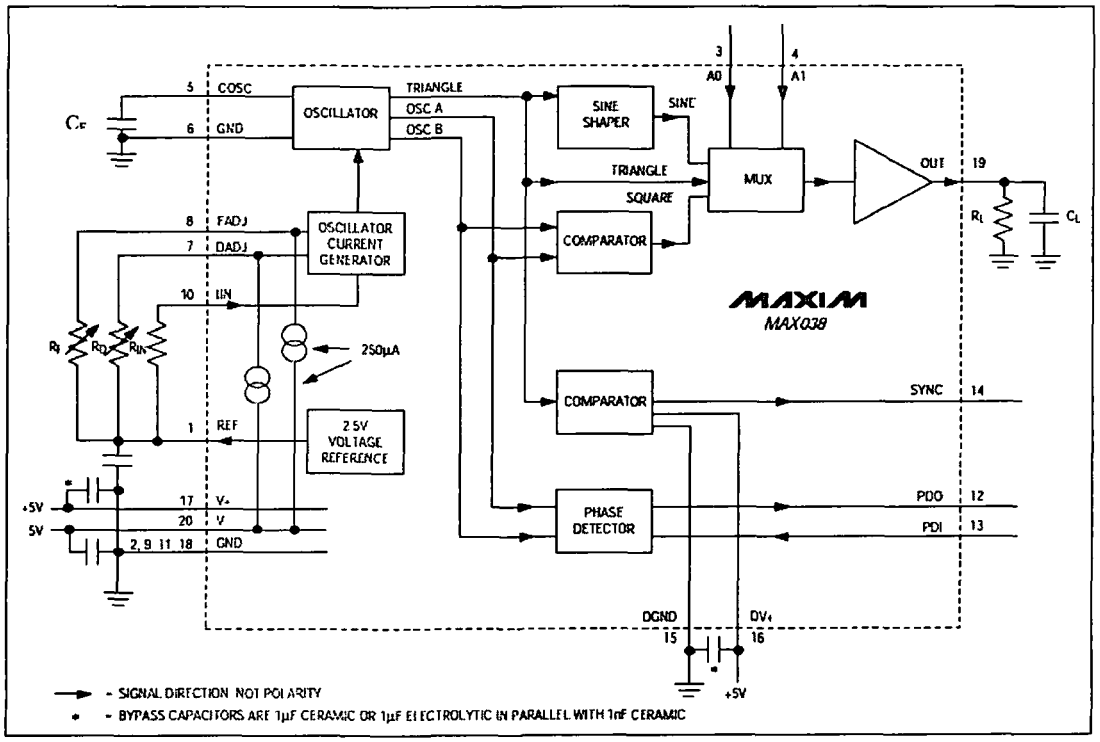

Fig.6.10: Internal circuit diagram of MAX 038 (VCO) [21]

When using a control voltage (Tuning voltage) in series with fixed input resistor R_{IN}, the output frequency is a direct function of control voltage (V_{IN}).Varying V_{IN} modulates the oscillator frequency. For example, using a 10K ohm resistor for R_{IN} and sweeping V_{IN} from 20mV to 7.5V produces large frequency deviations linearly. The output

frequency is calculated using the formula given in the Equation 6.3. Figure 6.11 shows the circuit diagram for obtaining sinusoidal output of the VCO.

$$F_o(MHz) = \frac{V_{IN}(Volts)}{R_{IN}(Ohm) \times C_F(pF)} \tag{6.3}$$

With resistance R_{IN} 100K Ohms capacitor C_F 3pico Farads, DAC output varies from 90m Volts to 1.35Volts, the VCO frequency varies from 300KHz to 4.5MHz as given by Equation (6.3). This output of the DAC is applied to the VCO and corresponding to this varying voltage (tuning voltage), VCO generates the different sinusoidal frequencies

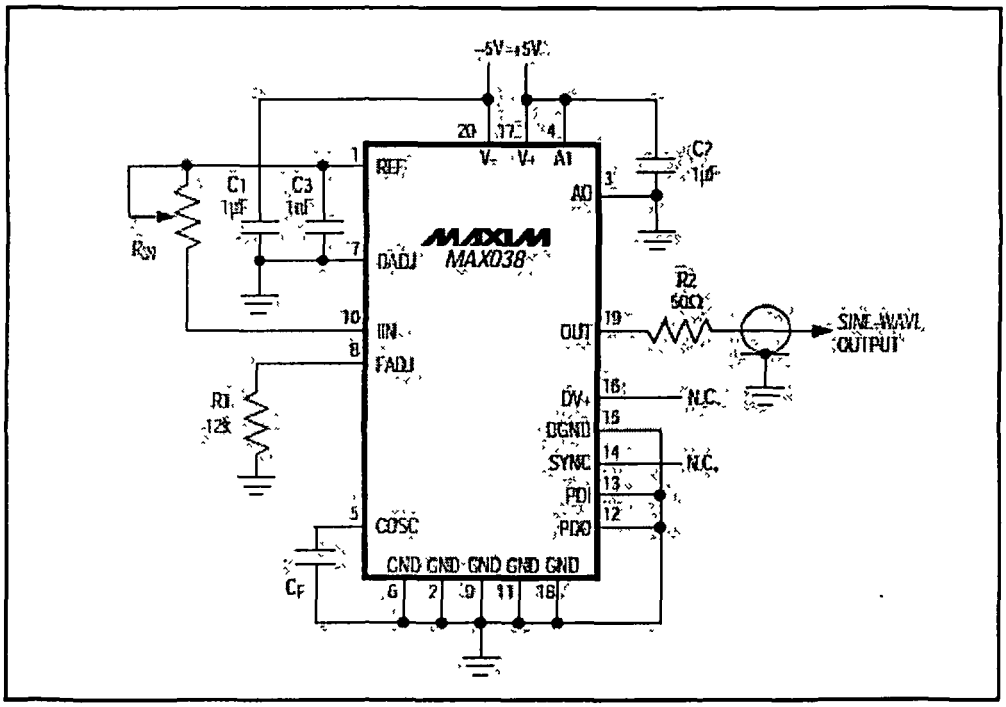

Fig. 6.11: IC MAX038 as sinusoidal VCO [21]

Table: 6.2 VCO Output frequencies

V_{IN} (m Volt)	R_{IN} Ω	C_F (pF)	F_o (KHz)
90	100K	3	300
180	100K	3	600
270	100K	3	900
360	100K	3	1200
450	100K	3	1500
540	100K	3	1800
630	100K	3	2100
720	100K	3	2400
810	100K	3	2700
900	100K	3	3000
990	100K	3	3300
1080	100K	3	3600
1170	100K	3	3900
1260	100K	3	4200
1350	100K	3	4500

6.4 Simulation Results of CMFSK based FHSS Transmitter

In this section we have shown the simulation results of the full circuit of 4-channel CMFHSS transmitter. The block diagram and P-Spice simulated circuit diagrams for multiplexing 4-users are shown in Figure 6.12 and Figure 6.13 respectively. Table 6.3 shows the different components used for the simulation of CMFSK transmitter circuits along with their specifications. The selected PN sequences by the PN sequence selector are applied at the input of SIPO which converts serial coming PN sequences into

parallel output as discussed in Section 6.3.1. These 15 parallel PN sequences are applied at the input pins of DAC. DAC generates a D.C voltage as per weight of each bit in a PN sequence. The output of DAC varies from 90mVolt to 1350mVolts as shown in Figure 6.8. Proportional to these control voltages, the VCO generates different frequencies (hops). Figure 6.14 shows different waveforms generated at different stages in the proposed transmitter.

In Figure 6.14 trace (a) shows the 4-bit data word (symbols) generated by data word generator circuit. This 4-bit data word (symbol) represents 4-channels. The each symbol is of as shown by the trace. The trace shows all 15 possible states from 0001 to 1111. Trace (b) shows the required 15 PN sequences. Trace (c) shows the output of data selector which is the selected PN sequence. Trace (d) shows the PN sequence in parallel obtained at the output of SIPO. Trace (e) shows the control voltage for the VCO and generated by the DAC. As seen from the Figure, it varies from 90m volts to 1250m volts as per PN sequence. Finally, the trace (f) shows the 15 frequencies varying from 300 KHz to 4.5 MHz as the transmitted symbols.

Table-6.3 List of components used for design of Transmitter

Block	Type	Value
PN Generator	D-flip flop- 4 No	SN74ls74a
	Resistance - 01 No	10 Ω, 0.25Watt
	Capacitor- 01 No	2nF
	EX-OR gate-01 No	SN7486
	D-Flip Flop-15 No	SN74ls74a
Data word generator and PN Sequence Selector	JK Flop Flops-4 No	SN74F109
	Multiplexer- 01	74as250
	Inverter-01	74ls04
SIPO	SIPO-01	74ls673

DAC	D/A converter-01	DAC701
	Potentiometer-02 Resistance -02	4.7 KΩ, 1Watts 269K Ω, 3.9M Ω
VCO	Sinusoidal VCO-01 No	MAX038
	Potentiometer -01 No	4.7KΩ, 1Watts

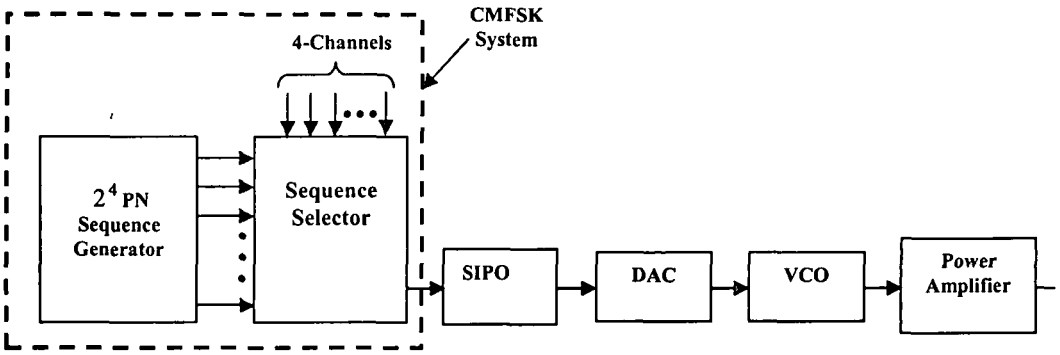

Fig. 6.12: Block diagram of CMFSK based FHSS transmitter

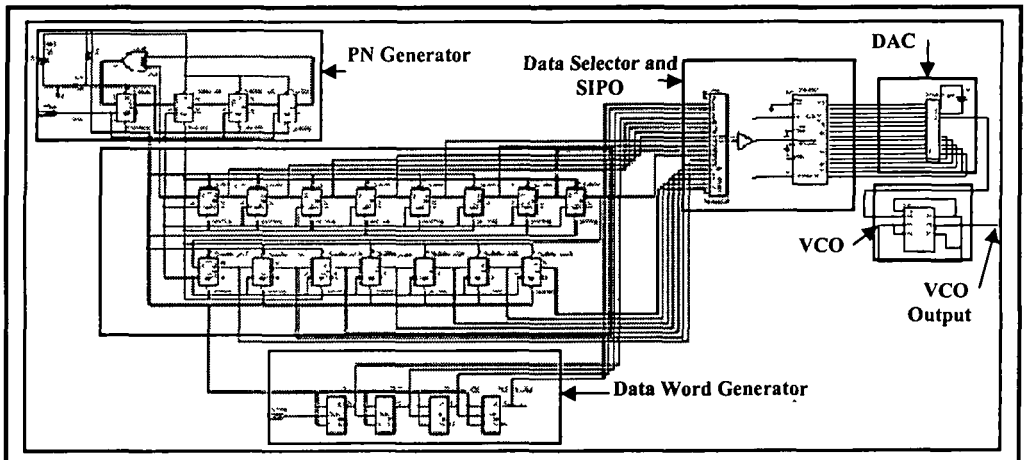

Fig.6.13: Simulated Circuit Diagram of CMFSK based FHSS Transmitter

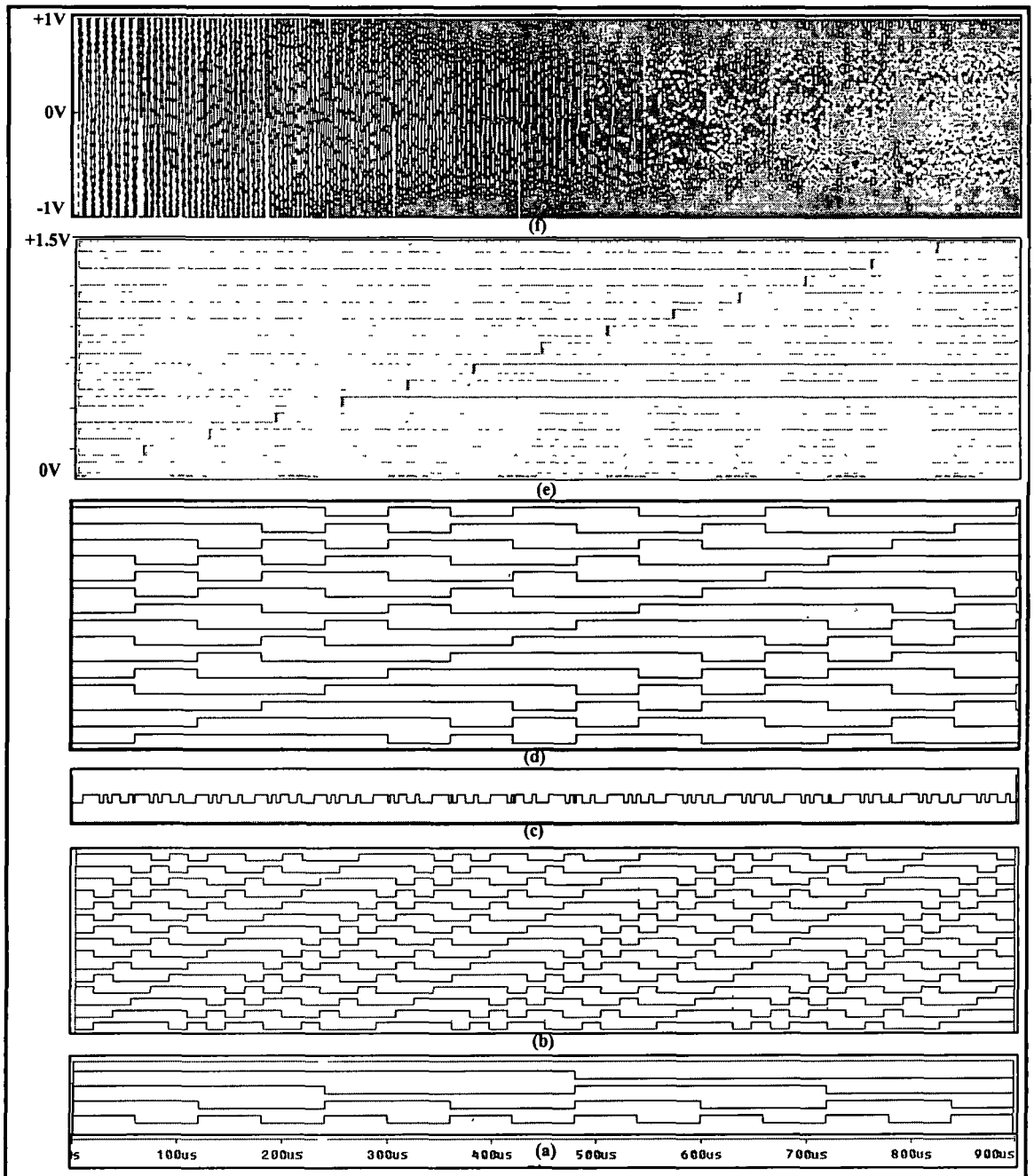

Fig.6.14: P-Spice simulated waveform of transmitter circuit, (a) Data word generator, (b) 15 PN sequences obtained from PN circuit, (c) PN sequence at the output of PN selector, (d) PN sequence at the output of SIPO, (e) Output obtained from DAC, (f) VCO output.

6.5 CMFSK based FHSS Receiver Design with Band Pass Filters

As discussed above this section focuses on the design and simulation of 4-channel CMFSK based FHSS receiver for separating the 4-users that are multiplexed with the designed 4-channel CMFSK transmitter. We have designed a CMFSK based FHSS receiver to separate the 4-channels. The designed receiver consists of band pass filters (BPF), detectors, integrators, comparators and decoder circuits [22]-[23]. Each stage is discussed in details with the simulated waveforms.

6.5.1 Band Pass Filters

In FHSS system band pass filter (BPF) is essential components for separating the one hop from other hop. The proposed CMFSK based FHSS receiver consists of 15 BPF each filter is matched to one of the carrier frequency. The receiver signal is first passed through these 15 BPF. The output of each filter is further processed in the next stages.

The BPF is a filter that passes frequencies in a desired range and attenuates frequencies below and above [23]. Band-pass filters ideally have a pass band between a low and a high cut-off frequency and reject frequencies outside of this band (the stop band). In this design, we have used multiple feed back BPF for keeping the number of components limited for simulation. The multiple feedback topologies are widely used as a band-pass filter because it offers a simple and reliable band-pass implementation. The schematic of a multiple feedback BPF is shown in Figure 6.15 [21]. The design Equation for the circuit shown in Figure 6.15 for multiple feed back BPF is given as [21]:

$$\frac{E_i}{E_o} = -\frac{-s\dfrac{1}{C_4R_1}}{s^2 + s\dfrac{C_3 + C_4}{C_3C_4R_5}} + \frac{1}{R_5C_3C_4}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \qquad (6.4)$$

Choose C_3

then

$$k_o = 2\pi F_o C_3 \tag{6.5}$$

$$C_3 = C_4 \tag{6.6}$$

$$R_1 = \frac{1}{Hk} \tag{6.7}$$

where H is the gain of the BPF, and it is taken as unity.

$$R_2 = \frac{1}{(2Q - H)k} \tag{6.8}$$

$$R_5 = \frac{2Q}{k} \tag{6.9}$$

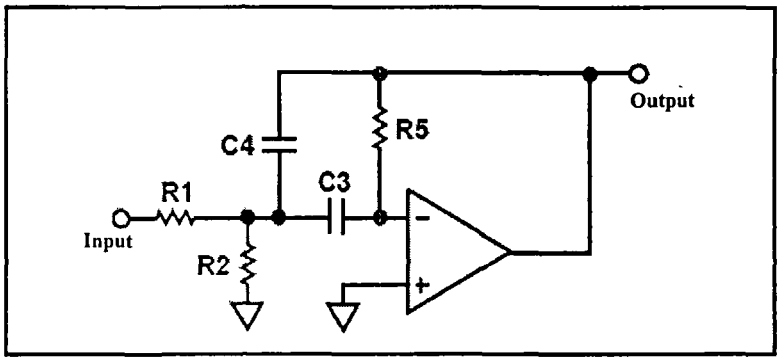

Fig. 6.15: Multiple Feedbacks BPF [21]

We have designed 15 BPF using Equations 6.5, 6.6, 6.7, 6.8, and 6.9 for 15 hoping frequencies. High speed integrated circuit AD 817/AD has been used for designing the each BPF with the help of simulation software. Figure 6.16 shows the simulated circuit of one BPF with center frequency 300 KHz, with the Microsim Version 8.0. Figure 6.17 shows its simulated frequency response. For other BPF the values of different components used are given in the Table 6.4 along with the center frequency of each BPF. Figure 6.18 shows the output signals obtained at the output of 15 BPF. One output represents one hop.

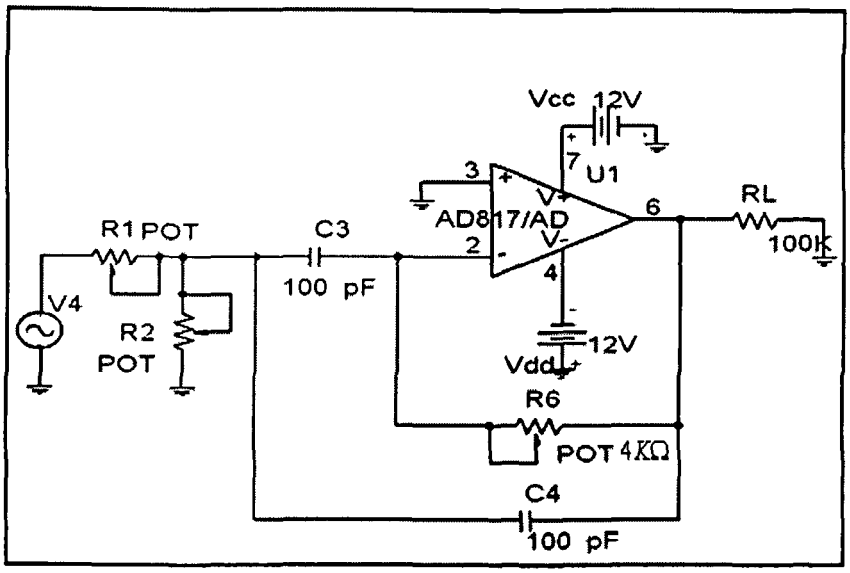

Fig. 6.16: Circuit diagram of BPF at 300 KHz

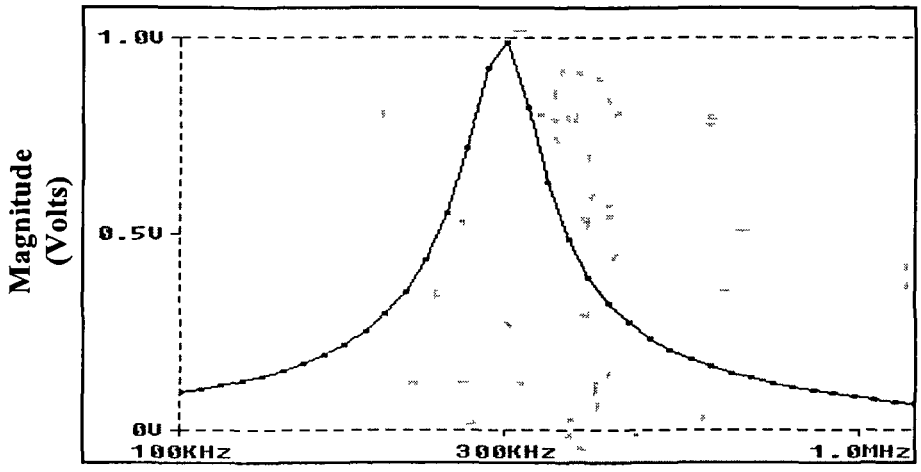

Fig.6.17: Response of BPF tuned at 300 KHz

Table: 6.4 Components values for 15 BPF

Frequency	R1 in K Ω	R2 in Ω	R5 in K Ω	C3 =C4
300KHz	5.31	280	106.1	100pF
600KHz	2.653	140	53	100pF
900KHz	1.77	93.3	35.3	100pF
1200KHz	17.8	923	35.37	10pF
1500KHz	5.3	279	106	20pF
1800KHz	4.42	233	88.4	20pF
2100KHz	3.79	199	75.8	20pF
2400KHz	3 32	175	66.4	20pF
2700KHz	2.95	155	59	20pF
3000KHz	2.65	140	53	20pF
3300KHz	2 41	127	48.2	20pF
3600KHz	2.21	116	44.2	20pF
3900KHz	2.04	107	40.8	20pF
4200KHz	1.9	100	37.9	20pF
4500KHz	1.77	93	35.37	20pF

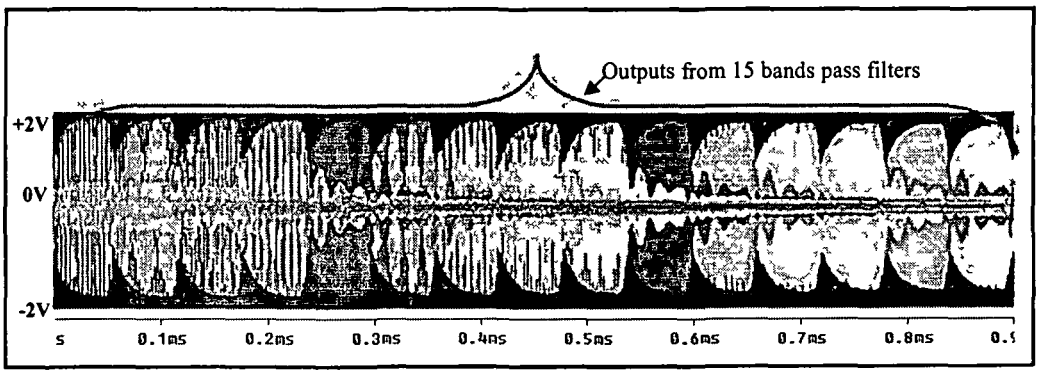

Fig.6.18: Outputs from 15 bands pass filters

6.5.2 Detector and Integrator

The outputs obtained from the BPF are applied to the detector and integrator circuit. This stage detects (rectify) the signal obtained at the output of the BPF and integrate for one hop period. This circuit consists of a simple diode as a detector followed by capacitor resistance (RC) circuit as an Integrator. There are 15 such similar circuits, one for each hop of frequencies. The output signal obtained at the output of the detector and Integrator circuit is a D.C voltage. This D.C. voltage is applied to the next stage for further processing the detected signal. In our simulated circuits for detector and integrator, we have used diode BAS 116/SIE, resistance of 1KΩ and capacitor of 2.2nF values [21]. Figure 6.19 shows the circuit diagram for detector and integrator circuit.

To maintain the linear response of each integrator, it requires the entire rectified voltage to be directly proportional to the entire for half cycle. For this we have used high voltage high speed switching diode BAS 116/SIE also the time constant τ of the circuit to the time period of one integration cycle T. If the integration duration is very short compared to the time constant $T << \tau$, capacitor integrates linearly and there will be linear increment in the voltage developed across the capacitor.

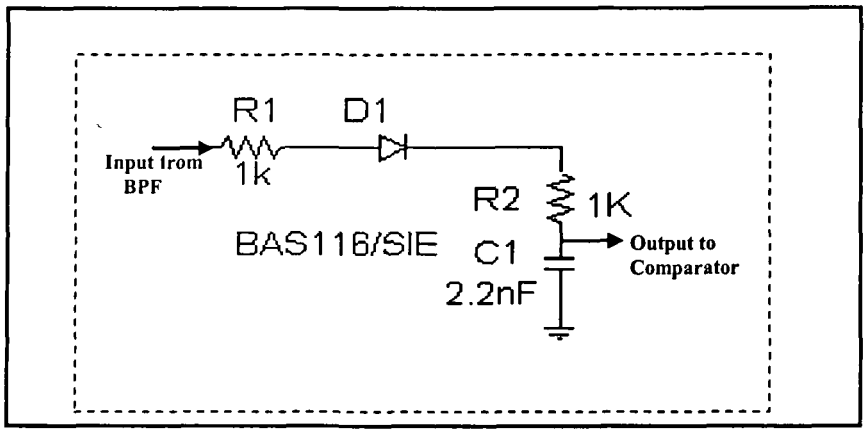

Fig-6.19 Diode detector and integrator circuit

6.5.3 Dump and Comparator

The dump circuit resets the output of the Integrator circuit to zero value at the end the integration cycle and keep the circuit ready for a next integration process for the next pulse. Comparator circuits are used to compare the output of each integrator with the preset value and provide a high output if the input value is higher than the preset value otherwise gives low output.

The dump circuit is a switching circuit which consists of one switching transistor driven by a fixed sharp pulse at the end of the integration period for resetting the output of an Integrator circuit to zero. The sharp pulse is applied to the transistor base and drives it to saturation. The voltage across the integrator capacitor is discharged to zero and keep it ready to integrate the next pulse. The comparator is designed using high-speed integrated circuits operational amplifier AD817/AD [21] connected in open loop comparator configuration to provide the infinite gain. The output from the integrator circuit is applied at the non inverting input of the amplifier and to inverting input a reference voltage (threshold level) is applied. It provides high output if the input is higher than the preset value otherwise low output. There are total 15 dump and comparator circuits. Figure 6.20 shows the P-Spice simulated circuit diagram of dump and comparator circuit.

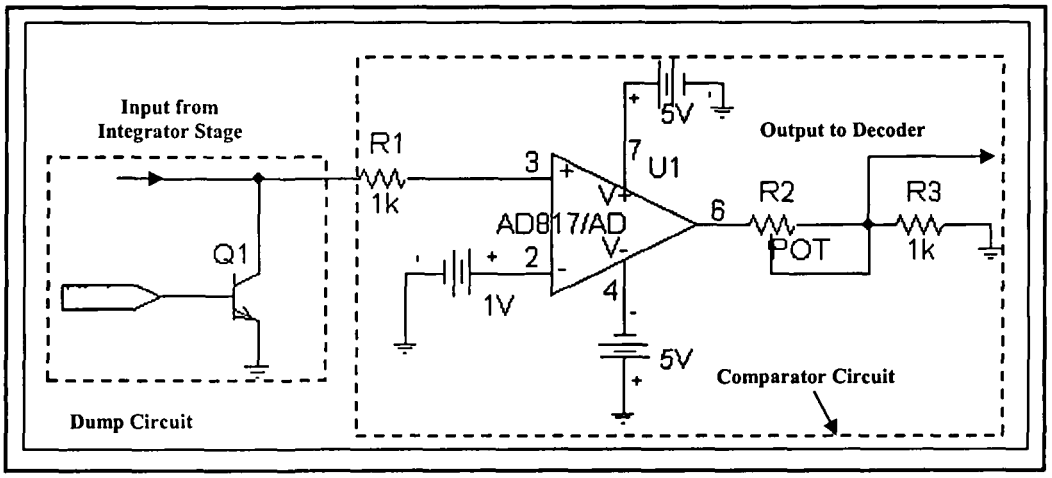

Fig.6.20: Circuit diagrams of dump and comparator

Figure 6.21 shows the simulated output obtained from comparator circuits. As discussed above, during one hop period only one BPF provides high output. The signal obtained from other BPF filters will be low. The corresponding integrator and dump will also gives high output. This high output from the integrator is applied to comparator circuit. The comparator circuit compares this signal with a preset value. Therefore, during a hop period only one comparator will provide high output and the output of remaining 14 comparators will be low. The Figure 6.21 shows the 15 pulses for the CMFSK based FHSS received which is simulated for all 15 hops and simulated for 900 microseconds as the duration of one hop is 60 microseconds.

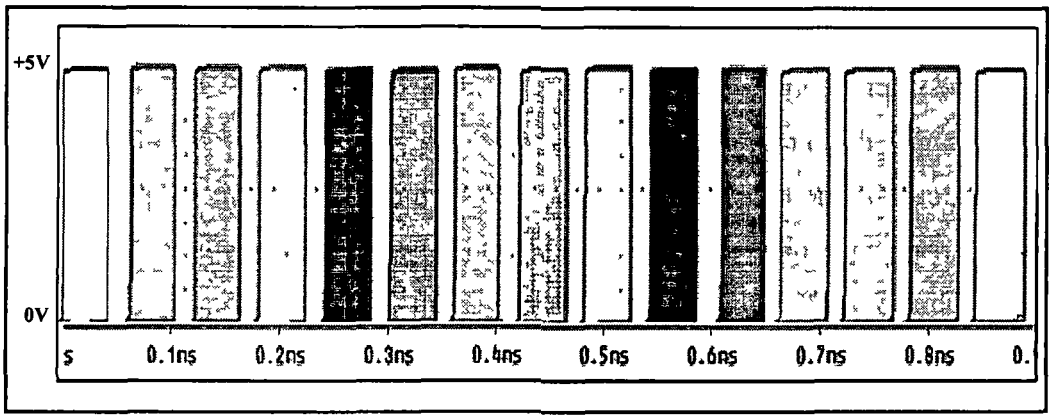

Fig.6.21: Output pulses from 15-comparators

6.5.4 Decoder

The decoder circuit decodes the output of the comparator circuit into 4-bits data word which was transmitted and 4-channels are separated. It consist of four 8-inputs OR gates and inputs to these OR gates are connected as per the Table 6.5 [19]-[20]. Same circuit has been used in Chapter 4 Section 4.5.6 and discussed in details for its working and design. Figure 6.22 shows the circuit diagram of a decoder and simulated waveforms obtained by using Microsim version 8.0 is presented in Figure 5.23.

Table: 6.5 Connection to 8-input OR gate to use it as a decoder

INPUTS	8-INPUTS OR-GATE	OUTPUTS
$A_1, A_3, A_5, A_7,$ $A_9, A_{11}, A_{13}, A_{15}$	OR Gate No $_1$	Y_0
$A_2, A_3, A_6, A_7,$ $A_{10}, A_{11}, A_{14}, A_{15}$	OR Gate No $_2$	Y_1
$A_4, A_5, A_6, A_7,$ $A_{12}, A_{13}, A_{14}, A_{15}$	OR Gate No $_3$	Y_2
$A_8, A_9, A_{10}, A_{11},$ $A_{12}, A_{13}, A_{14}, A_{15}$	OR Gate No $_4$	Y_3

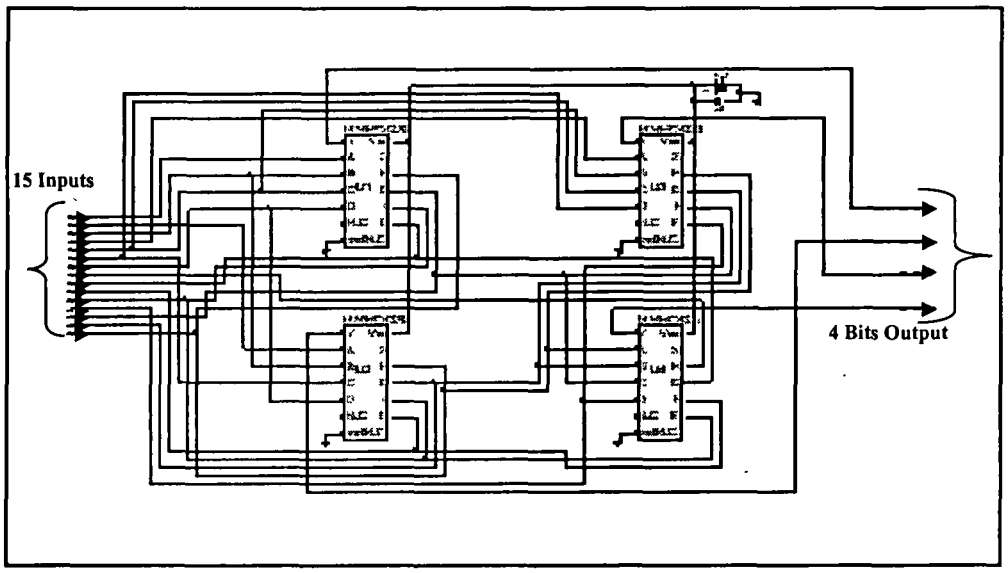

Fig. 6.22: Simulated Circuit Diagram of Decoder

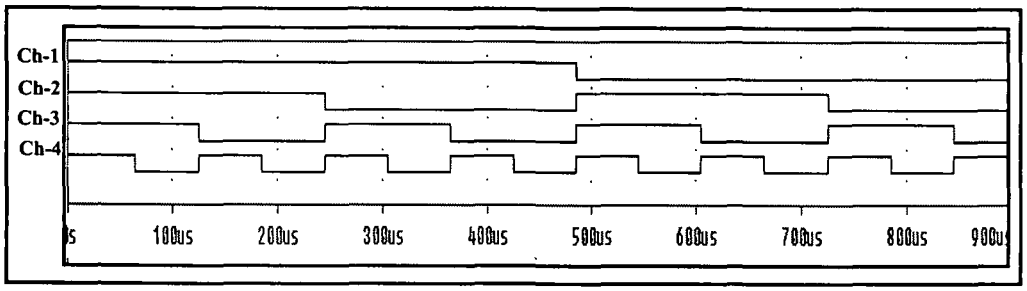

Fig. 6.23: Simulated waveform from Decoder

6.6 Simulation Results of BPF based CMFSK- Receiver

We have simulated the CMFSK based FHSS receiver for accommodating 4-users, using BPF for separating different hops. The P-Spice simulated block diagram and circuit diagrams of the receiver are given in Figure 6.24 and Figure 6.25 respectively. Figure 6.27 shows the traces generated by different circuits as signals are processed through them. Trace (a) shows the received sinusoidal signal. Trace (b) shows the outputs obtained at the output of different filters. These filter output is processed in the detector and comparator stage, trace (c) shows the output of the comparator circuit. Trace (d) shows the waveform of decoded 4-channel signals with time delay ~ 40- 55 μs which are mainly due to propagation delays in the components used in the device. It is the same signal as it was transmitted. Table 6.6 shows the different components along with specification used for different blocks of CMFHSS transmitter

Table-6.6 List of components used in CMFHSS Receiver

Block	Type	Value
Band Pass Filters	Operational Amplifiers- 15No	AD 817/AD
	Resistance - 15 No	10K Ω, 0.25W
	Capacitor- 30 No	Different Values

	Pot meters-45 No	Different Values
Detector and Integrator	Resistances-30 No	1KΩ, 0.25W
	Diode -15 No	BAS 116/SIE
	Capacitor-15 No	2.2nF
Dump and Comparator	Transistor-15 No	2N2222
	Resistance-30 No	1KΩ, 0.25 W
	Pot -15 No	4.7KΩ, .5W
	Operational Amplifier- 15No	AD 817/AD
Decoder	8-input OR gate-04	M74HC4078

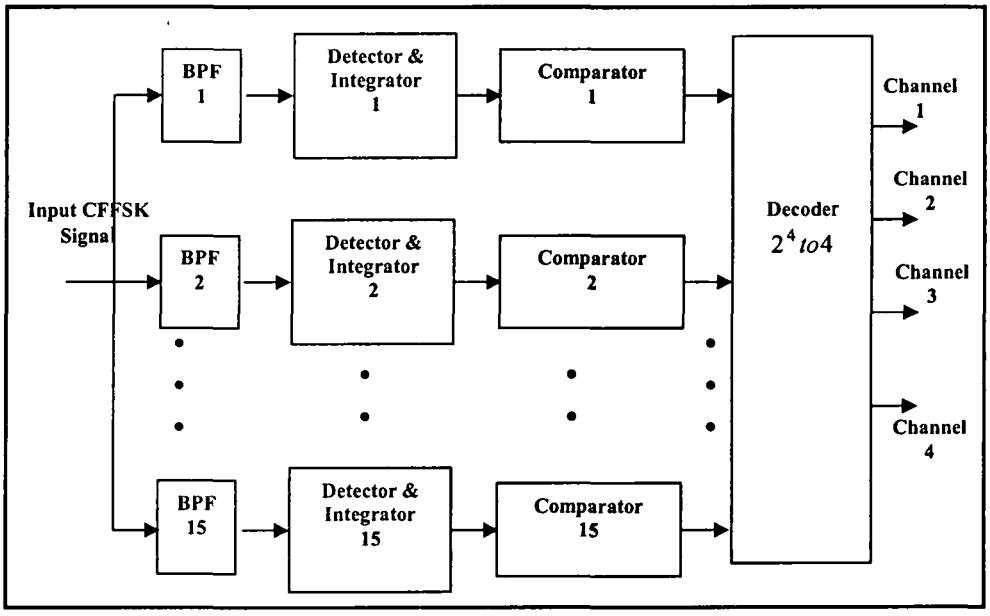

Fig.6.24: Simulated block diagram of Filter based CMFSK receiver

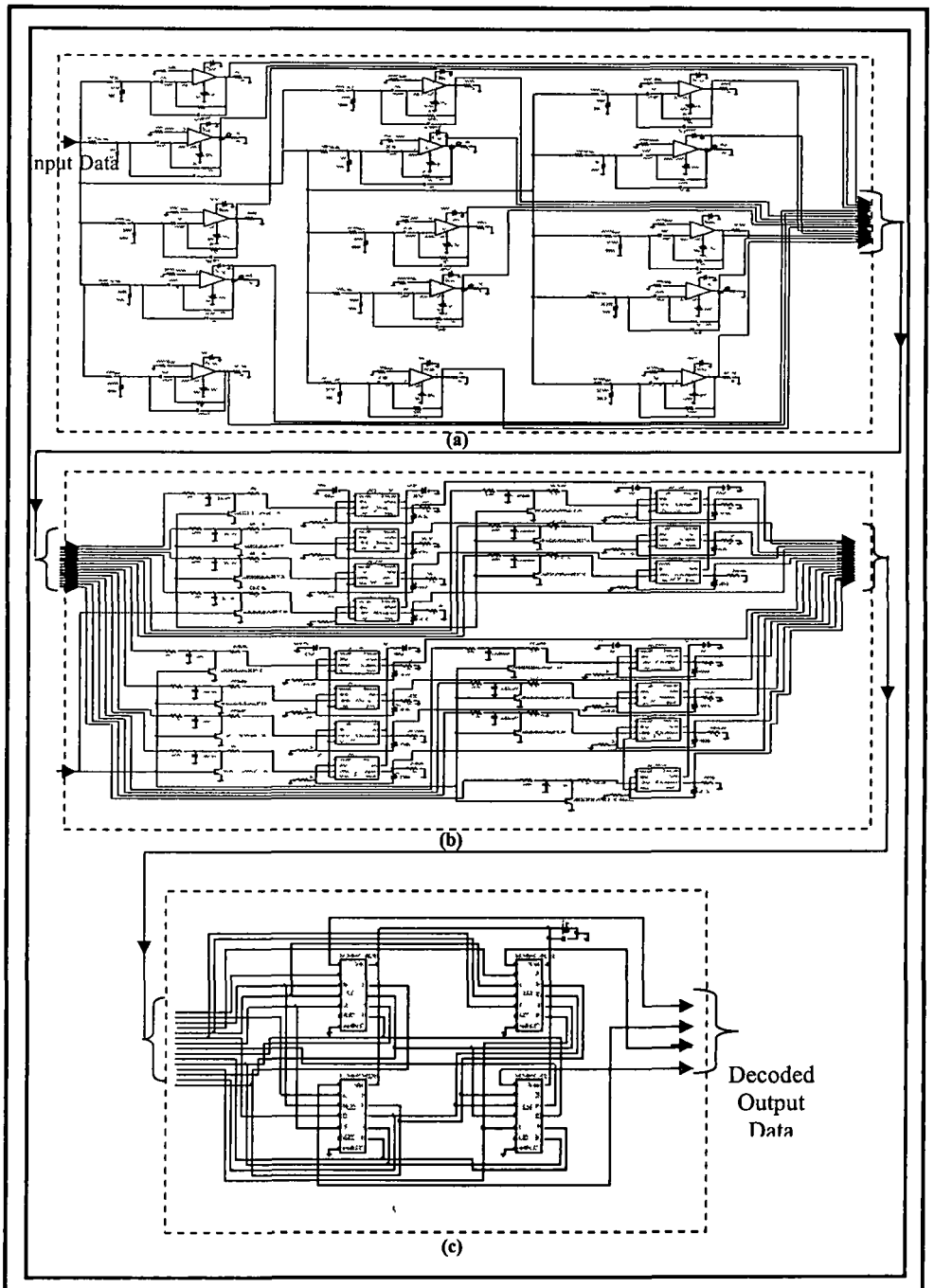

Fig. 6.25: P-Spice Simulated circuit diagram of CMFSK receiver, (a) 15 filters, (b) Integrator, dump and comparator, (c) Decoder

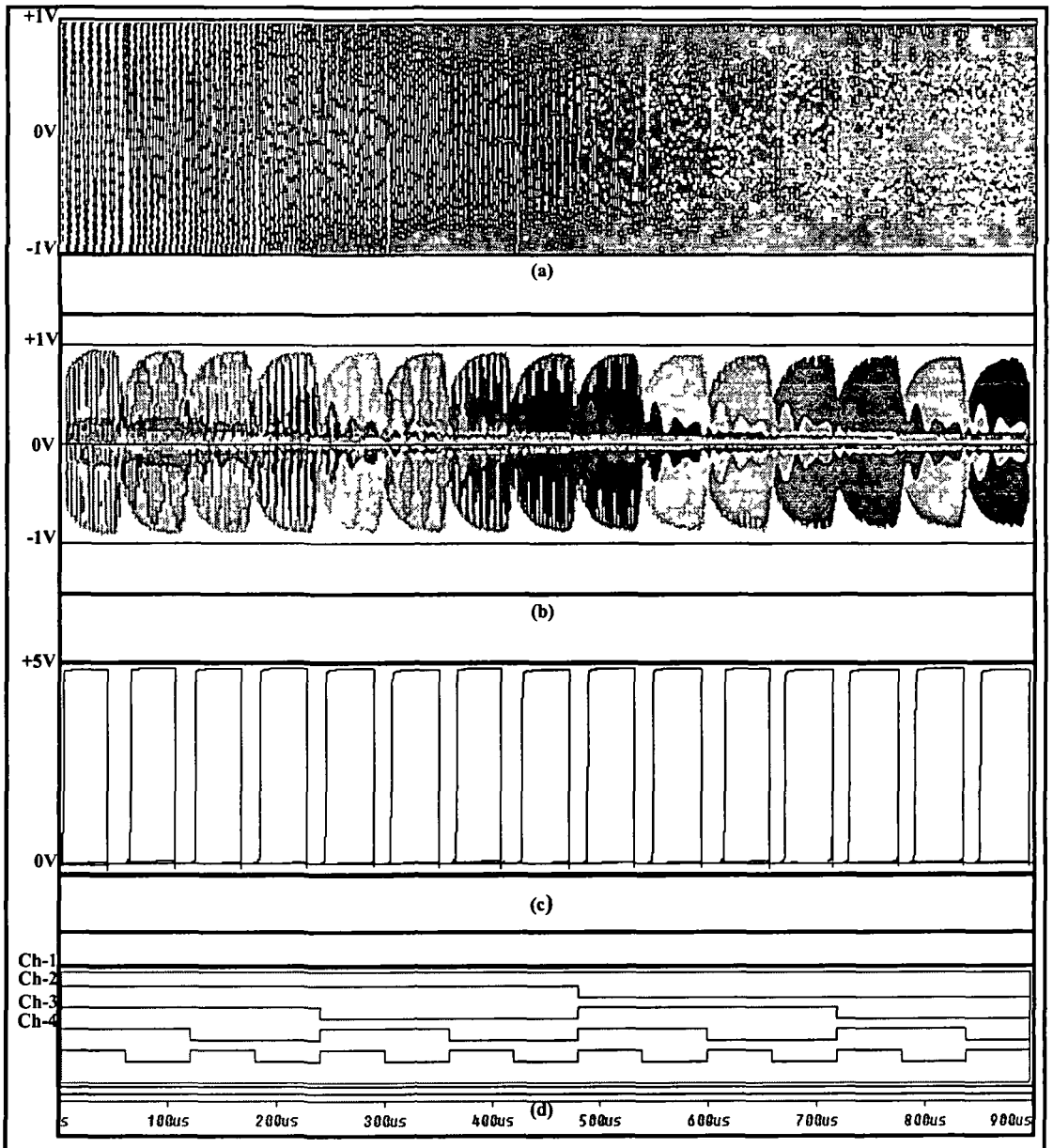

Fig.6.26: P-Spice Simulated Waveforms of the CMFHSS receiver, (a) Received Sinusoidal signal, (b) Output from BPF, (c) Output Comparator, (d) Decoded Data

6.7 CMFSK Receiver design with Frequency to Voltage Converter

For improvement of the performance of the multi channel CMFHSS system, we have tried to design the proposed FHSS system using frequency to voltage converter (FVC) [24]-[26]. The FVC based FHSS system consists of FVC, comparators, priority decoder which are discussed separately in different subsection. A FVC is a very important device that generates an output D.C. voltage proportional to the frequency of an input signal. This device is very useful and has many applications in power system control, in processing of very-low-frequency signals, and in many fields of instrumentation. For example, it can be used as a frequency meter, as a control unit in a VCO, or as a frequency- measuring device in flow meters and tachometer read outs in motor-speed controls. Previous authors had proposed many FVC [24]-[26] and many commercial integrated circuits are also available for conversion of sinusoidal signals into a proportional voltage. But these all circuits have very limited bandwidth and are unsuitable for wideband operation in the communication systems. So we have proposed and designed a wide band sinusoidal FVC based on R-C network as discussed in detail in the next section. This proposed FVC is used for demodulating the M-ary FHSS signal which has reduced the banks of BPF and circuit is reduced to simple and small in size [27].

6.7.1 Frequency to Voltage Converter Principle

The proposed sinusoidal FVC is based on series R-C differentiator as shown in Figure 6.27 [28]. This series R-C network is a high pass filter and allows the high frequency sine waves to pass unhindered from its input to its output, but the amplitude of lower frequency is reduced. It is because of the reactance of the capacitor (X_C) and the resistance of the resistor (R), act as a potential divider placed across the input, with the output signal taken from the centre of the two components. Under certain condition the

signal voltage across (R) will be equal to the differentiation of the input signal. This is the basic principle of this proposed FVC. There are also many FVC proposed for digital signal in the literature [30]-[35].

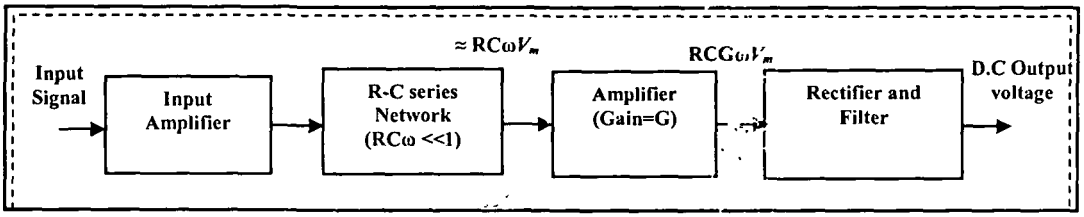

Fig. 6.27: Block diagram of proposed FVC

The received signal is amplified using the amplifier to a level sufficient to drive the successive stage. In wireless communication systems the front end receiver is generally automatic gain controlled (AGC) to maintain the constant magnitude of the received signal. Also first stage is a low noise amplifier (LNA) to keep the SNR ratio high for better performance. In this design we have amplified the signal generated by the transmitter with the wide band amplifier AD 817/AD before it is applied to FVC stage.

The proposed FVC composed of an R-C series network, amplifier, absolute value output circuit, and filter circuit. A sinusoidal input signal $V_{in}= V_m$ Sin (ωt) (where V_m = peak voltage and ω= angular Frequency = $2\pi f$ and f =frequency) is applied in RC series circuit. In the figure, the RC network acts as a high pass differentiator in which the output voltage is $V_R \approx RC\frac{dV_{in}}{dt}$. From the circuit analysis, the voltage drop (V_R) across the series resistance, (R) increases with frequency (f) due to decrease in impedance of the capacitor as given by Equation (10).

$$V_R = K(f).f \tag{6.10}$$

$$\text{where, } K(f) = \left(\frac{2\pi RCV_m}{\sqrt{1+4\pi^2 f^2 R^2 C^2}}\right) \tag{6.11}$$

If $4\pi^2 f^2 R^2 C^2 << 1$ (which corresponds to more capacitive impedance than resistance value of RC circuit), then from above Equation (5.9),

$$V_R \approx 2\pi V_m f RC = K_0 . f \tag{6.12}$$

where, $K_0 = 2\pi V_m RC$ =linearity constant.

The linearity error is defined as

$$\text{Linearity error} = \frac{K_0 - K(f)}{K_0} \times 100\% \tag{6.13}$$

The voltage dropped across the resistance R, V_R is then fed to the voltage amplifier to raise the amplitude sufficiently before it is fed to absolute value rectifier [23] which rectifies the sinusoidal signal into pulsating D.C signal. The amplifier amplifies this voltage by gain (G). The absolute value output circuit which provides positive peak value approximately same as the input peak value and finally filter circuit is used for reduction of ripples. Amplifier and rectifier circuits are designed by using high speed amplifier AD 817/AD [21]. Filter based RLC network gives the D.C. voltage which is proportional to the frequency of the input signal. Figure 6.28 shows the P-Spice simulated circuit diagram.

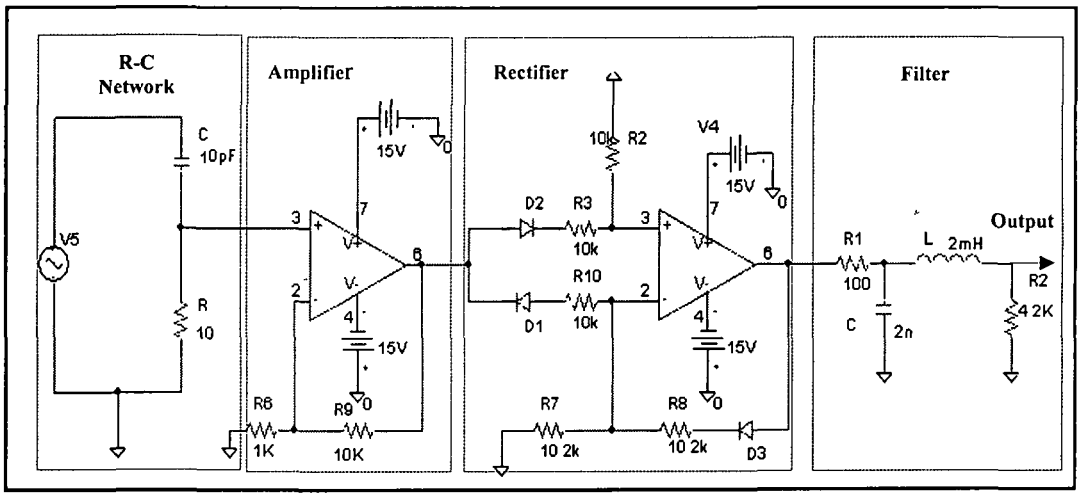

Fig.6.28: Circuit diagram of the proposed FVC

6.7.1.1 Linearization of FVC

Figure 6.29 shows the voltage (V_R) across a series resistance R in series R-C networks with input frequency to FVC obtained by using P-SPICE simulation. The series RC network was simulated with frequency range 0-200 MHz for different values of C and R. It is seen from the figure that all curves show linearity up to 10 MHz as it satisfies the linearity condition ($4\pi^2 f^2 R^2 C^2 << 1$). Beyond 10 MHz up to 200MHz, the curves for R=10 Ω, C =100pF and R=10 Ω, C =200pF are not linear and it is made linear (Figure 6.29) after satisfying linearity condition with R=10 Ω and C =10pF. So R=10 Ω and C=10 pF were chosen for the design of linear sinusoidal FVC with operating frequency up to 200 MHz. The figure also shows the linearity error (%) versus frequency (up to 200 MHz) obtained by using the equation (3). It is seen that linearity error for R=10 Ω, C=10 pF is almost negligible up to 100 MHz and slightly increases with frequency after 100 MHz.

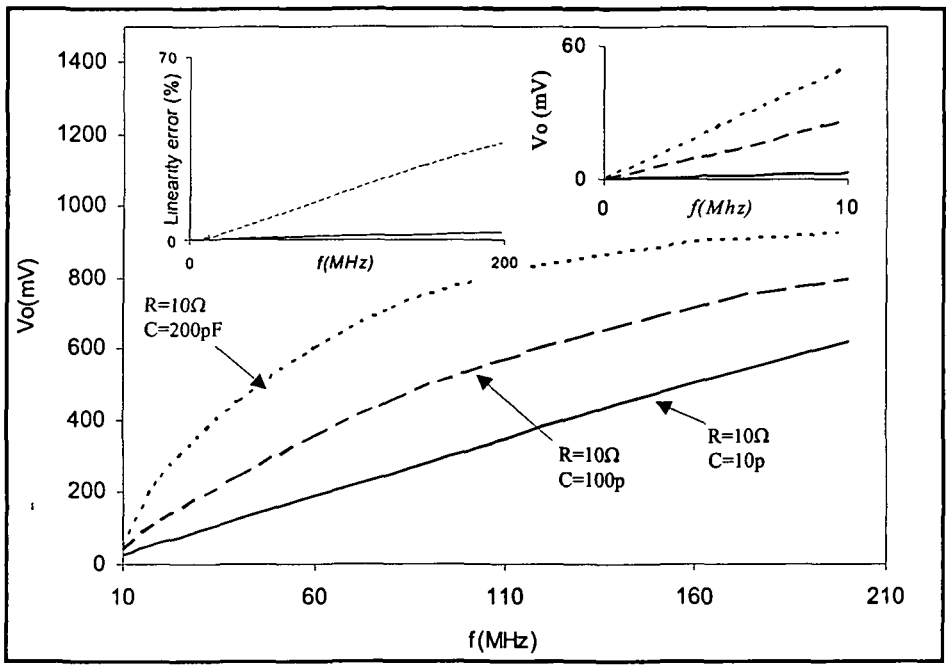

Fig. 6.29: Linearization of proposed FVC

Figure 6.30 shows dependence of linearization and sensitivity (V_0 / f), where V_0 = output voltage (mV) of FVC, f = frequency (MHz) on change of capacitance (ΔC) up to 5 pF (which is normally considered due to parasitic effect. It is seen from the figure that linearity error for f=50 Hz and 100 MHz are ~ 0.18 % and 0.25 % respectively which are almost constant with $\Delta C/C$ but for 200 MHz linearity is slightly more and it increase with $\Delta C/C$. It is concluded that linearity is not affected much by parasitic effect up to frequency 100 MHz. It is also seen that the sensitivity remains constant with frequency up to 150 MHz but sensitivity is slightly affected with ΔC as the output voltage is directly proportional to capacitance. It was concluded (not shown in the Figure) that similar type of behavior was obtained with change of resistance due to parasitic effect.

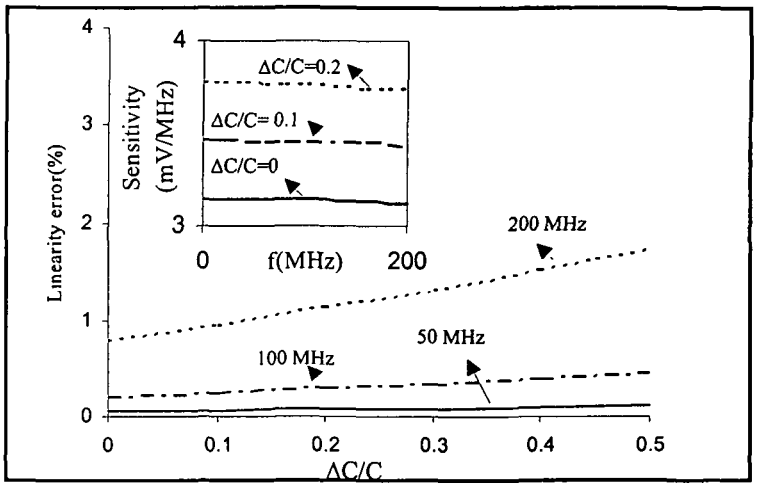

Fig.6.30: Dependence of sensitivity and linearization on small change of capacitance in RC network due to parasitic effect

6.7.1.2 Ripples Calculation

The ripples are produced at the output of the FVC due to the sinusoidal nature of rectification. To reduce these ripples to an acceptable level a passive filter using RLC

shown in Figure 6.31 is used [23] . The ripples available in the output are determined by using the Fourier series analysis with the full wave rectified signal as input voltage to filter using KVL.

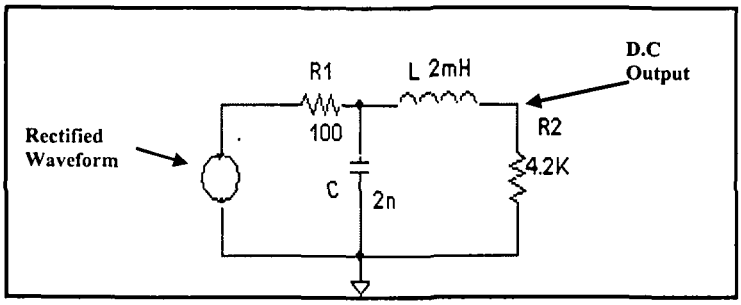

Fig.6.31: Circuit diagram of filter circuit [23]

Figure 6.31 represents the circuit of the filter where the input voltage is the rectified output obtained from the absolute value rectifier circuit. Using Fourier series analysis [28]-[29], the input to the filter can be written approximately as:

$$\approx \frac{2V_{Rect}}{\pi} - \frac{4V_{Rect}}{3\pi} Cos2\omega t \qquad (6.14)$$

where $V_{Rect} = \omega RCGV_m Cos\omega t$. It is the input voltage to filter, obtained across resistance R of R-C network. The higher terms in the Fourier series representation in equation (5), are neglected because of very low magnitude. In steady state condition, by applying Kirchhoff's voltage laws (KVL) to Figure 6.31. The Equation for current I_1 and I_2 can be written as:

$$I_1(j\omega R_1 + 1) - I_2 = j\omega C_1 V_{Rect} \qquad (6.15)$$

$$I_1 - I_2(1 - \omega^2 LC + j\omega R_2 C_1) = 0 \qquad (6.16)$$

From the Equations (7) and (8) I_2 is obtained as:

$$I_2 = \frac{-jC_1V_{Rect}}{\left(\omega LC_1 + \omega R_2R_2C_1^2\right) + j\left(\omega^2R_1LC_1^2 - R_1C_1 - R_2C_1\right)} \tag{6.17}$$

The ripple voltage is obtained by multiplying the current I_2, obtained from Equation (6.17), and resistance R_2 as shown in Figure 6.31.

$$V_{ripple} = \frac{R_2C_1V_{Rect}}{\sqrt{\left\{\left(\omega LC_1 + \omega R_1R_2C_1^{\,2}\right)^2 + \left(\omega^2R_1LC_1^{\,2} - R_1C_1 - R_2C_1\right)^2\right\}}} \tag{6.18}$$

Using above Equation (6.18) we have estimated the ripple volt (V_{ripple}), for the proposed circuit for frequency range from 400 Hz – 5 MHz as shown in Figure 6.32. The figure shows that the variation of ripple voltage with frequency obtained by using the Equation (6.13) in PSPICE simulation waveforms (as shown in Figure 6.32) is almost close to that obtained by using the Equation (6.18). It is also seen that the rate of decrease of ripple voltage with frequency is more up to 1 MHz and after 1 MHz it decreases slowly with frequency. So the proposed FVC circuit has a lower ripple voltage for frequency > 1 MHz. The black dots represent the experimental value of ripple voltage (at frequency 1 MHz and 4 MHz).

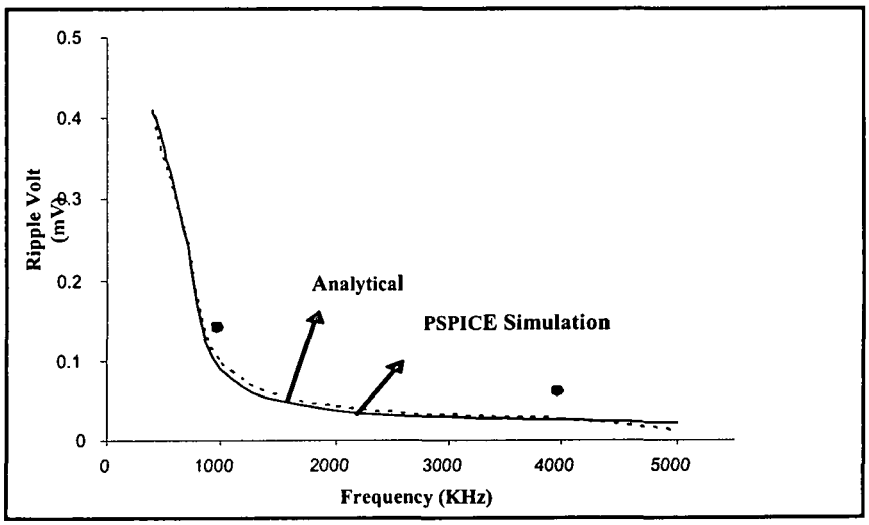

Fig.6.32: Ripple voltage vs. frequency for R_1=100 ohm, R_2= 4.2K Ω using PSPICE and analytical simulation

6.7.1.3 Response Time

From Equation (6.14), output of full wave rectifier can be assumed as obtained by summing D.C. voltage source of magnitude $-\frac{2V_{Rect}}{\pi}$ with a sinusoidal voltage source. The frequency of this assumed sinusoidal source is twice of FVC input signal and magnitude as $-\frac{4V_{Rect}}{3\pi}$. The response of the filter is determined from these two inputs by transient and steady-state analysis of the filter circuit [28]. There are two types of currents flowing in the output resistance R_2. The current $I_{2(step)}$ is due to step source voltage and $I_{2(\cos)}$ is due to second harmonic voltage. Finally, the output voltage across resistance R_2 is obtained as $V_{R2} = I_2 R_2$

$$V_{R2} = \frac{2V_{Rect}R_2}{\pi(R_1+R_2)} - K_1 e^{-s_1 t} - K_2 e^{-s_2 t} + \frac{4V_{rect}R_2}{3\pi Z} Sin(2\omega t - \theta) - K_3(\theta,\omega)e^{-s_1 t_1} - K_4(\theta,\omega)e^{-s_1 t} \tag{6.19}$$

where, $Z = \sqrt{\{(R_1+R_2) - 4\omega^2 LC_1)^2 + (2\omega L + 2\omega R_1 R_2)^2\}}$,

$\theta = -\tan^{-1}\left(\frac{2\omega L + 2\omega R_1 R_2 C_1}{R_1 + R_2 - 4\omega^2 LC_1}\right)$,

$V_{Rect} = \omega RCGV_m Cos\omega t =$ rectifier input. The s_1 *and* s_2 are the roots of characteristic equations obtained from KVL analysis of Figure 6.31.

It is also seen that $\frac{2V_{Rect}R_2}{\pi(R_1+R_2)} >> \frac{4V_{Rect}}{3\pi Z}$ for higher frequency (MHz range is considered as operating frequency range). So V_{R_2} is approximately written as:

$$V_{R_2} \approx V_0[1 - De^{-s_1 t}] \tag{6.20}$$

where $V_0 = \frac{2V_{Rect}R_2}{\pi(R_1+R_2)}$ and $D = \frac{\{K_1 + K_3(\theta,\omega)\}(R_1+R_2)}{2V_{Rect}R_2}$

From the definition, response time ($t_{Response}$), of a system is the time required to reach 99% of its maximum value V_0. So the response time can be written from the Equation as:

$$t_{res} \approx \frac{4.605}{S_1} + \frac{1}{S_1}\ln[D] \qquad (6.21)$$

The response time for R_1=100 ohm, R_2= 4.2 K ohm, L=2 mH, C_1 = 2nF has been estimated as 2.09 μ second which is almost very close to that obtained in P-Spice simulation. Figure 6.33 shows the dependence of response time and ripple voltage on LC_1/ R_2 for frequency 1 MHz. It is seen that the ripple voltage decrease with the increase of LC_1/ R whereas the response time increases with increase of LC_1/ R_2. In the Figure, the optimum value of LC1/ R_2 is obtained as ~ 1.8 x 10^{-12} second^2/ohm which corresponds to R_2= 4.2 K ohm, L=2 mH and C1 = 2nF. The black dot and cross signs in Figure 6.33 shows.

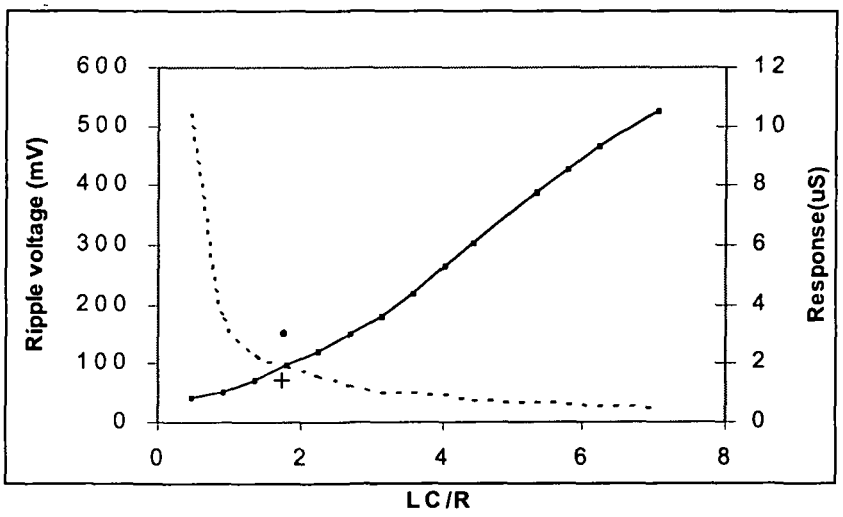

Fig.6.33: Dependence of response time and ripple voltage on LC/ R_1

After discussing the principle of proposed FVC, and testing its linearity, ripples in the output voltage and response time, we have used this circuit in the 4-channel CMFHSS receiver. The proposed block diagram of FVC based CMFHSS receiver is given in

Figure 6.39. The different hops generated by the VCO as CMFSK based FHSS signal (discussed in Section 6.3.3) are applied to FVC and processed as discussed in Section 6.7.1. The input and output waveforms of the FVC are shown in the Figure 6.34. The waveform (a) represents the signal

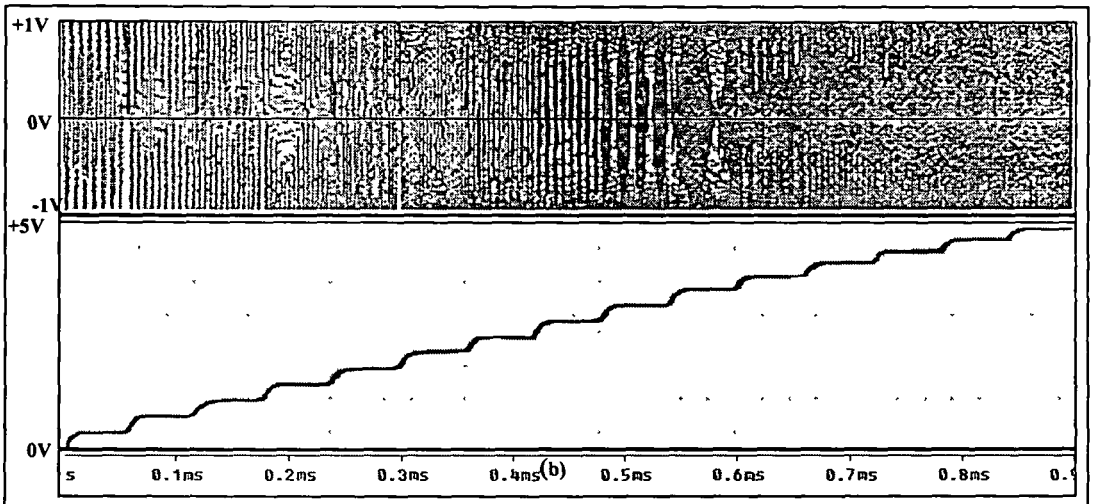

Fig.6.34: Input and output to FVC based FHSS Receiver (a) Sinusoidal inputs to FVC (b) D.C. output from FVC

6.7.2 Comparators

The output of FVC is a D.C voltage proportional to the input frequency which is applied to comparator circuit for comparing it with the preset value. Comparator circuit compares the output of the FVC using operational amplifier AD817/AD as shown in Figure 6.36. There are 15 such circuits for comparing the output of FVC into 15 different levels. FVC output is connected to all comparator and each comparator is tuned to give high output at preset level only. Like this all the correlators are tuned one by one and when highest frequency is received in that condition the output of all the comparators will be high and when lowest hop frequency is received for that only one correlator will gives high output. The output of all other comparators will be low only during this state only. Figure 6.35 shows the simulated circuit diagram for one

comparator. Likewise 15 circuits are used to compare the output of FVC with the preset value. Figure 6.36 shows the simulated output waveforms for all 15 comparators, one for each 15 hop frequency.

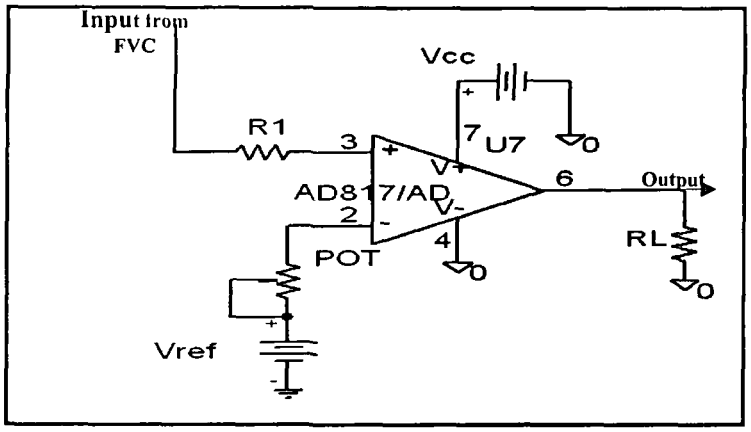

Fig.6.35: Circuit diagram of comparator

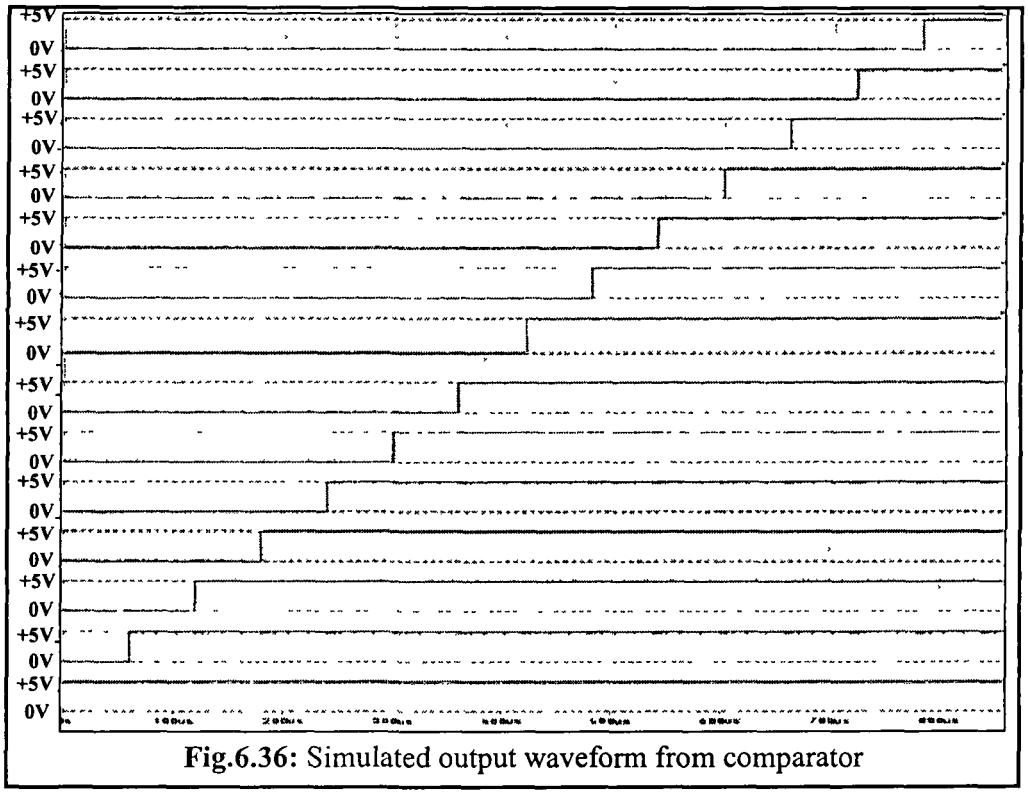

Fig.6.36: Simulated output waveform from comparator

6.7.3 Priority Decoder

Priority encoder is a circuit that reduces many binary inputs into a smaller number of outputs [19]-[20]. The output of a priority encoder is the binary representation of the ordinal number starting from zero of the most significant input bit. If two or more inputs are high at a time, the highest priority will take precedence. The truth table for the decoder is given in Table-6.7.

Table: 6.7 Truth Table for 16 to 4 Priority Decoder

C_{15}	C_{14}	C13	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	D	C	B	A
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The 15 outputs of the correlator are encoded into 4-bit binary output using the priority encoder with the help of integrated circuit HCF4532B which is 16 pin in 16-lead dual in-line plastic package. It consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each

have an assigned priority. D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input El is low. When El is high, the binary representation of the highest priority input appears on output linesQ2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (EO) is high when no priority inputs are present. If anyone input is high, EO is low and all cascaded lower-order stages are disabled. Table-6.6 shows the truth table of the decoder.

Table: 6.8 Truth table of HCF 4532B [14]

Input									Output				
E_I	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_O
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	0	0
1	0	1	X	X	X	X	X	X	1	1	1	1	0
1	0	0	1	X	X	X	X	X	1	1	0	0	0
1	0	0	0	1	X	X	X	X	1	1	0	1	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 = High Logic 0 = Low

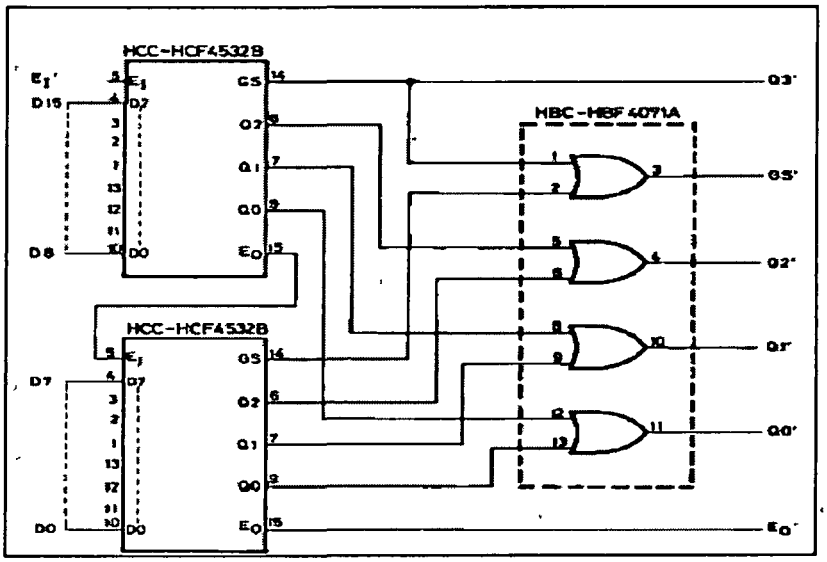

Fig.6.37: IC HCF4532 for 16 to 4 Priority decoding.[21]

Integrated circuit HCF 4532B provides cascading feature to handle more number of inputs, therefore by cascading two HCF 4532B, 16 to 4 priority decoder is implemented. Figure 6.37 shows the pin connection diagram for cascading and achieving the 15 inputs for decoding into 4 channels. The simulated waveforms are shown in Fig-6.38 for the priority encoder stage. These waveforms show all states of a 4 bit data word, from state 1111 to 0001 as it was transmitted by CPSK based transmitter. The transmitted 4 bit data word is shown in Figure 6.26 by trace (d). In this way, we have decoded the same data as it was transmitted by the proposed transmitter for 4-channel multiplexing.

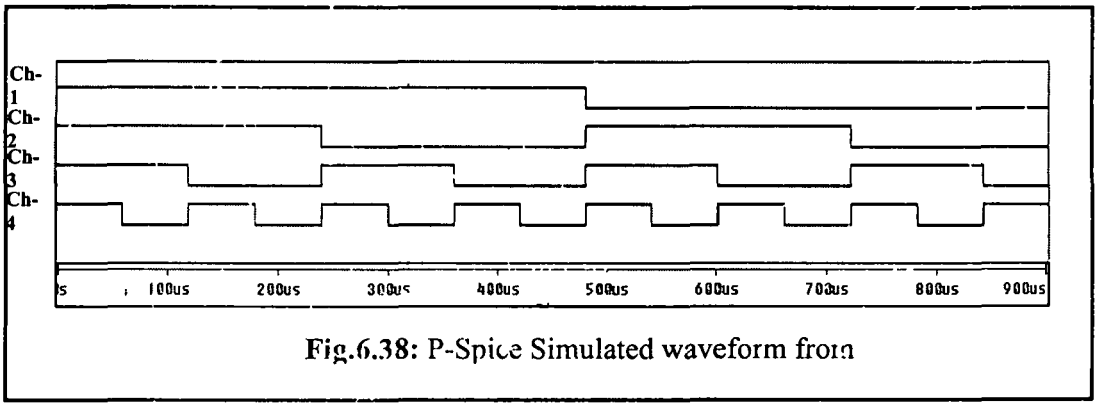

Fig.6.38: P-Spice Simulated waveform from

6.8 Simulation Results of FVC based CMFSK Receiver

We have simulated the 4-channel MFSK based FHSS receiver for separating the 4-users using proposed FVC. Table-6.9 shows the components with specification used in the design and simulation of the FVC based CMFHSS receiver. The block diagram and P-Spice simulated circuit diagram of the receiver are given in Figure 6.39 and Figure 6.40 respectively. The each stage of receiver has been discussed with simulated circuit diagram and waveform obtained from the simulation. The data transmitted by 4-users simultaneously decoded in the designed receiver The PN generating circuit generates PN sequences with a chip of 4 micro seconds duration. In a PN sequence there are 15

chips, and making the PN duration equal to 60 micro seconds. The proposed CMFSK receiver also designed and simulated using proposed wide band sinusoidal FVC. In both cases receiver was simulated upto 20 MHz frequency with using different hop sizes.

The Figure 6.41 shows the different waveforms at the different stages of the receiver. In this Figure waveform (a) shows the input sinusoidal signal changing with hop of 300 KHz. The duration of each hop is 60μsecond. Wave from (b) shows 15 outputs from the FVC one for each hop of frequency. The total output is varying from 1.0 volts to 4.5 volts as shown by trace (b). Waveform (c) shows the output of comparator which converts the FVC output to +5 volts logic which is processed by the priority encoder as per Table-6.7. Waveform (d) shows the separated 4-chanels indicating same delay as obtained in BPF based transceiver. The improvement of BER performance by FVC based transceiver over BPF based transceiver is shown in chapter-7.

It is required to test the performance of designed CMFHSS transceiver under noise and jamming. We have discussed the performance analytically and with simulation model discussed in the Chapter 7.

Table-6.9 List of components used for FVC Based CMFHSS Receiver

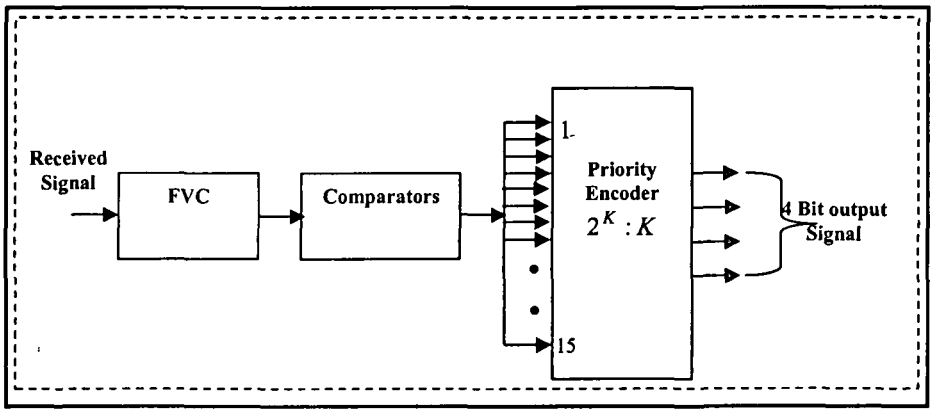

Fig.6.39: Simulated Block diagram of receiver with proposed FVC

Table-6.9 List of components used for FVC based CMFSK receiver

Block	Type	Value
FVC	Op-Amplifier- 2No	AD 817/AD
	Resistance - 10 No	Different values
	Capacitor- 02 No	Different values
	Diode -03	IN4148
	Inductor-01	2mH
Comparator	Op-Amplifier-15No	AD 817/AD
	Resistance - 30 No	0.25W
	Pot-15No	0.25W
Encoder	Priority Encoder-02No	HCF 4532B
	2 Input OR gate-01No	HBF 4071

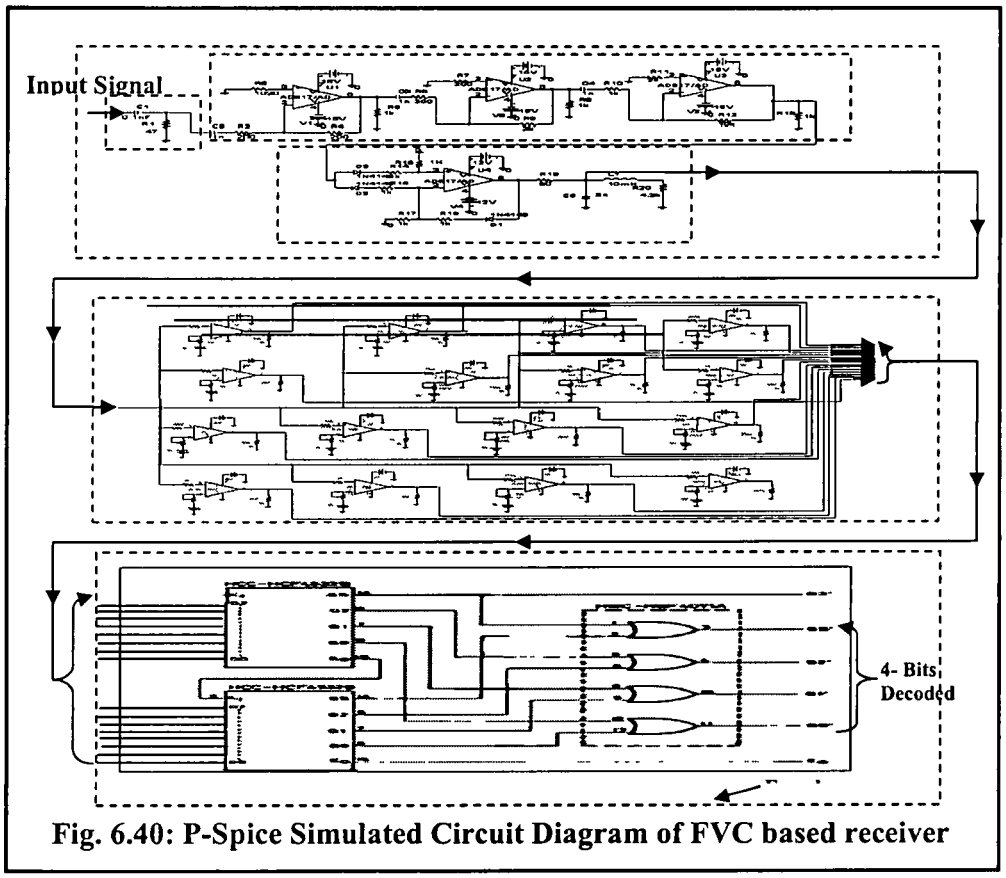

Fig. 6.40: P-Spice Simulated Circuit Diagram of FVC based receiver

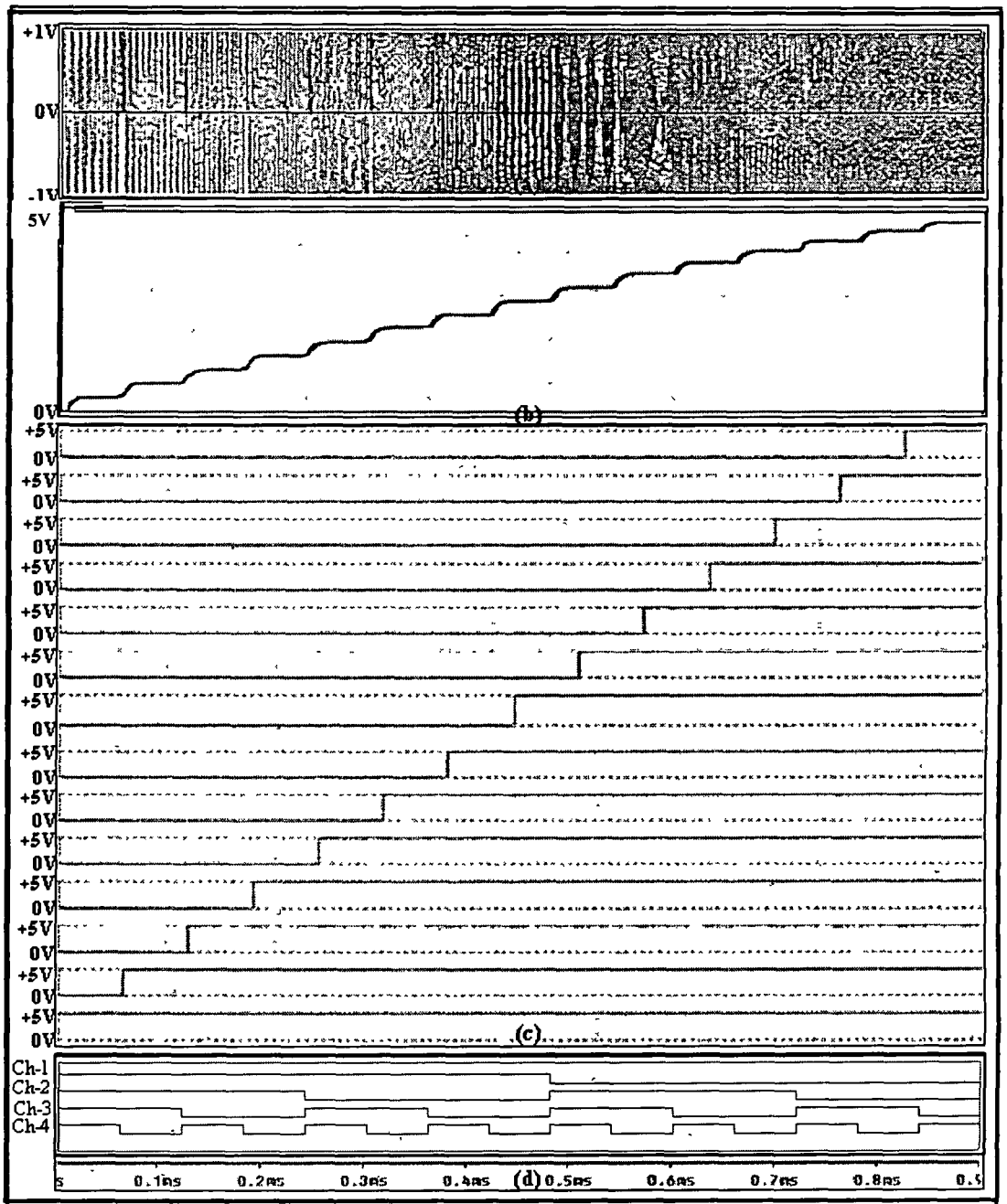

Fig-6.41 P-Spice Simulated Waveforms of the CMFHSS receiver, (a) received sinusoidal signal, (b) Output from FVC, (c) Output comparator, (d) Decoded data

6.9 Conclusion

In this chapter, we have designed and simulated the BPF based CMFSK transceiver for multiplexing 4-users on same channel using commercial Microsim software version 8.0. We have used M-ary modulation techniques for multiplexing 4-users with FHSS system. The transmitter frequency was changing from 300 KHz to 4500 KHz in linear hop steps of 300 KHz. For separating the 4-channles in the receiver we have designed the receiver using BPF. The proposed wide band sinusoidal FVC was tested for its linearity, response time and ripples in the output. The FVC provide linear output and fast response time over a wide band of 100MHz. It is also seen that the separated signal of four channels obtained FVC based receiver shows same delay of 40-55 μs as obtained in BPF based transceiver. The improvement of BER performance by FVC based transceiver over BPF based transceiver is shown in chapter-7.

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Chapter 7

Performance Evaluation of CMFSK based FHSS System

7.1 Introduction

In Chapter 6 we have proposed the designed coded M-ary FHSS system for multi-user applications. The system was designed and simulated by using Microsim software 8.0 for multiplexing 4-users on a transmission media. It is also required to study the performance of the designed circuit under additive white Gaussian noise (AWGN) and jamming signal [1]-[8]. It has been discussed in chapter 4 and chapter 5, that the DSSS system does not performed well under jamming signal. Therefore, in this chapter we have studied the performance of the proposed multi-channel CMFSK based FHSS [9-12] system designed in Chapter 6 under additive white Gausian noise (AWGN) and jamming [3]-[4].

The Chapter is organized as follows. In section 7.2 theoretical evaluation of symbol error rate (SER) and bit error rate (BER) performance [5] of the designed FHSS system under AWGN and jamming has been investigated. The FHSS device was tested with simulation model under different AWGN condition and simulated result are discussed in Section 7.3. Section 7.4 presents the performance analysis of designed device with proposed frequency to voltage converter (FVC) using P-Spice simulation. Section 7.5 presents the eye diagram analysis for noise margin and distortion . In section 7.6 the comparison between the CPSK based DSSS and CMFSK based FHSS is presented. Section 7.7 shows the experimental traces obtained from experimental measurement. Finally, the conclusion of the Chapter is presented in Section 7.8.

7.2 Analytical Performance of CMFSK based FHSS system

As discussed in Chapter 6, the coded M-ary frequency shift keying (CMFSK) [1]-[5] based FHSS system has been designed for multi-user wireless communications. In wireless communication the designed systems are tested for its performance under AWGN and jamming resistance. The noises (mainly AWGN) are coupled to system from channel and after mixing with the desired signal, alter its characteristics [7]. This

will results in the system performance degradation. The system performance analytically is measured in terms of symbol error rates/bit error rates (SER/BER) [3].

7.2.1 Symbol Error Performance under AWGN

The received signal $r(t)$, at the input of the receiver is expressed as [4]-[5].

$$r(t) = s(t) + n(t) \tag{7.1}$$

where $s(t)$ is the signal and $n(t)$ is the AWGN noise.

For m th symbol, the probability of symbol error (SER) is given by,

$$P_s(m) = \sum_{\substack{i=1 \\ i \neq m}}^{M} P(S_m(t, f_m), S_i(t, f_m)) \tag{7.2}$$

where, $P(S_m(t, f_m), S_i(t, f_m))$ = the probability of the receiver mistaking for $S_m(t, f_m)$ and it is written as:

$$P(S_m(t, f_m), S_i(t; f_m)) = \int_{d_{mi}/2}^{\alpha} \frac{1}{\sqrt{\pi N}} \exp(-\frac{v^2}{N}) dv \tag{7.3}$$

where d_{mi}=Euclidean distance between $S_i(t, f_m)$ and $S_m(t, f_m) = \| S_m(t, f_m) - S_i(t, f_m) \|$.
Considering complementary function, we can write the Equation (7.3) as:

$$P(S_m(t, f_m), S_i(t, f_m)) = \frac{1}{2} erfc\ (\frac{d_{mi}}{2\sqrt{N}}) \tag{7.4}$$

From the Equation (7.2) and (7.4), we can write

$$P_s(m) = \frac{1}{2} \sum_{\substack{i=1 \\ i \neq m}}^{M} erfc\ (\frac{d_{mi}}{2\sqrt{N}}) \tag{7.5}$$

The probability of SER for CMFSK signaling is written as

$$P_s = \sum_{m=1}^{M} p_m P_s(m) \tag{7.6}$$

where p_m = probability of transmitting mth symbol.

Considering $p_1 = p_2 = \cdots = p_m = \cdots = \frac{1}{2^K}$, we can write the Equation (7.6) as:

$$P_s = \frac{1}{2^{K+1}} \sum_{m=1}^{M} \sum_{\substack{i=1 \\ i \neq m}}^{M} erfc\left(\frac{d_{mi}}{2\sqrt{N}} \right) \tag{7.7}$$

The Equation (7.7) represents the SER.

Figure 7.1 shows the SER plot for M-ary signaling with FSK/FHSS system. It is seen from the plot that as M increased from 2 to 4, SER performance improves. But at the same time the bandwidth of channel also increases.

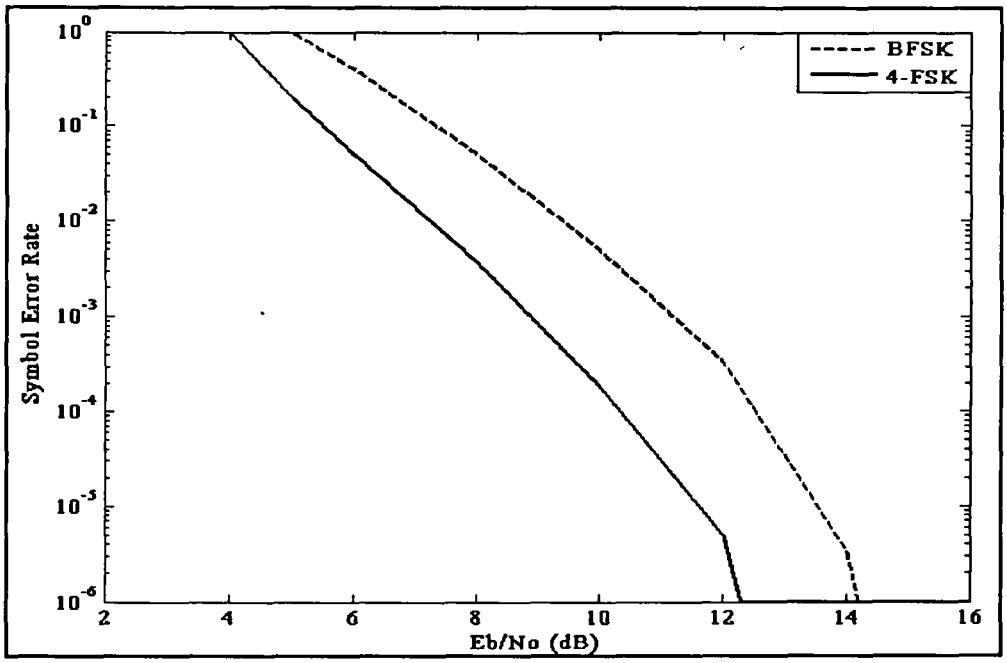

Fig.7.1: SER versus SNR, for M-ary

7.2.2 Bit Error Rate obtained from Symbol Error Rate

If the symbol consists of a single bit, as in BPSK, then both the BER (P_e) and SER (P_s), are same. In case, system encodes K bits into M-symbols with $M = 2^K$ then, P_s and P_e are not same [5]. In such condition the BER is calculated from SER. When K-bit symbol is received with error, it may be that, 1 bit or 2 bits or that all K bits are in error. If we assume that the probability P_e, of receiving any of these erroneous symbols is the

same then to assess the noise performance of a digital pass band transmission system, the average probability of SER is used. Therefore, BER is written in terms of SER as [5].

$$BER = SER\left(\frac{2^{K-1}}{2^K - 1}\right) \tag{7.8}$$

From Equation (7.8), we see that as K increases, the BER decreases as shown in Figure 7.2. The decrement is not linear, rather it decrease exponentially as number of users increases. The Figure shows the variation in BER with K=2 and K=4. It is seen from the plot that with SNR =10dB, the two user system (2-FSK) provides a BER ~ 10^{-2} whereas, 4-FSK system provides improved performance as BER~ $0.8x10^{-3}$.

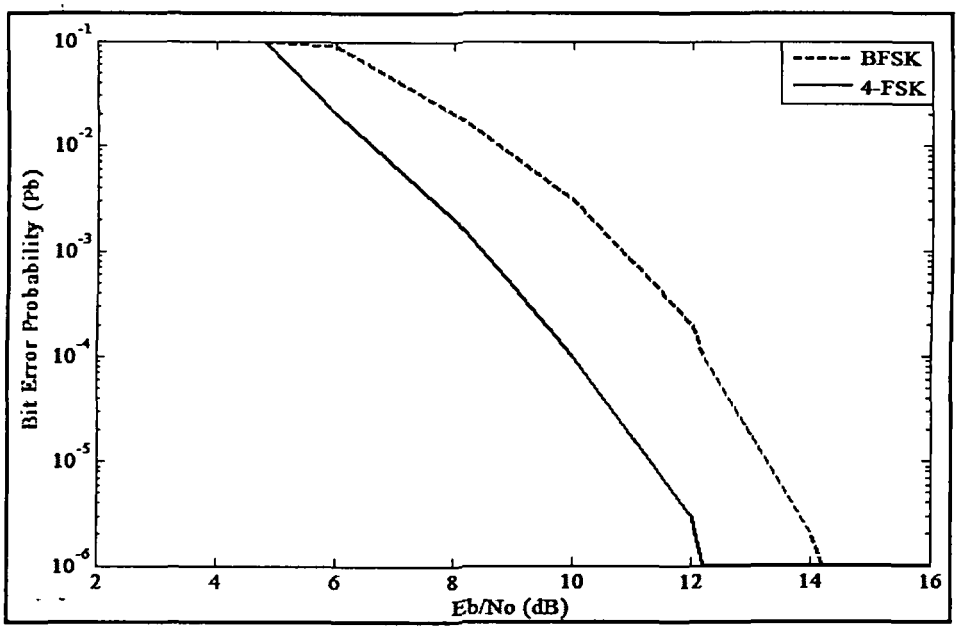

Fig.7.2: Plot for BER for M-ary FSK

7.3 SER from Simulation Model

Figure 7.3 shows the block diagram of simulation model for SER analysis. Simulation model consists of data generator, CMFSK transmitter, CMFSK demodulator, AWGN generator (2 kHz –25 MHz), comparator and signal generator. The data generator

generates the signal which are coded and transmitted by CMFSK transmitter as discussed in Chapter 6. For noise performance analysis the CMFSK signals are mixed with AWGN source and fed to the CMFSK receiver. CMFSK receiver processes the signal and demodulates into output data (decoded data). Depending upon the magnitude of SNR, errors are generated at the output of the receiver.

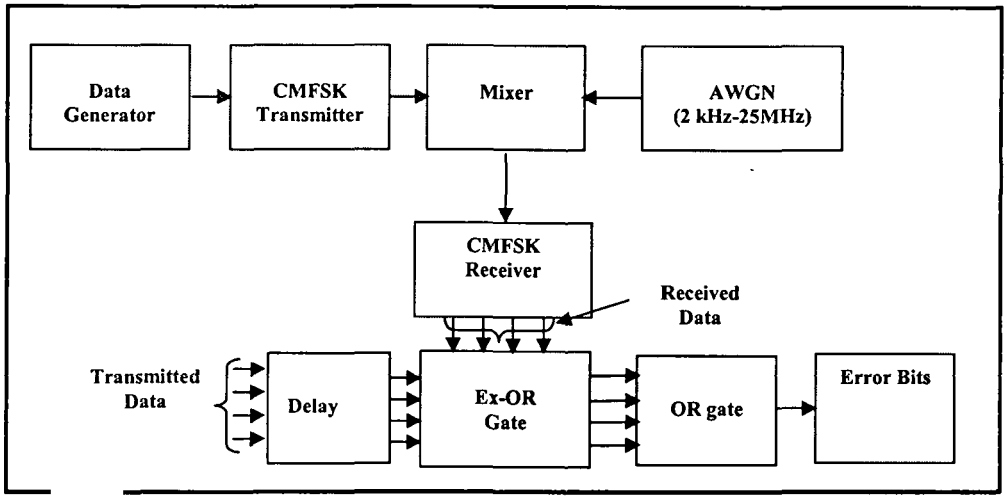

Fig.7.3: Block diagram of SER simulation setup

The errors are measured by comparing the received data with the phase matched transmitted data. Therefore, the transmitted data are synchronized (phase matched) with received data by providing delay to transmitted data. These synchronized data are applied to the four EX-OR gates as shown in the Figure 7.3. At one input of each EX-OR gate, transmitted bit is connected and to other input the corresponding received bit is connected. It is expected that under no noise condition, no errors are detected at the output of the receiver. Under such condition both the inputs to EX-OR [13]-[14] gates are same and the output from the EX-OR gates will be low continuously. For BER/SER estimation of four channels, four EX-OR gates are used one for each channel. Under no noise situation all the four EX-OR gates will have low output continuously as both inputs (transmitted and received) are similar. The output of these EX-OR gates are applied to 4-input OR gate. It will provide high output when any input is high. By counting high bits at the output of the OR gate, total symbol with error are calculated. SER is determined by dividing the total

symbol with error by total transmitted symbols. Using Equation 7.8, BER is calculated from SER.

Figure 7.4 shows the P-Spice simulated circuit diagram for performance analysis of the designed CMFSK system. Figure 7.5 shows waveforms obtained from the simulation setup for BER/SER measurement. Waveform (a) shows the output waveform obtained from simulation setup under AWGN noise condition. In this waveform, the presence of pulse represents a symbol having error. This waveform shows 4-high pulse which represents 4 symbols with error detected by the receiver. In Figure waveform (a) and (b) shows the transmitted and received signals.

Similarly, in Figure 7.6 the waveforms show the high SNR condition and no errors detected by the receiver. In this Figure waveform (a) shows the output signal with no errors, as it is low continuously. Waveforms (b) and (c) show the transmitted signal and received signals of the system.

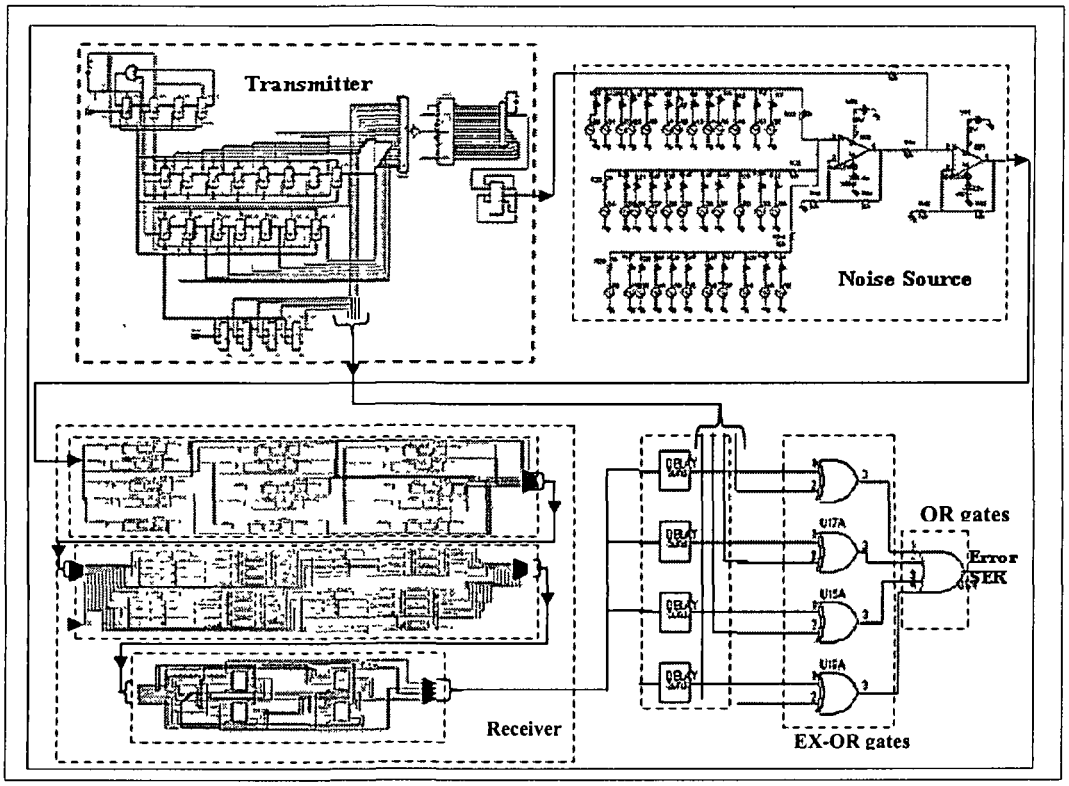

Fig.7.4: Simulated Circuit diagram for SER estimation

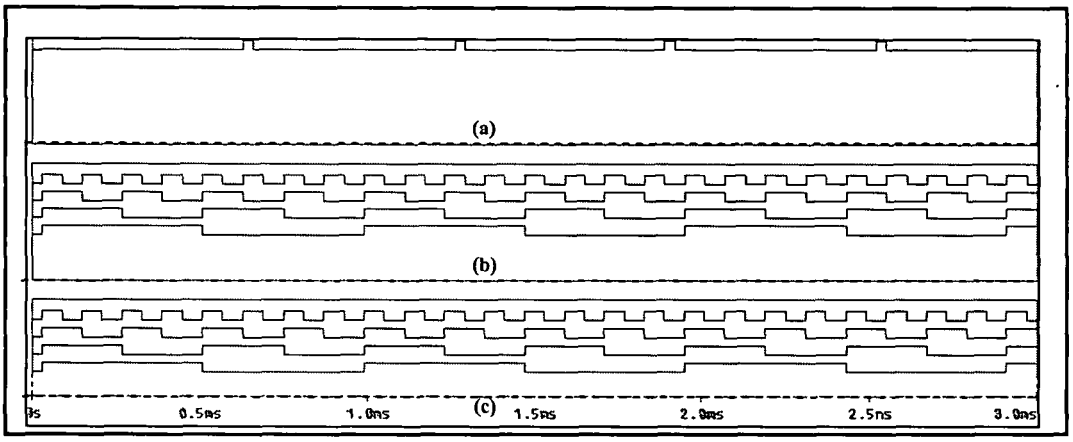

Fig. 7.5: Simulated waveform for SER with noise, (a) Output from EX NOR gate high pulses errors in the received signal, (b) Input data, (c) Output data

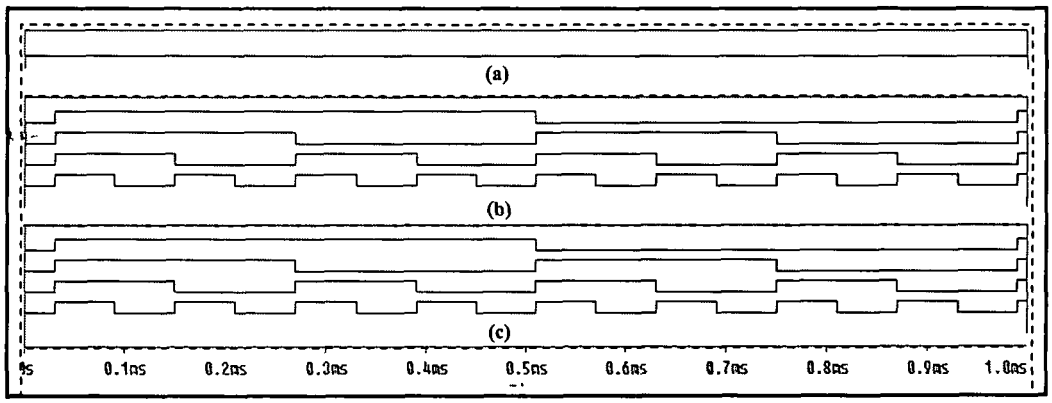

Fig. 7.6: Simulated waveforms for SER without noise, (a) Output of EX-NOR gate, low continuously, as no error (b) Input data, (c) Output

7.3.1 Bit Error Rate

Using the SER simulation setup shown in Figure7.3, we have measured the BER performance of the designed MFSK based FHSS system. The measured BER performance of the receiver under AWGN is plotted in the Figure 7.7. The graph shows that both theoretical and obtained results from the simulation model are same.

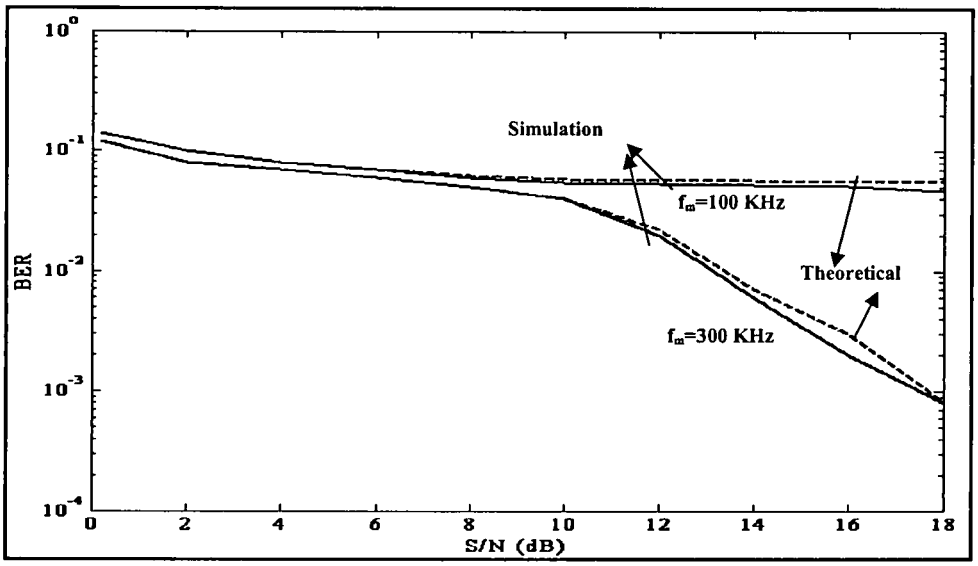

Fig-7.7 BER versus SNR from measurement

We have tested our simulation model of CMFSK/FH system with four channels for BER analysis by using Microsim EDA software release 8.0 Figure 7.8 shows the comparison of SER performance between the existing FH system [7] and the proposed CMFSK/FH system with hop size fm = 100 KHz. The dashed line indicates the SER for CMFSK/FH system obtained using Equation (7.7) and (7.8) and the solid line represent that for existing FH system. It is seen from the Figure that, the SER performance of CMFSK system is better than that of existing FH system [3]. Figure 7.8 shows the comparison of BER performance between analytical and simulation model with hop size 100 KHz and 300 KHz. In the Figure, the dashed line represents analytical curve obtained by using the Equation (7.7), whereas, the solid line shows the simulation results obtained by using P-Spice software Microsim EDA release 8.0. It is seen that the variation of BER with SNR obtained by using analytical method is approximately close with that of simulation result. For other hope sizes (not shown in the figure), the results of our simulation model are also closely matched with the analytical results.

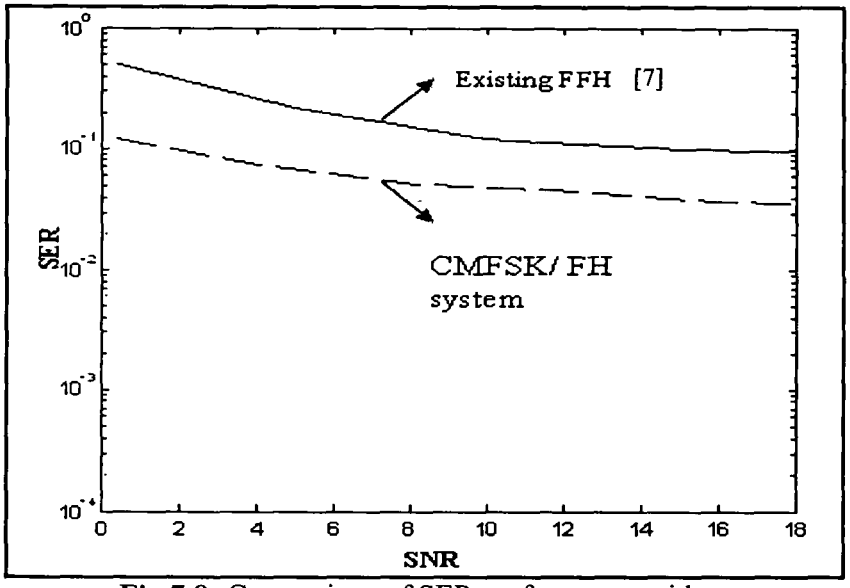

Fig.7.8: Comparison of SER performance with existing FH system [7], and proposed CMFSK

Figure 7.9 shows BER performance of the CMFSK/FH circuit using simulation model with fm = 50 kHz, 100 kHz, 300 kHz, and 500 kHz. It is seen in the Figure that in case of f_m ~50 kHz, BER performance is worst and for f_m = 500 kHz, BER performance is best among all the hop sizes, that we have taken for simulation. So BER performance of the circuit is degraded as f_m reduces. For better BER performance we can take higher hop size but bandwidth requirement is more. Actually, the bandwidth is formulated in terms of frequency hope size for K number of channels as:

$$Bandwidth = \left(2^K - 1\right) f_m . \qquad (7.9)$$

In case of f_m =50 kHz, 100 kHz, 300 kHz, and 500 kHz, the bandwidth required for four channel CMFSK/ FH system obtained by using the Equation. 6.8 are =750 kHz, 1.5 MHz, 4.5 MHz, and 7.5 MHz respectively. As f_m increases, the bandwidth requirement increases. For further study, one can choose the intermediate hop size 100 kHz, and 300 kHz for which BER are 3.5×10^{-2} and 1×10^{-2} respectively at SNR =12.8 dB.

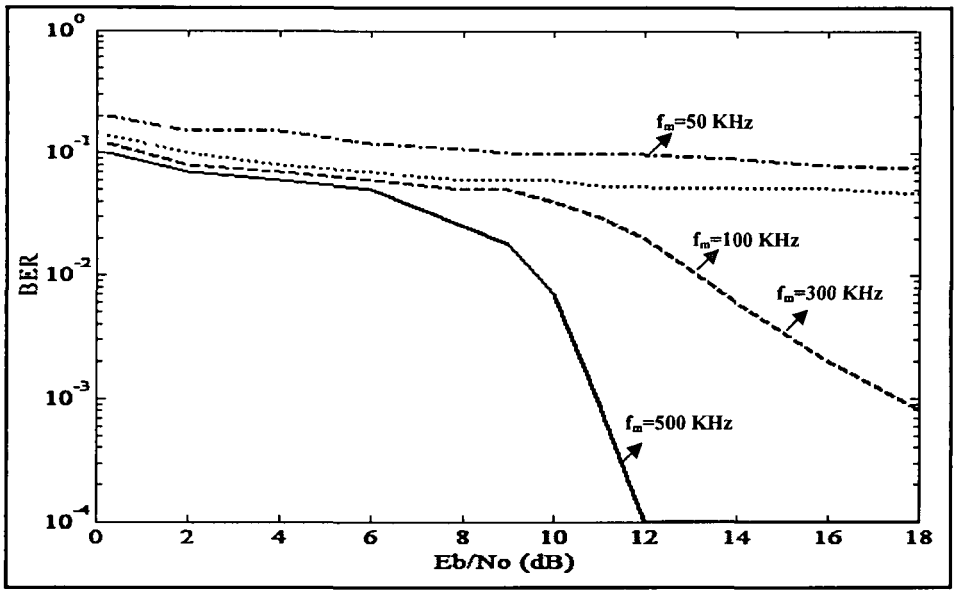

Fig.7.9: BER Performance of CMFSK with different hop

We have also measured BER with varying hope size at SNR =0.4 dB, 4 dB, 8 dB, and 12 dB using our simulation model, as shown in Figure 7.10. It is seen in the Figure that the BER reduces with increase of hop size and for higher SNR, this reduction of BER is faster than that for lower SNR ratio.

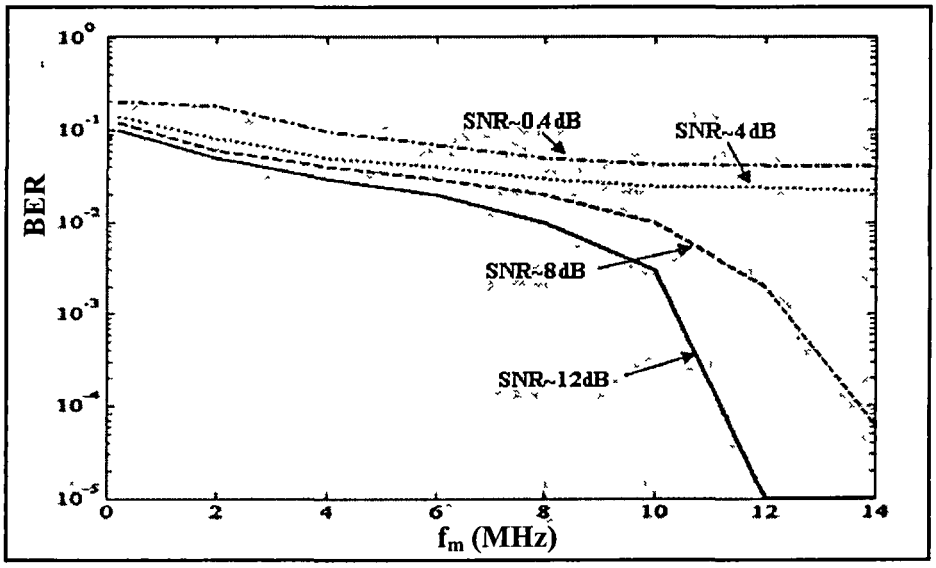

Fig.7.10: BER performance variation of CMFSK with frequency (f_m)

7.4 Performance of Code M-ary CMFSK based FHSS System with proposed Frequency to Voltage Converter

In Chapter 6 we discussed the design and simulation of CMFSK system using proposed wide band FVC for band pass filters to reduce the circuit complexicity [15]-[19]. The system was designed with considering four users. The performance of this circuit is tested using P-Spice software Microsim and with BER measurement setup as shown in Figure 7.3.

7.4.1 Analytical model for BER under AWGN

As discussed, in Chapter 6, that we have designed the CMFSK based system for four channels. The performance of M-ary FSK system with non-coherent detection is discussed in [20]-[22]. The designed system using CMFSK based FHSS also uses the same technique, with non-coherent detection therefore, the analytical expression for our system is same as discussed in [23] - [25] and given as:

$$P_s = \sum_{K}^{M-1} \left(\frac{M-1}{K} \right) \frac{(-1)^{K+1}}{K+1} e^{\left(-\frac{K}{K+1} \frac{E_s}{N_o} \right)} \qquad (7.10)$$

when M=2(binary system), above Equation (7.10) reduced to simple form of as:

$$P_s = \frac{1}{2} e^{-\frac{E_s}{N_o}} \qquad (7.11)$$

If one of M possible symbols is transmitted, the number of bits required to specify this symbol is $Log_2 M$. Since in M-ary each symbol is represented by n-bit binary number, the probability of a given data bit being in error is given by the Equation (7.11). Plot for BER is shown in Figure 7.11.

7.4.2 Bit Error Rate from Measurement

We have also tested our proposed CMFSK based FH system for BER/SER performance analysis. The analysis has been carried out by measurement using simulation model of

Figure 7.3 for four channels using P-Spice simulation software Microsim EDA software release 8.0.

Figure 7.11 plots the measured and analytical BER performance and shows the comparison. It shows that upto SNR of 10dB both; the measured and theoretical BER are same and both the plots overlap each other as seen from the Figure. Further, increasing the SNR improves the BER performance of the system but measured value shows more BER than theoretical value. It is because of the filter circuit used in the proposed FVC. For wide band of frequencies there is deviation in the reactance of the inductor used in the filter circuit. The variation in the impedance of filter due to frequency dependant component, caused the output filtered D.C. to vary non-linearly. We have tested the FVC based CMFSK system for different hop size and the plot in Figure 7.11 shows BER performance with hop size of 300 KHz. The bandwidth of the 4-channel system with this hop size is 4500 KHz.

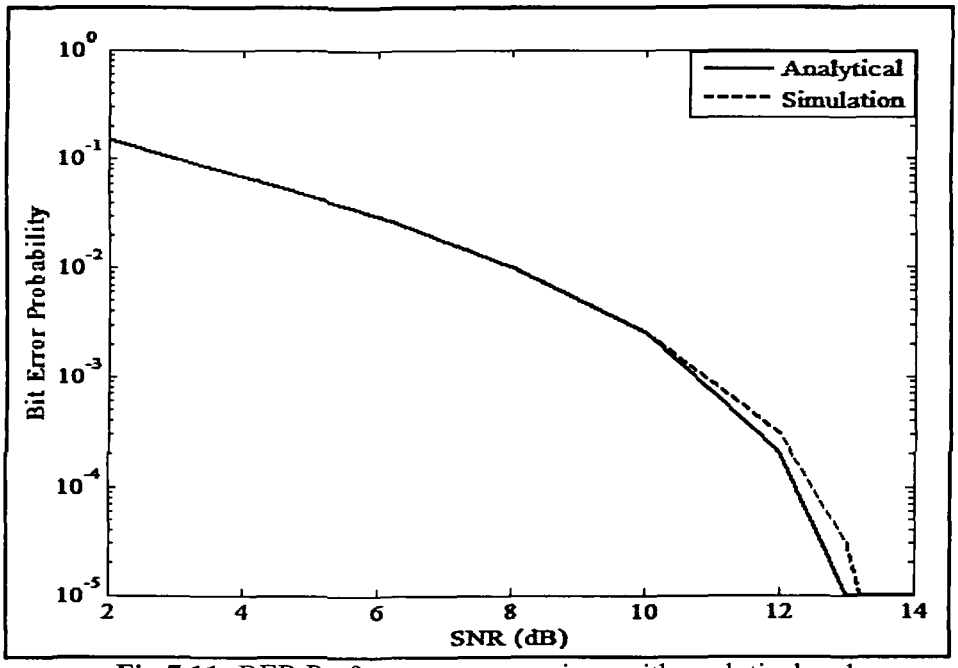

Fig.7.11: BER Performance comparison with analytical and simulation model at f_m 300 KHz

7.5 Performance Measurement with Eye Pattern

The proposed circuit performance has been studied using the eye pattern and Figure 7.12 shows the eye diagram under the AWGN condition for the proposed system CMFSK /FHSS system based on FVC.

In Figure 7.13 we have estimated the noise margin and distortion from the eye pattern using P-Spice circuit simulation. It is seen that with increasing of SNR, distortion due to ISI decreases and noise margin increases. From the eye diagram we have calculated the noise margin and distortion as 0.39 volts and 0.4 volts at a SNR of 10 dB. It is seen that the distortion of the proposed CMFHSS is almost half of the proposed DSSS system with almost same noise margin (discussed in Chapter 5).

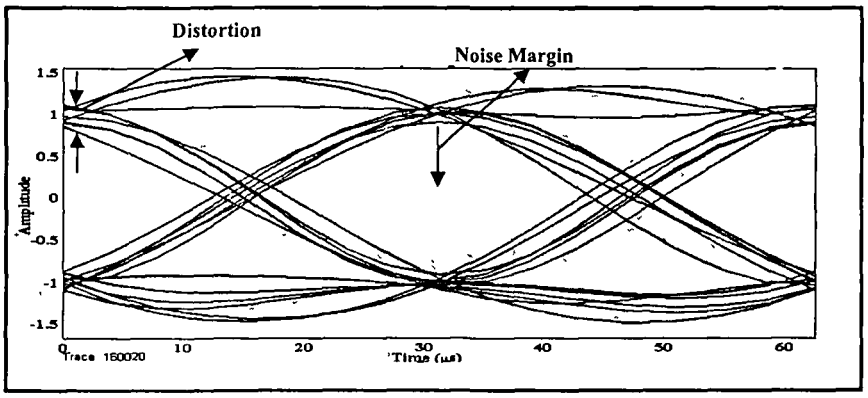

Fig.7.12: Eye diagram of CMFHSS receiver at 12 dB SNR.

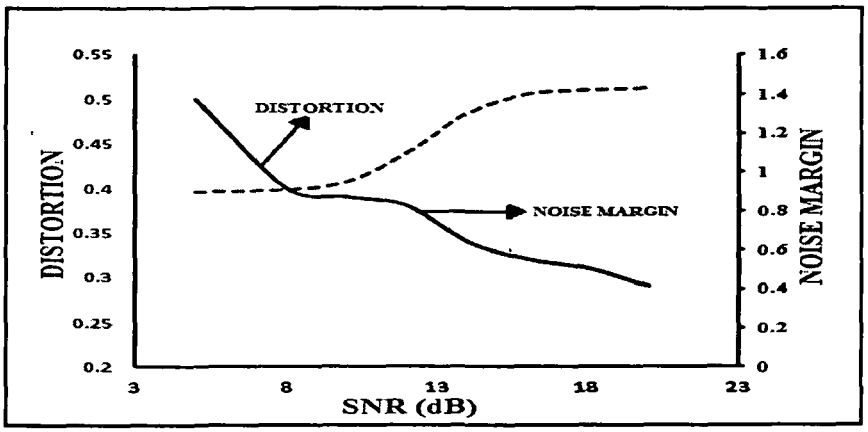

Fig.7.13: Plot for noise and distortion eye diagram

7.6 Comparison of the Proposed DSSS and FHSS under Jamming.

We have carried out the jamming performance of the CMFSK system using measurement setup shown in Figure7.3 and compared with the CPSK based DSSS system as discussed in the Chapter 5. For BER analysis under jamming, we have taken SNR as 12 dB and it is evident from the plot that BER performance under jamming is better for CMFSK system in compare to CPSK based DSSS system as shown in Figure 7.14. The performance improvement is almost constant from -14 dB JSR to -4dB JSR. At -8dB JSR, DSSS system gives 0.25×10^{-2} BER whereas from FHSS system provides 0.5×10^{-3} BER. Similarly, at -14dB these measurements are as 0.25×10^{-3} and 0.45×10^{-4} respectively. This shows that there is a linear degradation in the performance with jamming signal. It is also seen that the BER of the FHSS system is less than that of the DSSS system because FHSS uses more frequencies with hopping in comparison of DSSS using single frequency. So the FHSS system is less jammed with jamming signal than that of the DSSS system.

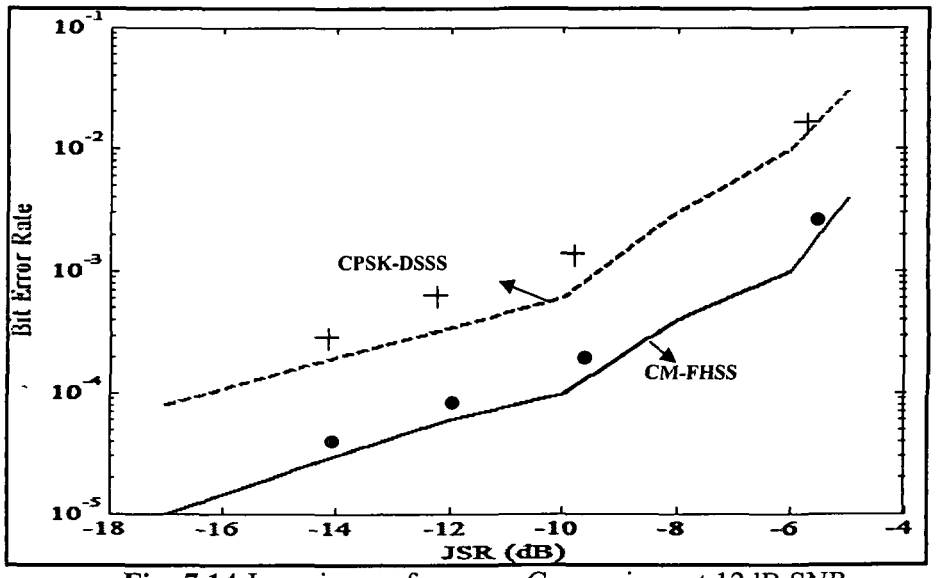

Fig- 7.14 Jamming performance Comparison at 12dB SNR

The cross sign and black dot in the Figure 7.14 shows the experimental values of BER at different values of JSR and these experimental results are discussed in Section 7.7.

7.7 Performance Measurement Experimentally

We implemented the designed four channel BPF based FHSS transceiver (shown in Figure 6.25) and FVC based FHSS (shown in Figure 6.40) on copper clad using different components discussed in Chapter 6 [26]. Figure 7.15 shows the experimental setup. Figure 7.16 shows oscilloscope traces of waveforms of different stage of FVC based FHSS. Trace (a) shows the waveform of four channels. Trace (b) shows PN sequences generated by PN sequence generator circuit. Trace (c) shows the output of voltage control oscillator (VCO). Trace (d) shows the output of frequency to voltage converter stage. Trace (e) shows the output of the decoded 4-chennels.

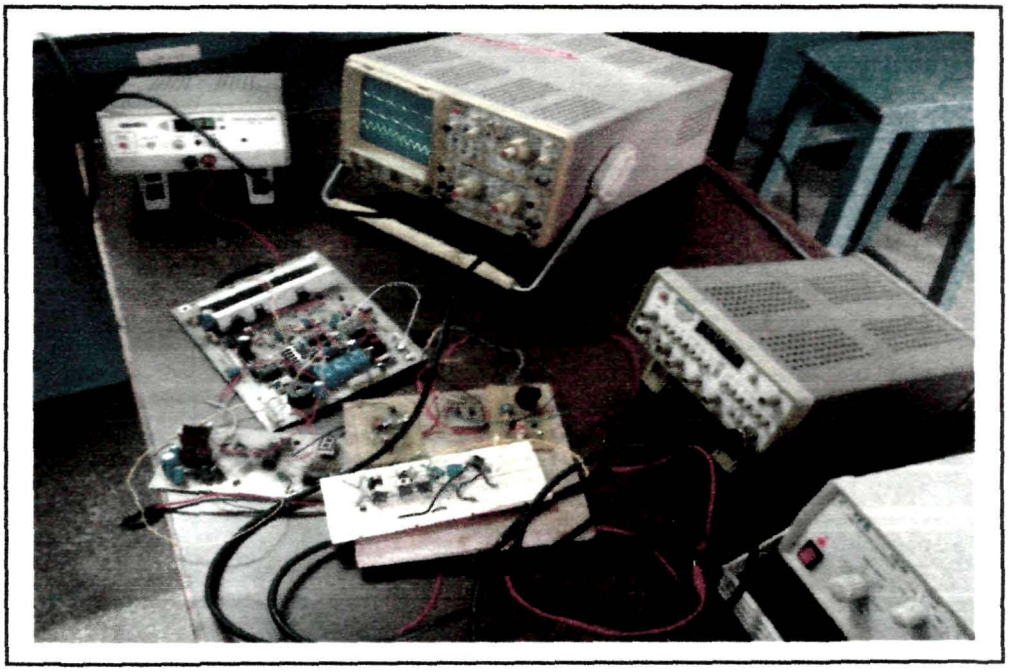

Fig.7.15: Experimental Setup for CMFSK based FHSS system

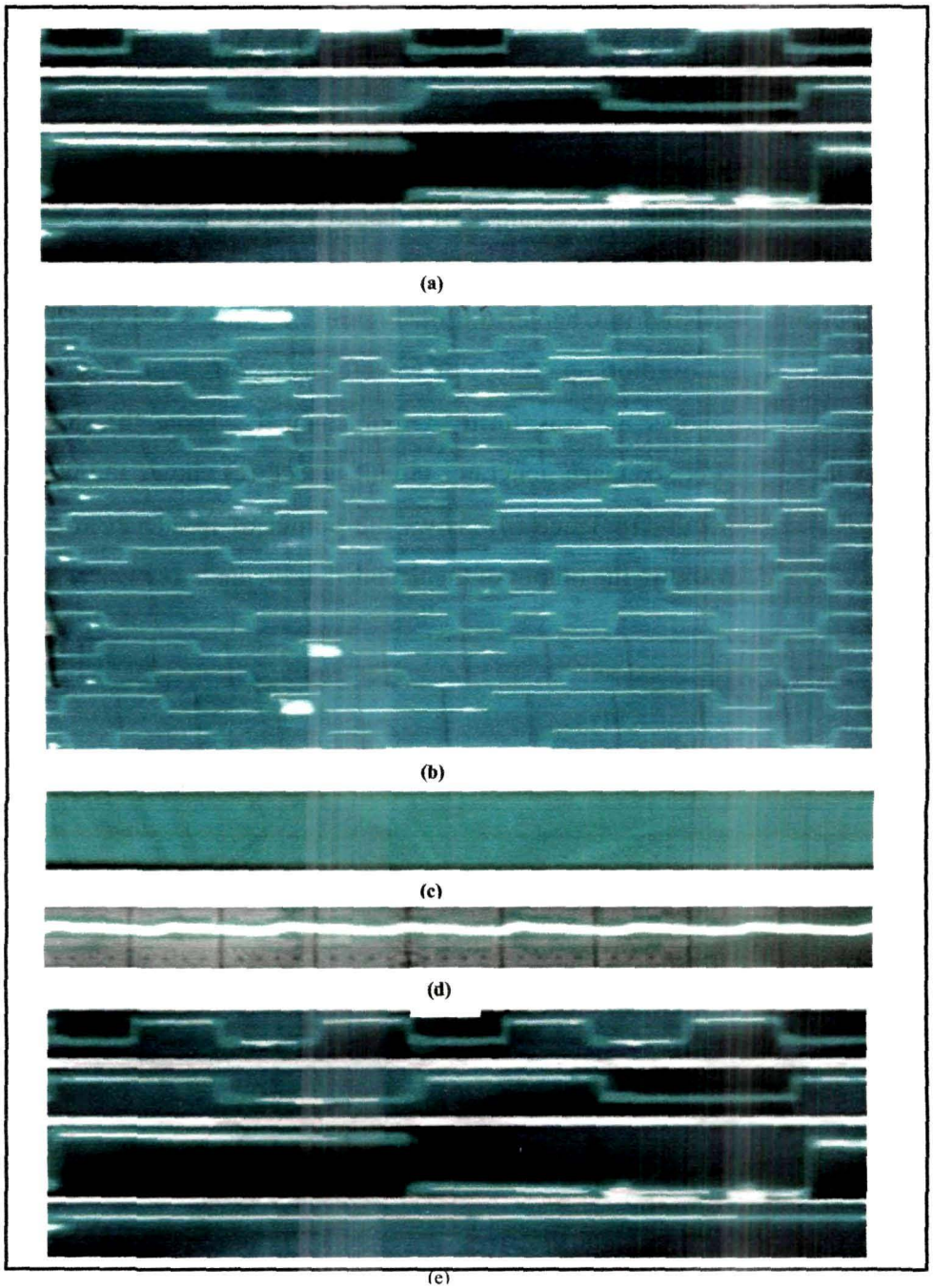

Fig.7.16: Oscilloscope traces of FVC based FHSS transceiver (a) Waveform of 4 Channels (b) PN sequences (c) VCO output (d) FVC output (e) Separated 4 channels at receiver

The traces of PN sequences and four channels shown in the Figure are matched well with simulated waveforms of PN sequences and four channels. We have measured BER by using BER meter at SNR values of 12 dB for different of JSR values of both DSSS and FHSS transceiver. It is seen that the experimental values of BER are close with simulated values of BER (shown in Figure 7.14). We have measured ripple voltage from FVC output and shown in Figure 6.32 matching well with theoretical results. The values of ripple voltage, response time of FVC obtained experimentally are also shown in Figure 6.33 also matching with theoretical results.

7.8 Conclusion

In this Chapter, we have analyzed CMFSK based FHSS transceiver for performance evaluation with four users. The performance of FHSS system was evaluated under different hop size of 50 KHz, 100 KHZ and 500 KHz. This circuit was analyzed analytically and with the simulation model. It is seen that for the proposed CMFSK system more the number of user less the SER. At 12 dB SNR the CMFSK system with 2 users provides 0.5 x 10^{-3} SER whereas for 4-CMFSK system it provides 0.5 x 10^{-5} SER. If the numbers of users are increased further, better SER performance is obtained. It is seen from the simulation results that higher the hop sizes lower the SER/BER. At hop size 100 kHz, and 300 kHz for which BER are 3.5×10^{-2} and 1×10^{-2} respectively at SNR of 12.8 dB.

From eye diagram analysis it is seen that with the proposed FVC based CMFSK system noise margin and distortion are obtained as 0.39 volts and 0.4 volts at a SNR of 10 dB. It shows the improvement in the performance of CMFSK system over CPSK based DSSS system which is discussed in the Chapter 5. We demonstrated FVC based FHSS experimentally and it is seen that the experimental results are matched well with the simulated results.

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Chapter 8

Conclusions and Future Scope

8.1 Conclusions

Due to sky rocketed increase of user and services, present day's wireless communications requires high multi channel capability within limited available bandwidth [1]-[3]. In this thesis we have proposed and studied multi-channel code phase shift keying based DSSS and code M-ary frequency shift keying based FHSS transceiver using multiplexing techniques [4]-[6]. Firstly, we have tried to describe the basics of spread spectrum communication with direct sequence and frequency hopping concept from the previous studies, it is seen that most of the previous works are related to single channel communication [7]-[9]. We have reviewed previous works on different multiplexing techniques which can deal this issue without degradation of signal due to jamming signal [10][-11]. In this thesis, we tried to use multiplexing technique for development of multichannel capability.

In our works, first we have proposed and demonstrated CPSK based DSSS transceiver accommodating 4 users with 100 MHz carrier frequency as reported in Chapter 4. The circuit has been designed and simulated by using Microsim software Version 8.0.The simulated waveforms of transmitter and receiver are shown. It is seen that the signal for 4 user separated by decoder in the receiver with delay of 50 to 55 μS (micro seconds) in comparison to transmitted signal of same users. The design of receiver is crucial to improve the BER performance under AWGN [12]-[14] .In order to improve the performance, we have proposed binary phase shift keying demodulator using 90° phase shifter, squarer, summing circuits for CPSK based DSSS receiver. We have designed and simulated the same receiver circuit. The improvement of BER performance using designed 4-channels DSSS transceiver with proposed BPSK demodulator over proposed BPSK demodulator under AWGN and jamming are shown in Chapter-5. The circuits have been simulated both analytically and with simulation model using Microsim software Version 8.0, as shown in the Chapter 5. The circuit has implemented and BER of the circuit was demonstrated. It is seen that BER at SNR of 8dB and JSR of -8dB is obtained as $\sim 2x10^{-3}$ by using CPSK-DSSS transceiver based

conventional BPSK receiver. And BER at same values of SNR and JSR is obtained as 10^{-4} by using CPSK-DSSS transceiver based on proposed BPSK demodulator. So there is an improvement of BER performance by CPSK-DSSS transceiver based on proposed BPSK demodulator. We have performed eye pattern analysis of the circuit and it is seen that noise margin and distortion for CPSK-DSSS transceiver using proposed BPSK demodulator are obtained as 0.94 volts and 0.5 volts respectively. We have also investigated the effect of phase mismatch in the demodulator and its effect on BER degradation [.

In our works we have also designed 4- channels CMFSK-FHSS transceiver for improvement of performance of BER under AWGN and jamming as shown in Chapter 6. The circuit has been simulated by using Microsim software Version 8.0. The simulated waveform of transmitter and receiver are also mentioned. It is seen that the signals for 4 users are separated by decoder designed in the receiver with delay ~ 55 μS (micro seconds) in comparison to transmitted signals of the same users. The design of the receiver is key to improve the BER performance under AWGN and jamming. In order to improve the same, it is required to reduce circuit complexity as seen in MFSK-FHSS receiver due to having band pass filters (BPF). We have proposed wide band frequency to voltage convert (FVC) with less complicated resistance-capacitor (R-C) circuit for signal processing of CMFSK –FHSS receiver instead of using BPFs [15]-[17]. The BER analysis of both designed 4 channel FHSS transceiver using BPF are FVC have been performed both analytically and with P-Spice simulation model as shown in Chapter7. The BER performance of FHSS transceiver was evaluated under different hop size of 50 KHz, 100 KHz and 500 KHz. It is seen that BER at SNR of 8dB and JSR of -8dB is estimated as $5x10^{-4}$ for BPF based CHFSK–FHSS transceiver whereas BER at the same values of SNR and JSR is 10^{-4} for FVC based CFSK-FHSS transceiver. So there is an improvement of BER of CMFSK-FHSS transceiver based on FVC. We have performed eye pattern analysis of the same circuit and it is seen that noise margin and distortion are obtained as 0.48 volts and 0.37 volts. The distortion is

reduced in CMFSK-FHSS transceiver in comparison CPSK-DSSS transceiver due to frequency hopping concept but with sacrifice of noise margin.

8.2 Future Scope

From out studies, we have seen that CPSK-DSSS has used single carrier frequency for providing services to multi users (where we have designed for 4 users)whereas CMFSK-FHSS has used 15 frequencies with frequency for providing services to multi users(where we have designed for 4 users) to improve the BER performance under AWGN and jamming. So bandwidth requirement for CMFSK-FHSS is more than that of CPSK-DSSS. It is required to use less number of frequencies to reduce bandwidth requirement for CMFSK-FHSS without degradation of BER performance. So reduction of bandwidth in FHSS transceiver is one of the future works in this direction [18]. Recently signal security and safety are important in wireless communication [19]-[21]. So we have to deal these issues both with DSSS and FHSS signaling.

One should definitely look into issue related to inter symbol interference (ISI) which arises due to multi path fading/multi path in wireless communication specially for its use in data communication [22]-[23].

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